

UNIT - I (A)
Operational Amplifier

①

Introduction: In olden days to computing data they use calculator. For speed up and avoiding mistakes they use faster electronic calculators with printing facilities. Over some years these calculators were replaced by a comprehensive electronic device with memory, speed and accuracy. This is called Computer. (Father of computer is - Charles Babbage)

COMPUTER:- Commonly Operated Machine Particularly Used for Technical Educational and Research purpose.

Computer Generations:- 5 types

<u>Generations</u>	<u>Years</u>	<u>Used Technology</u>
1 st	1945 - 55	① Thermionic valves ② magnetic drums ③ vacuum tubes
2 nd	1955 - 65	Transistors
* 3 rd	1965 - 75	Integrated circuit (IC) (a) IC is also some times known as ① chip, ② silicon chip ③ memory chip ④ microprocessor chip → ⑤ 1 st up chip IC (now Intel) (c) SSI, MSI, LSI
4 th	1975 - 85	VLSI (Very Large Scale Integrated ckt)
5 th	1985 - till now	Artificial Intelligence (A.I) & Knowledge Process eg:- Robotics

A.I Def.:- It is an ability to think like human beings.

→ Computer size 1st - 5th → decreasing
→ Memory " " " → Increasing

Classification of IC's

IC Family Properties	Monolithic IC	Thin and Thick Film	Hybrid IC
Substrate	silicon	Glass ceramic	(i) Glass, ceramic (ii) silicon
Structure	Active and Passive devices along with interconnections on a single chip.	Active and Passive devices on an insulating substrate along with interconnection.	(i) Passive devices & interconnections on one insulating substrate with active device wire wound. (ii) Active devices on a single chip while passive devices along with interconnections on thin and thick film.
Active devices	(i) BJT (ii) MOSFET	MOSFET	(i) BJT (ii) MOSFET
Passive devices	(i) Diffused resistors, oxide capacitors (ii) MOS resistors, oxide capacitors	metal film resistor, oxide capacitor	(i) Metal film resistor, cement resistor, oxide capacitor (ii) Metal film resistor, oxide capacitor.
Application	Linear IC	Digital IC	Linear and Digital IC.

IC chip size and circuit Complexity :-



Level of Integration	Year	No. of Transistors/chip
① Small scale Integration (SSI)	1960-65	1-100 Transistors/chip
② medium " " (MSI)	1965-70	100 - 1000
③ Large " " (LSI)	1970-80	1,000 - 20,000 → 8 bit up
④ very " " (VLSI)	1980-90	20,000 - 1,00,000 → 16 & 32 bit up
⑤ Ultra " " (ULSI)	1990 -	$10^6 - 10^7$ → special processors virtual reality machines smart sensors.
Giant		

Integrated circuit (IC) - All the active and passive components are fabricated on the same chip.

Most of IC's are produced by monolithic process. In this process elements like resistors (R), capacitors (C) are fabricated on a single piece of semiconductor material (generally silicon).

Year	IC material
1958	Ge
1959	Si

Another IC technology is called "thick film wafer" or substrate. Such a monolithic process makes low cost mass production of IC's possible.

With the help of IC's the circuit design becomes very simple.

The variety of useful circuit can be built without the necessity of knowing about the complex internal circuitry.

The components used in IC's have different look than the corresponding conventional components but their electronic functioning is same.

IC Package Types:



Metal can Package → Heat dissipation is important.

Criteria: ① High Power application like Power amplifier, Voltage regulator etc.

② For Experimental (or) bread boarding purpose as easy to and

③ It bending (or) soldering of the leads is not required.

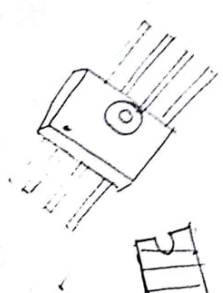
④ Suitable for printed circuit board as lead spacing is more

⑤ More reliability ⑥ Light in weight ⑦ suited for airborne application

⑧ Flat Pack →

Factors affecting selection of IC Package:

- ① Relative cost
- ② Reliability
- ③ Weight of Package
- ④ Edge of IC fabrication
- ⑤ Power to be dissipated
- ⑥ Need of external heat sink.



Manufacturer's Designation for Op-Amp's

(1)

- ① Fairchild $\rightarrow$ $\mu A, \mu A F$
- ② National Semiconductors $\rightarrow$ LM, LH, LF, TBA
- ③ Motorola $\rightarrow$ MC, MFC
- ④ RCA $\rightarrow$ CA, CD
- ⑤ Texas Instruments $\rightarrow$ SN
- ⑥ Signetics $\rightarrow$ N1s, NE/SE
- ⑦ Burr-Brown $\rightarrow$ BB

$\rightarrow$ Depending on operating temperature range, op-amp's are classified into three types:-

- (i) Commercial Grade $\rightarrow$ 0°C to $70^{\circ}\text{C}/75^{\circ}\text{C}$
- (ii) Industrial " $\rightarrow$ -40°C to 85°C
- (iii) Military " $\rightarrow$ -55°C to 125°C

LM741C	Commercial
LM741A	Industrial
LM741	Military

$\rightarrow$ Some op-amps are represented with letters like $\rightarrow$ A, C, E, S, SC
These represent device and its electrical characteristics. Eg:- μA

- (i) $\mu A 741$ $\rightarrow$ Military Grade op-amp
- (ii) $\mu A 741A$ $\rightarrow$ Improved version of $\mu A 741$ (better electrical characteristics)
- (iii) $\mu A 741C$ $\rightarrow$ Commercial Grade op-amp
- (iv) $\mu A 741E$ $\rightarrow$ Improved version of $\mu A 741C$
- (v) $\mu A 741S$ $\rightarrow$ Military Grade op-amp with higher slew rate
- (vi) $\mu A 741SC$ $\rightarrow$ Commercial grade " " " "

Advantages of IC Technology - ③

IC technology offers various Advantages such as

① Small size :-

Practically size of an IC is thousands of times smaller than the discrete circuit.

② Low cost :-

Thousands of silicon wafers consisting of no. of components individually are produced simultaneously called mass production. Due to this, cost of IC is very very low and hence millions of ICs are now in use annually.

③ Less Weight :-

No. of components are fabricated on a single wafer hence weight of IC is very much less compared to a discrete circuit consisting of same no. of components.

④ Low supply voltage :-

IC's work at lower voltages which avoids the need of the large supply voltages.

⑤ Low Power consumption :-

The power consumption of IC's is very very low.

⑥ Highly Reliable :-

Due to absence of soldered connections and less interconnections, the IC's highly reliable from the performance point of view.

→ Due to low power consumption the temp rise of IC is low which increase reliability, accuracy and the life time of IC.

(1) Matched device :-
The characteristics of device can be matched to a high degree of accuracy.

(2) Increased operating speeds.

→ The IC's are used popularly because of versatility, flexibility, dependability along with above advantages.

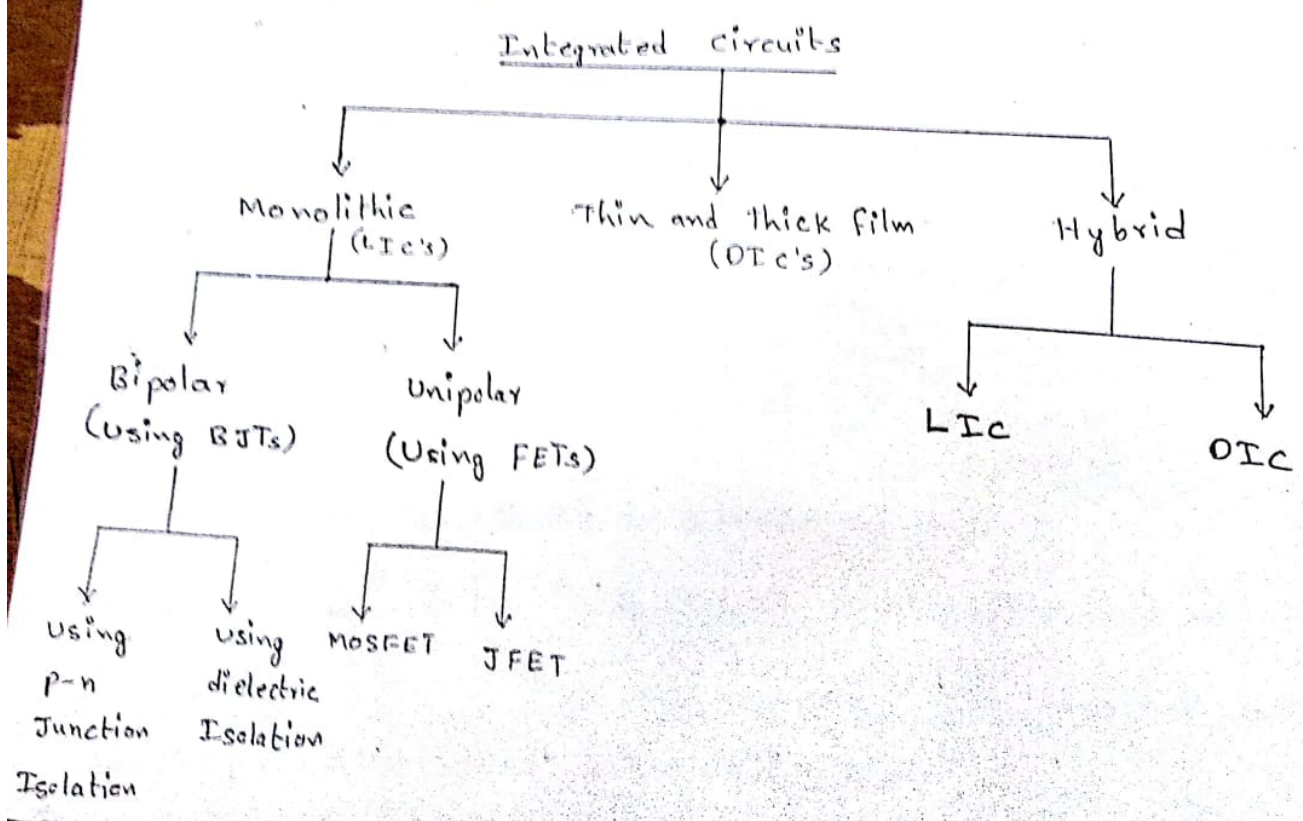
Classification of IC's :-

→ The IC's are broadly classified as

(i) Linear IC's

(ii) Digital IC's

→ The requirements of the above two types of IC's are different hence methods of fabricating these two types of IC's are also different. The various technologies used to fabricate these IC's are,



Operational Amplifier (Op Amp):-

- The operational amplifier is a multi terminal device which internally is quite complex.
- The symbol for an op-amp along with its various terminals, the op-amp is indicated basically by a triangle which points in the direction of the signal flow.
- The operational amplifier in its basic form is a high gain differential amplifier.

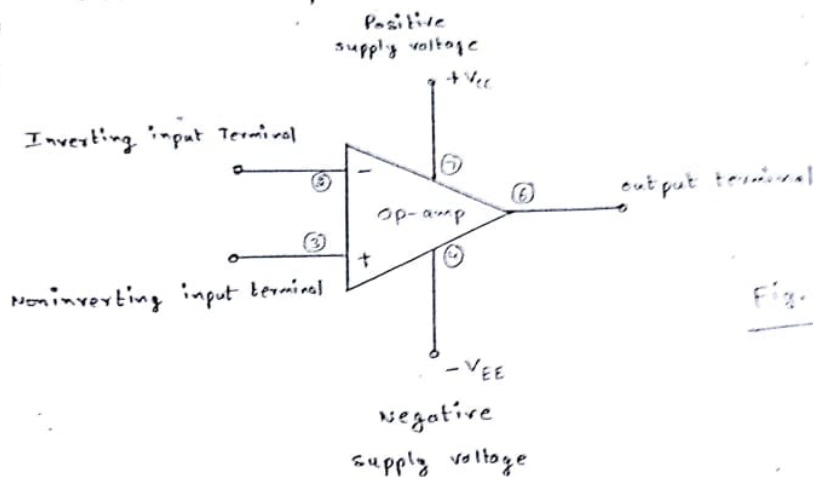
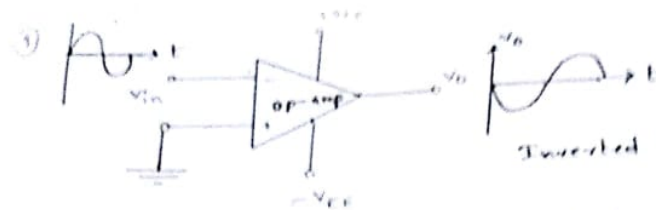


Fig. Op-amp Symbol

All the op-amps have atleast following five terminals:

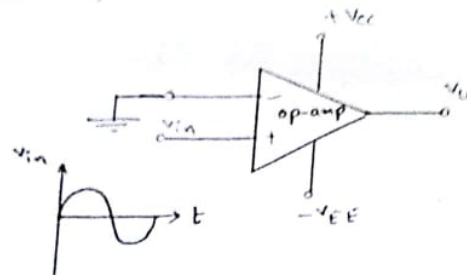
- ① The positive supply voltage terminal V_{cc} (or) $+V$.
- ② " negative " " " $-V_{ee}$ (or) $-V$.
- ③ The output terminal.
- ④ The inverting input terminal, marked as negative.
- ⑤ " Noninverting " " " " positive.

→ The i/p at inverting i/p terminal results in opposite polarity (antiphase) o/p.



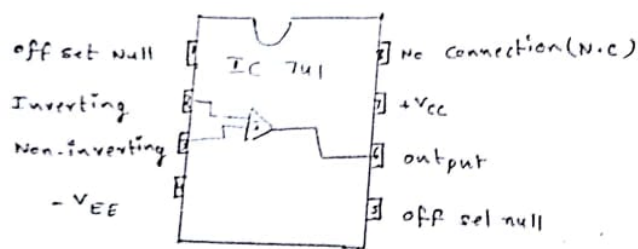
Inverted op with respect to i/p.

→ The i/p at noninverting i/p terminal results in the same polarity (phase) o/p.



Noninverted op in-phase with i/p

Pin diagram -



8 pin mini DIP

- op-amp wants dual supply i.e., $\pm 15V$, $\pm 9V$, $\pm 12V$, $\pm 22V$
- op-amp packages may contain single, dual (two), four (Quad) op-amps.
- The widely used very popular type $\mu A741$ is a single op-amp and is available as an 8 pin can, an 8-pin DIP.

Saturation region → both the junctions are F.B

Cut-off region → both the junctions are R.B

active region → EB is F.B and CB junctions R.B

Block Diagram Representation of Op Amp :-

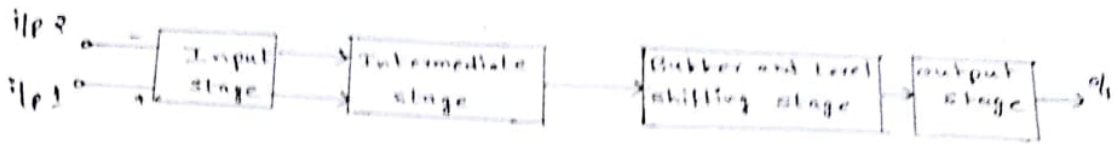


Fig. Internal Block Schematic of an op-amp

Input stage :-

Basic requirements of the i/p stage of op-amp are

- ① high voltage gain
- ② high i/p impedance
- ③ Two i/p terminals
- ④ small i/p offset voltage
- ⑤ small i/p offset current
- ⑥ high CMRR
- ⑦ low i/p bias current

→ All such requirements are achieved by using the dual i/p, balanced op diff. amp as the i/p stage.

Intermediate stage :-

→ The o/p of the i/p stage drives the next stage which is an intermediate stage. This is another diff. amp. with dual i/p, unbalanced i.e., single ended o/p.

→ The overall gain requirement of the op-amp is very high.

→ The i/p stage alone cannot provide such a high gain.

→ The main function of the intermediate stage is to provide an additional voltage gain required.

→ Practically, the intermediate stage is not a simple amplifier but the chain of cascaded amplifiers called multistage amplifiers.

→ Requirements of the intermediate stage:

→ very high voltage gain

→ Direct coupling without coupling capacitor.

prevent = 8

Level shifting stage:-

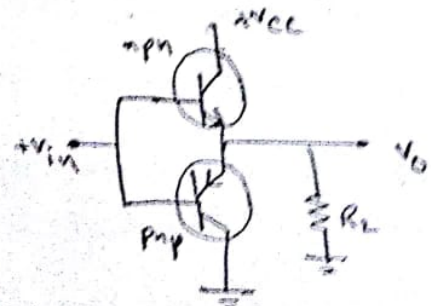
- All the stages are directly coupled to each other as the op-amp amplifies d.c. signals also, the coupling capacitors are not used to cascade the stages.
- Hence the d.c. quiescent voltage level of previous stage gets applied as the i/p to the next stage. Hence stage by stage d.c. level increases well above ground potential.
- Such a high d.c. voltage level may drive the transistors into saturation.
- This further may cause distortion in the o/p due to clipping.
- This may limit the maximum a.c. o/p voltage swing without any distortion. Hence before the o/p stage, it is necessary to bring such a high d.c. voltage level to zero volts w.r.t. ground.
- The level shifter stage brings the d.c. level down to ground potential, when no signal is applied at the i/p terminals. Then the signal is given to the last stage which is the o/p stage.

Buffer:- The buffer is usually an emitter follower whose i/p impedance is very high. This prevents loading of the high gain stage.

Output stage:-

The basic requirements of an o/p stage are ① low o/p impedance, ② Large a.c. o/p voltage swing and ③ High current sourcing and sinking capability.

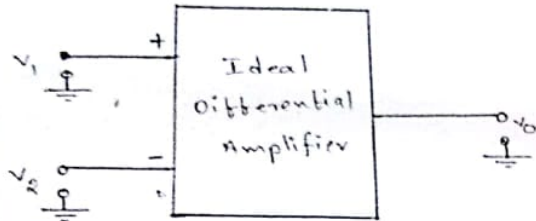
- The push-pull complementary amplifier meets all those requirements and hence used as an o/p stage. This stage increases the o/p voltage swing and keeps the voltage swing symmetrical with respect to ground.



Differential Amplifier :-

(10)

- The op-amp is nothing but a differential amplifier.
- Differential Amplifier amplifies the difference b/w two input voltage signals. Hence it is also called difference amplifier.



→ V_1 and V_2 are the two i/p signals while V_0 is the single ended o/p. Each signal is measured w.r.t. the ground.

$$V_0 \propto (V_1 - V_2)$$

Differential Gain (A_d) :-

$$V_0 \propto (V_1 - V_2)$$

$$V_0 = A_d (V_1 - V_2)$$

The difference b/w the two inputs ($V_1 - V_2$) is generally called difference voltage and denoted as V_d .

$$\therefore V_0 = A_d V_d$$

$$A_d = \frac{V_0}{V_d}$$

$$A_d = 20 \log_{10} (A_d) \text{ in dB}$$

→ Differential gain is expressed in its decibel (dB) value.

Common mode Gain (A_c) :-

- If we apply two i/p voltages which are equal in all the respect to the differential amplifier i.e., $V_1 = V_2$ then

③ Ideally, the o/p voltage $V_o = A_d (V_1 - V_2)$ must be zero.

→ But the o/p voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of two i/p's.

→ Such an average level of the two i/p signals is called 'common mode' signal denoted as V_c .

$$V_c = \frac{V_1 + V_2}{2}$$

Practically:- The diff. amp. produces the o/p voltage proportional to such common mode signal, also.

→ The gain which it amplifies the common mode signal to produce the o/p is called "common mode gain" of the diff amp. Denoted as A_c

$$V_o = A_c \cdot V_c$$

→ So the total o/p of any diff amp can be expressed as

$$V_o = A_d V_d + A_c V_c$$

Common Mode Rejection Ratio (CMRR) :-

→ When the same voltage is applied to both the i/p's the diff amp said to be operated in common mode configuration.

→ Many disturbance, noise signals appears as a common i/p signal to both i/p terminals of diff amp.

→ Such a common signal should be rejected by the differential amplifier.

→ The ability of a diff amp to reject a common mode signal is expressed by a ratio called CMRR.

→ It is defined as ratio of the diff voltage gain (A_d) to common mode voltage gain (A_c)

$$\boxed{\text{CMRR} = \rho = \frac{A_d}{A_c}}$$

Ideally

$$A_c = 0 \Rightarrow \text{CMRR} = \infty$$

$$A_d = \infty$$

$$A_c = 0$$

Practically

A_d is large $\Rightarrow$ CMRR is large
 A_c is small

A_d is large

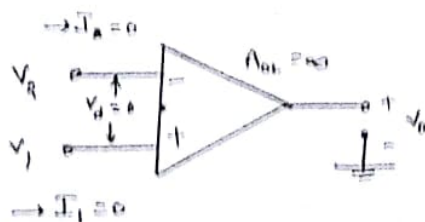
A_c is small

CMRR
in dB

$$\boxed{\text{CMRR} = 20 \log_{10} \left| \frac{A_d}{A_c} \right| \text{ dB}}$$

$$\boxed{V_o = A_d V_d \left[1 + \frac{1}{\text{CMRR}} \cdot \frac{V_c}{V_d} \right]}$$

Ideal Op-amp:-



→ An Ideal op-amp it has two i/p signals V_1 and V_2 applied to non-inverting and Inverting terminals resp.

→ An Ideal op-amp draws no current at both the i/p terminals i.e., $I_1 = I_2 = 0$

thus its Input Impedance is infinite ($R_i = \infty$) (Any source can drive it and there is no loading on the driver stage.)

→ The gain of an Ideal op-amp is infinite (∞). Hence the differential i/p $V_d = V_1 - V_2$ is essentially zero for the finite o/p voltage V_o .

→ The op voltage V_o is independent of the current drawn from the op terminals. thus its op impedance is zero.

Op-amp characteristics :-

- ① Infinite Voltage gain i.e., open loop gain ($A_{OL} = \infty$)
- ② Input Impedance ($R_{in} = \infty$) $\rightarrow Z_i = \frac{V_i}{I_i}$ i/p impedance
- ③ Output Impedance ($R_o = 0$) $\rightarrow Y_o = \frac{I_o}{V_o}$ (o/p Imp)
- ④ offset voltage ($V_{ios} = 0$)
- ⑤ Band width (B.W. = ∞)

→ The range of frequencies over which the amplifier performance is satisfactory is called Bandwidth.

i.e., operating frequency is 0 to ∞
i.e., dc to AC.

- ⑥ CMRR ($\rho = \infty$)
- ⑦ slew rate ($S = \infty$) $S = \left. \frac{dV_o}{dt} \right|_{\text{maximum}}$
- ⑧ No temperature Effect
- ⑨ Power supply Rejection Ratio ($PSRR = 0$) $PSRR = \frac{\Delta V_{ios}}{\Delta V_{cc}} \Big|_{V_{EF} \text{ const}}$

Practical op-amp :-

→ The ckt which represents op-amp parameters in terms of physical components for the Analysis purpose is called equivalent ckt of an op-amp.

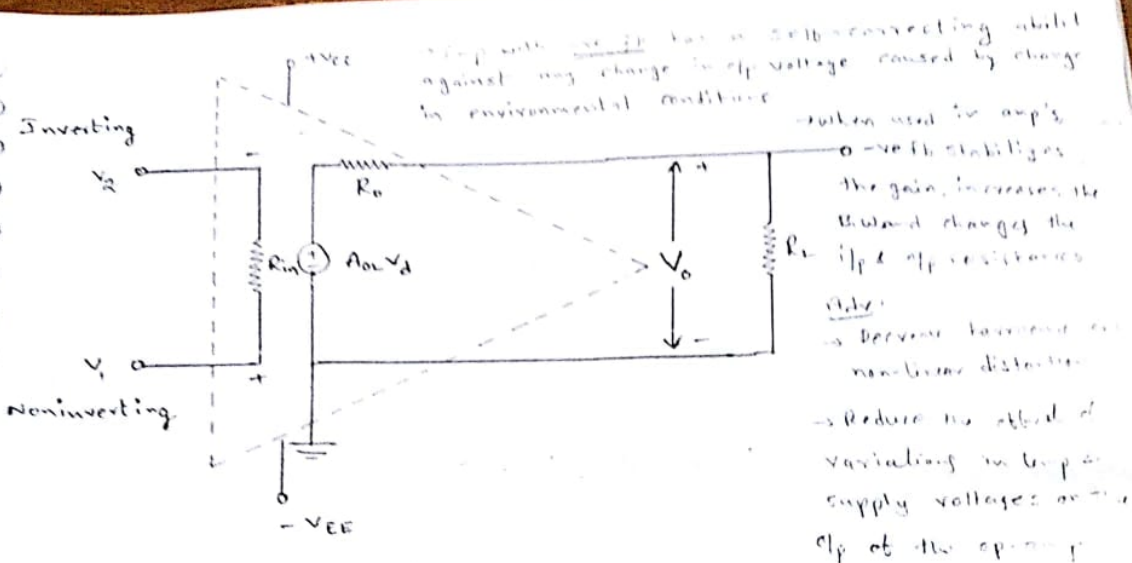


Fig. Equivalent circuit of an op-amp

→ The op-amp amplifies the diff b/w two i/p voltages

$$V_o = A_{OL} \cdot V_d = A_{OL} (V_1 - V_2)$$

→ It is to be noted that the op-amp amplifies different voltages and not the individual i/p voltages. Thus o/p polarity decide by the polarity of the difference voltage V_d .

→ The voltage source $A_{OL} \cdot V_d$ is the thevenin's equivalent voltage source while R_o is the thevenin's equivalent resistance looking back into the i/p terminals.

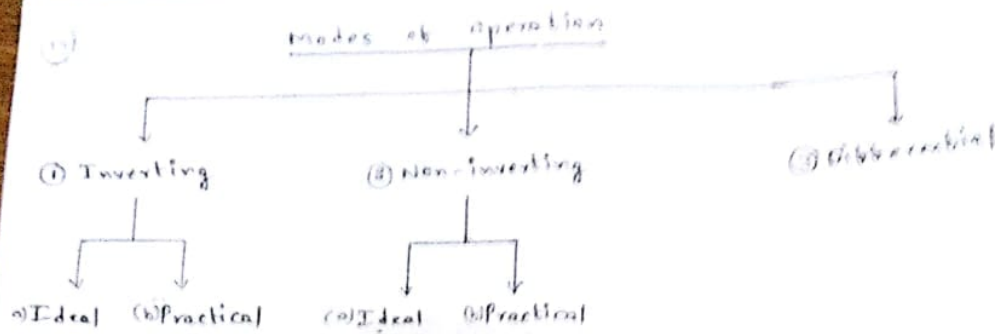
Feedback in Ideal op-amp:-

The utility of an op-amp can be greatly increased providing $-ve$ feedback ($-ve$ f.b.)

regenerative feedback

Note:- There are two basic feedback connections used

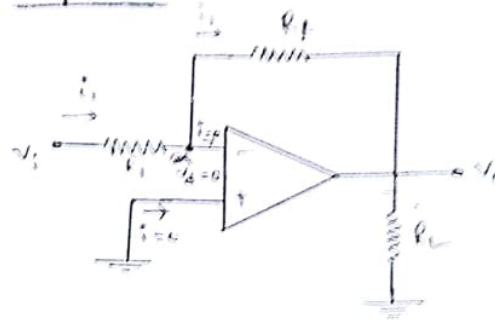
- ① The current drawn by either of the i/p terminals is negligible.
- ② The differential i/p voltage V_d b/w $-ve$ & $+ve$ terminals is essentially zero.



1(a) Ideal Inverting Amplifier:-

→ This is most widely used of all the op-amp circuit.

→ The o/p voltage V_o is feedback to the inverting i/p terminal through the R_f & R_i n/w where R_f is the feedback resistor.



→ Input signal V_i (ac or dc) is applied to the Inverting i/p terminal through R_i and non-inverting i/p terminal of op-amp is grounded.

→ For Ideal op-amp, As $V_i = 0$ node "a" is at grounded potential and the current i_1 through R_i is

$$i_1 = \frac{V_i}{R_i}$$

→ We know op-amp draws no current, all the current flowing through R_i must flow through R_f

$$V_o = -i_1 R_f = -\frac{V_i}{R_i} R_f$$

Hence the gain of Inverting amplifier (closed loop gain)

$$A_{CL} = \frac{V_o}{V_i} = \frac{-R_f}{R_i}$$

From Figure at node 'a'

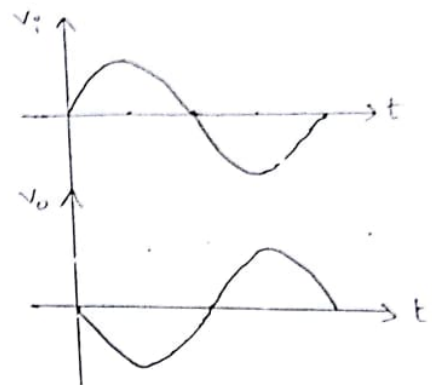
$$\frac{V_i - V_a}{R_i} = \frac{V_a - V_o}{R_f}$$

where $V_a \rightarrow$ voltage at node 'a'
 $\rightarrow$ since node 'a' is at virtual ground $V_a = 0$, then

$$+\frac{V_i}{R_i} = -\frac{V_o}{R_f}$$

$$\frac{V_o}{R_f} = -\frac{V_i}{R_i}$$

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$



$\rightarrow$ The $-ve$ sign indicates a phase shift of 180° b/w V_i and V_o .

$\rightarrow$ Inverting i/p terminal is at virtual ground, the effective i/p impedance is R_i .

$\rightarrow$ The value of R_i should be kept fairly large to avoid loading effect.

$$i_i = \frac{V_i}{R_i}$$

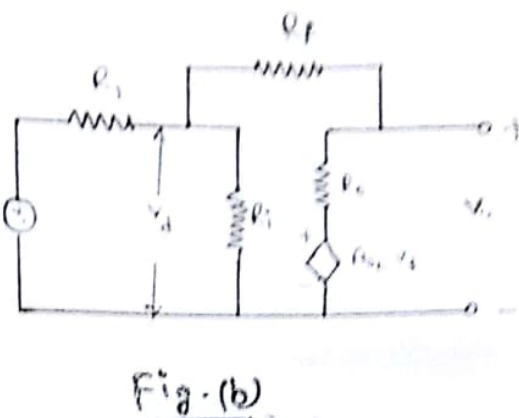
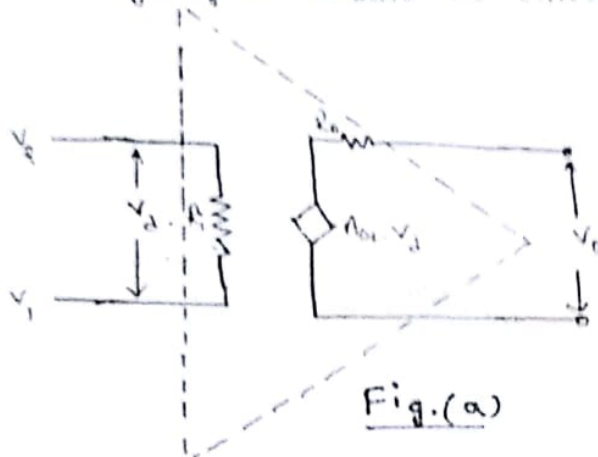
$$V_o = -\frac{R_f}{R_i} V_i$$

$$i_o = i_i + i_L$$

$$i_L = \frac{V_o}{R_L}$$

1(b) Practical Inverting Amplifier:-

→ For a practical op-amp, the expression for the closed loop voltage gain should be calculated using low frequency model.



Equivalent circuit of Practical op-amp Inverting amp.

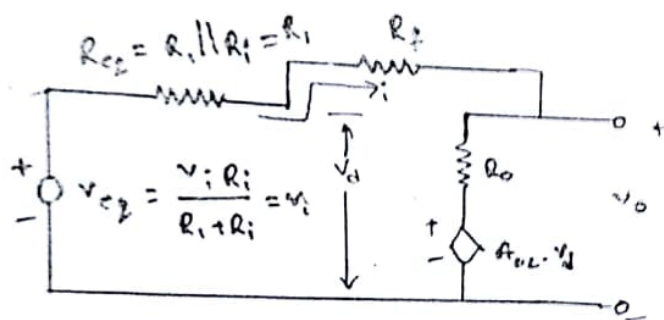
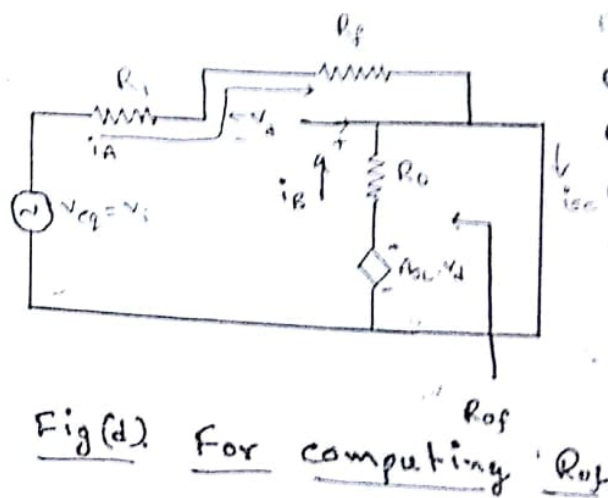


Fig. (c) Simplified ckt
Using Thevenin's



→ Simplified ckt replaced by the signal source V_i and resistors R_1 and R_i by thevenin's equivalent for analysis, to calculate the exact expression for closed loop gain, A_{cl} .

→ $R_i \gg R_1$ so that $V_{eq} = V_i$ and $R_{eq} = R_1$

From o/p loop of Fig. c.

$$V_o = iR_o + A_{ol} \cdot V_d \quad \text{--- ①}$$

$$\text{Also } V_d + iR_f + V_o = 0 \quad \text{--- ②}$$

$$V_d = -iR_f + V_o$$

Substituting Eqn (2) in (1), we get

$$\begin{aligned} V_o &= i R_o + A_{OL} V_d \\ &= i R_o - A_{OL} (i R_f + V_o) \\ &= i R_o - i R_f A_{OL} - A_{OL} V_o \end{aligned}$$

$$V_o + A_{OL} V_o = i R_o - i R_f A_{OL}$$

$$V_o (1 + A_{OL}) = i (R_o - A_{OL} R_f) \quad \text{--- (3)}$$

Apply KVL at fig. D. for getting i/p then

$$V_i = (R_i + R_f) i + V_o \quad \text{--- (4)}$$

closed loop Gain, $A_{CL} = \frac{V_o}{V_i}$

from Eqn (3). $i = \frac{V_o (1 + A_{OL})}{R_o - A_{OL} R_f}$

Substitute 'i' value in Eqn (4), we get

$$\begin{aligned} V_i &= (R_i + R_f) \left[\frac{V_o (1 + A_{OL})}{R_o - A_{OL} R_f} \right] + V_o \\ &= \frac{[(R_i + R_f) (1 + A_{OL})] V_o + V_o (R_o - A_{OL} R_f)}{R_o - A_{OL} R_f} \end{aligned}$$

$$\frac{V_o}{V_i} = \frac{R_o - A_{OL} R_f}{(R_i + R_f) (1 + A_{OL}) + (R_o - A_{OL} R_f)}$$

$$= \frac{R_o - A_{OL} R_f}{R_i + R_i A_{OL} + R_f + R_f A_{OL} + R_o - A_{OL} R_f}$$

$$\frac{v_o}{v_i} = \frac{R_o - A_{OL} R_f}{R_i + R_i A_{OL} + R_f + R_o}$$

$$A_{CL} = \frac{v_o}{v_i} = \frac{R_o - A_{OL} R_f}{R_o + R_f + R_i (1 + A_{OL})}$$

from above $A_{OL} \gg 1$ and $A_{OL} R_i \gg R_o + R_f$ and neglect R_o

$$A_{CL} = \frac{-A_{OL} R_f}{R_f + R_i + R_i A_{OL}}$$

But $A_{OL} R_i \gg R_f + R_i$

$$\therefore A_{CL} = \frac{-A_{OL} R_f}{A_{OL} R_i}$$

$$A_{CL} = -\frac{R_f}{R_i}$$

Input Resistance (R_{if}) :-

$$R_{if} = \frac{v_d}{i}$$

From the loop eqn R_{if}

$$v_d + i(R_f + R_o) + A_{OL} v_d = 0$$

$$v_d (1 + A_{OL}) + i(R_f + R_o) = 0$$

$$v_d (1 + A_{OL}) = -i(R_f + R_o)$$

$$R_{if} = \frac{V_d}{i} = \frac{-(R_f + R_o)}{1 + A_{OL}}$$

R_{if} is $\rightarrow$ the if is given
the terminal, neglect the sign

$$R_{if} = \frac{V_d}{i} = \frac{R_f + R_o}{1 + A_{OL}} \quad \text{Ans}$$

Output Resistance (R_{of}) :-

Output impedance R_{of} (without load resistance R_L) is calculated from the open circuit o/p voltage V_{oc} and short circuit o/p current i_{sc} .

$$R_{of} = \frac{V_{oc}}{i_{sc}}$$

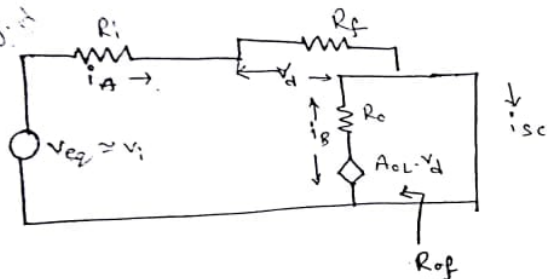


Fig. Equivalent circuit for computing R_{of} .

$$i_A = \frac{V_i - 0}{R_i + R_f} \quad \text{and} \quad i_B = \frac{A_{OL} \cdot V_d}{R_o}$$

$$\text{where, } V_d = -i_A \cdot R_f$$

$$i_B = \frac{-A_{OL} \cdot i_A \cdot R_f}{R_o}$$

$$i_{sc} = i_A + i_B = i_A - \frac{A_{OL} \cdot i_A \cdot R_f}{R_o}$$

$$= \frac{V_i}{R_i + R_f} - \frac{A_{OL} \cdot i_A \cdot R_f}{R_o}$$

substituting i_A value in above eqn in 2nd term

$$i_{sc} = \frac{V_i}{R_i + R_f} - \frac{A_{OL} \cdot V_i \cdot R_f}{R_o (R_i + R_f)}$$

$$= \frac{V_i R_o - A_{OL} V_i \cdot R_f}{R_o (R_i + R_f)}$$

$$= \frac{V_i (R_o - A_{OL} \cdot R_f)}{R_o (R_i + R_f)}$$

$$R_{of} = \frac{V_{oc}}{i_{sc}}$$

$$\text{but } A_{CL} = \frac{V_{oc}}{V_i} \Rightarrow V_{oc} = A_{CL} \cdot V_i$$

$$\begin{aligned} \text{then } R_{of} &= \frac{A_{CL} \cdot V_i}{\frac{V_i (R_o - A_{OL} \cdot R_f)}{R_o (R_i + R_f)}} \\ &= \frac{A_{CL} \cdot R_o (R_i + R_f)}{R_o - A_{OL} R_f} \end{aligned}$$

$$\text{sub } A_{CL} = \frac{R_o - A_{OL} \cdot R_f}{R_o + R_f + R_i (1 + A_{OL})}$$

$$R_{of} = \frac{(R_o - A_{OL} \cdot R_f) R_o (R_i + R_f)}{[R_o + R_f + R_i (1 + A_{OL})] (R_o - A_{OL} \cdot R_f)}$$

$$R_{of} = \frac{R_o (R_i + R_f)}{R_o + R_f + R_i (1 + A_{OL})}$$

If $A_{CL} \rightarrow \infty$ then $R_{of} \rightarrow 0$

Virtual Ground (or) Really Ground :-



→ This means the differential input voltage V_d b/w the non-inverting and Inverting i/p terminals is essentially zero.

→ V_d is very small.

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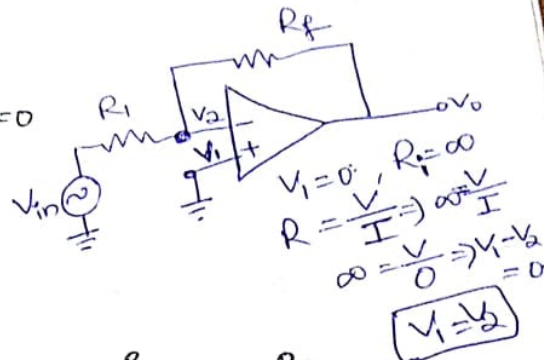
As $A_{OL} \rightarrow \infty$ then $V_d \rightarrow 0$ and assumed to be zero for analysing circuit

$$A_{OL} = \frac{V_o}{V_d} \Rightarrow V_d = \frac{V_o}{A_{OL}}$$

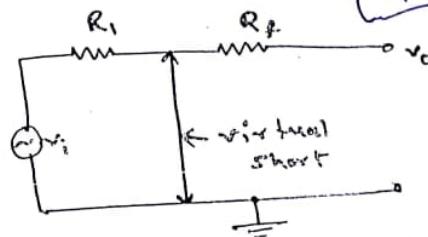
$$(V_1 - V_2) = \frac{V_o}{\infty} = 0$$

$$V_1 - V_2 = 0$$

$$V_1 = V_2$$



→ Thus we can say that under linear range of operation there is virtually short ckt b/w the two i/p terminals. I.e., their voltages are same.



Concept of virtual Ground in an op-amp

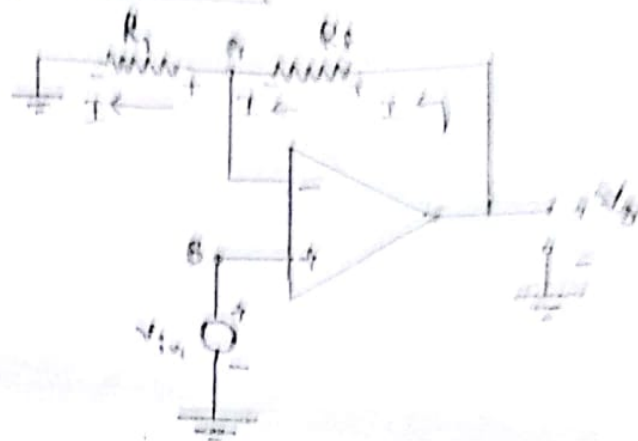
→ No current flows from the i/p terminals to the ground.

→ If the non-inverting terminal is grounded by the concept of virtual short, the inverting terminal also at ground potential through there is no physical connection b/w the Inverting terminal and ground. This is Principle of "Virtual Ground."

→ Assumptions are always used to analyse the Practical op-amp application.

Q2(a) Ideal Non-Inverting Amplifier :

→ An amplifier which amplifies the i/p without producing any phase shift b/w i/p & o/p is called non-inverting amplifier.



→ The i/p is applied to the non-inverting i/p terminal of the op-amp.
 V_d at i/p terminal is zero.

→ The voltage at node A is V_i is same as the i/p voltage applied to non-inverting i/p terminal.

Derivation of closed loop gain :

The node B is at potential V_{in} , hence the potential at point is same as A which is V_{in} from the concept of virtual Ground.

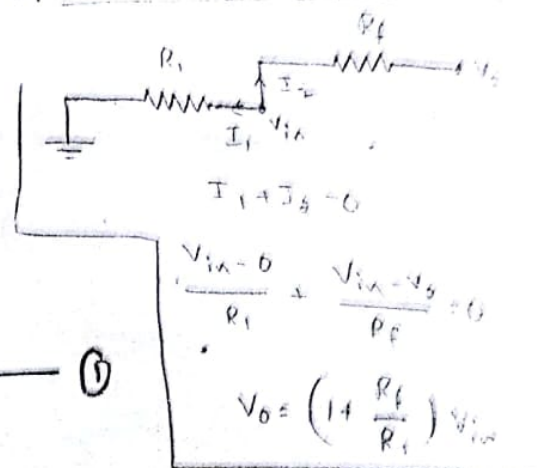
$$V_A = V_B = V_{in}$$

from o/p side

$$I = \frac{V_o - V_A}{R_f} = \frac{V_o - V_{in}}{R_f} \quad \text{--- (1)}$$

At Inverting terminal

$$I = \frac{V_A - 0}{R_1} = \frac{V_{in}}{R_1} \quad \text{--- (2)}$$



Entire current passes through R_f as i_p current at op-amp is zero

Equate Eqn (1) & (2)

$$\frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_i}$$

$$\frac{V_o}{R_f} = \frac{V_{in}}{R_i} + \frac{V_{in}}{R_f}$$

$$\frac{V_o}{R_f} = \left[\frac{R_i + R_f}{R_i R_f} \right] V_{in}$$

$$\frac{V_o}{V_{in}} = \frac{(R_i + R_f) \cancel{R_f}}{R_i \cancel{R_f}}$$

$$= \frac{R_i + R_f}{R_i}$$

$$A_{vp} = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_i}$$

→ The gain can be adjusted to Unity (or) more by proper selection of resistors R_f and R_i .

→ ' R_i ' is more in non-inverting amplifier compared to inverting amplifier.

Ideal Inverting	Ideal Non-inverting
① Gain = $-\frac{R_f}{R_i}$	Gain = $1 + \frac{R_f}{R_i}$
② o/p is inverted w.r.t i/p	No phase shift b/w i/p & o/p.
③ A is Unity (or) less (or) above	A is greater than one.
④ I/p impedance is R_i .	I/p impedance is large.

2(b) Practical Non-Inverting Amplifier :-

The analysis of a practical non-inverting amp can be performed by using the equivalent circuit

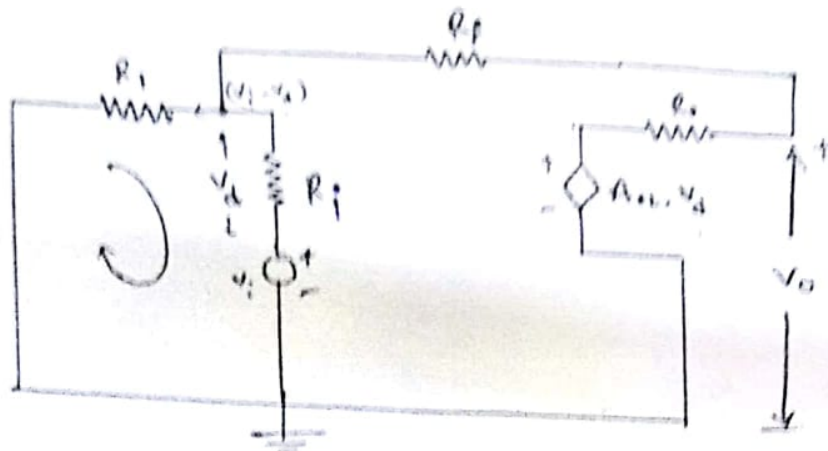


Fig. Equivalent
circuit non-inve-
rting amplifier
Using low
freq model

→ Apply K.C.L at i/p side

$$(v_i - v_d) \gamma_i + v_d \gamma_i + (v_i - v_o - v_o) \gamma_f = 0$$

$$-(\gamma_i + \gamma_i + \gamma_f) v_d + (\gamma_i + \gamma_f) v_i = \gamma_f v_o \quad \text{--- (1)}$$

Apply K.C.L at o/p side

$$(v_i - v_d - v_o) \gamma_f + (A_{OL} v_d - v_o) \gamma_o = 0$$

$$-(\gamma_f - A_{OL} \gamma_o) v_d + \gamma_f v_i = (\gamma_f + \gamma_o) v_o \quad \text{--- (2)}$$

from Eqn's (1) & (2) for $\frac{v_o}{v_i}$, we get

$$A_{CL} = \frac{v_o}{v_i} = \frac{A_{OL} \gamma_o (\gamma_i + \gamma_f) + \gamma_f \gamma_i}{(A_{OL} + 1) \gamma_o \gamma_f + (\gamma_i + \gamma_i) (\gamma_f + \gamma_o)}$$

where all admittances have been taken for simplicity

if $A_{OL} \rightarrow \infty$

$$A_{cl} = \frac{A_{ol}(Y_1 + Y_F)}{1 + A_{ol}Y_F} = \frac{Y_1 + Y_F}{Y_F} = 1 + \frac{Y_1}{Y_F}$$

$$A_{cl} = 1 + \frac{R_F}{R_1}$$

Voltage Follower (or) Unity Gain Amplifier (or) Buffer:

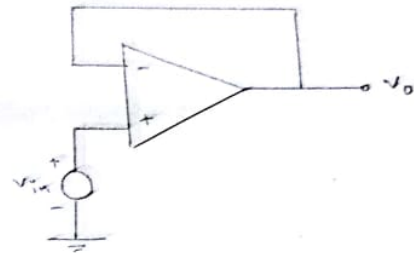
For the non-inverting amplifier
if $R_F = 0$ and $R_1 = \infty$, we get
the modified ckt is as

$$\frac{V_o}{V_i} = 1 + \frac{R_F}{R_1}$$

$$= 1 + \frac{0}{\infty}$$

$$\frac{V_o}{V_i} = 1$$

$$V_o = V_i$$



→ We can say that the o/p voltage is equal to i/p voltage both in magnitude and phase. Hence ckt is called voltage follower.

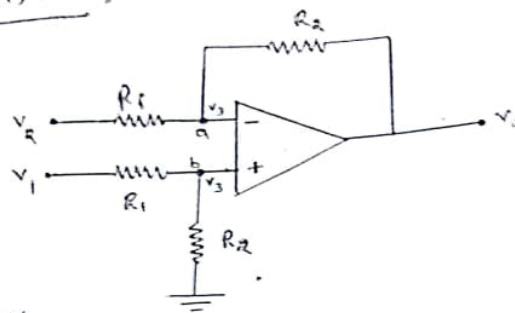
→ This ckt has i/p high impedance (∞) and o/p is zero.

→ Therefore it draws negligible current from the source.

→ Thus a voltage follower may be used as buffer for impedance matching that is to connect a high impedance source to a low impedance load.

③ Differential Amplifier :-

→ A ckt that amplifies the difference b/w two signals is called a difference (or) differential amplifier.



→ This type of the amplifier is very useful in instrumentation ckt's.

→ Since the difference voltage at the i/p terminals of the op-amp is zero. Nodes 'a' and 'b' are same potential indicated with V_3 .

→ Nodal equation at 'a' is

$$\frac{V_3 - V_2}{R_1} + \frac{V_3 - V_0}{R_2} = 0$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) V_3 - \frac{V_2}{R_1} = \frac{V_0}{R_2} \quad \text{--- (1)}$$

→ Nodal equation at 'b' is

$$\frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) V_3 - \frac{V_1}{R_1} = 0 \quad \text{--- (2)}$$

subtracting (2) from (1)

$$\left(\frac{1}{R_1} + \cancel{\frac{1}{R_2}}\right) V_3 - \frac{V_2}{R_1} - \left(\frac{1}{R_1} + \cancel{\frac{1}{R_2}}\right) V_3 + \frac{V_1}{R_1} = \frac{V_0}{R_2}$$

$$\frac{1}{R_1} (V_1 - V_2) = \frac{V_0}{R_2}$$

$$V_0 = \frac{R_2}{R_1} (V_1 - V_2)$$

$$A_{dm} = \frac{1}{2} (A_1 - A_2)$$

$$A_{cm} = A_1 = A_2$$

(This is very useful in detecting very small differences in signals.)

Feature of IC 741 op-amp:-

- ① No frequency compensation required.
- ② Short circuit protection provided.
- ③ Offset voltage null capability.
- ④ Large common mode and differential voltage range.
- ⑤ No latch up.

DC characteristics:-

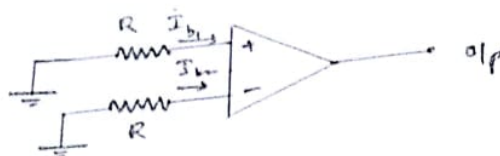
- ① Input bias current (I_b)
- ② Input offset current (I_{ios})
- ③ Input offset voltage (V_{ios})
- ④ Thermal drift
- ⑤ Output offset voltage

the steady state (d.c) response of the op-amp is effected by d.c. characterization.

① Input bias current (I_b) :-

The average value of the two currents flowing into the op-amp i/p terminals is called input bias current (I_b).

(11)



$$I_b = \frac{I_{b1} + I_{b2}}{2}$$

$$I_{ios} = |I_{b1} - I_{b2}|$$

→ Ideally it should be zero while for op-amp 741 IC maximum value of I_b is 500nA.

(2) Input offset current (I_{ios}) :-

→ The i/p stage of the op-amp is the dual i/p differential amplifier and i/p terminals are the base terminals of the two transistor.

→ The input currents of op-amp are the base currents of two transistors Q_1 and Q_2 used in the i/p stage.

→ Ideally, Q_1 and Q_2 must be perfectly matched and two base currents must be equal.

→ Practically, two input base currents difference is small amount.

→ The algebraic difference b/w the currents flowing into the two input terminals of the op-amp is called input offset current (I_{ios}).

$$I_{ios} = |I_{b1} - I_{b2}|$$

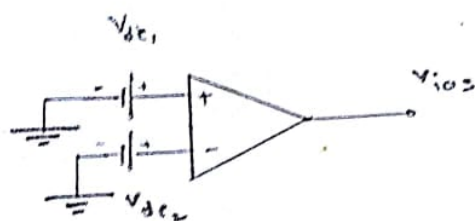
→ Maximum value is 200nA.

③ Input offset voltage (V_{ios}) :-

→ When both the i/p terminals of the op-amp are grounded, ideally the o/p voltage should be zero. However in this condition, the practical op-amp shows a small non-zero output voltage.

→ To make such a voltage zero, it is necessary to apply small difference voltage b/w the two i/p terminals of an op-amp. This voltage is called input offset voltage.

→ The differential voltage that must be applied b/w the two i/p terminals of an op-amp, to make the o/p voltage zero is called input offset voltage (V_{ios}).



$$V_{ios} = |V_{dc1} - V_{dc2}|$$

o/p voltage is zero.

④ Thermal Drift :-

→ The op-amp parameters input offset voltage (V_{ios}), input bias current (I_b) and input offset current (I_{ios}) are not constants but vary with the factors:

- ① Temperature
- ② supply voltage changes
- ③ Time

→ At Temperature = 25°C , parameters are constant.

when temperature raises from 25°C to 35°C the parameters (or) factor changes. The temp changes from 25°C to 35°C is called drift.

offset current drift — $\mu\text{A}/^\circ\text{C}$

" voltage — $\text{mV}/^\circ\text{C}$

$$\text{voltage drift} = \frac{\Delta V_{\text{ios}}}{\Delta T}$$

⑤ output offset voltage :-

→ The output offset voltage is d.c voltage present at the o/p terminals when both the i/p terminals are grounded.

→ Both input offset voltage (V_{ios}) and input bias current (I_b) contribute to generate output offset voltage.

A.C. Characteristics :-

① Frequency Response

② Frequency Compensation

③ Slew Rate

① Frequency Response :-

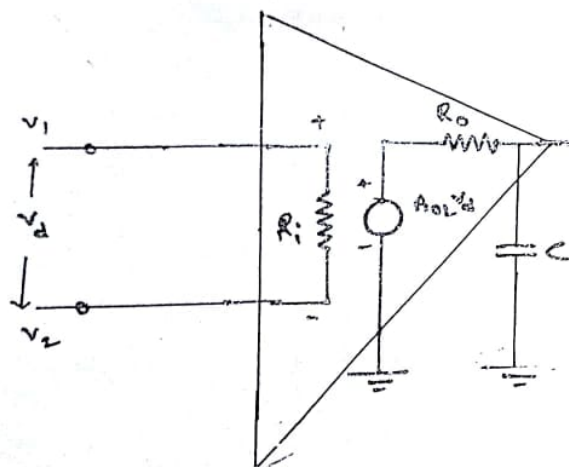
→ Ideally, an op-amp should have an infinite bandwidth. This means the gain of op-amp must remain same for all the frequencies from zero to infinite.

→ Practically, op-amp gain decreases at higher frequencies. Such a gain reduction w.r.t freq is called roll-off.

→ This happens because gain of the op-amp depends on the frequency and hence mathematically it is a complex number. Its magnitude and the phase angle changes with the frequency.

→ The plot showing the variations in magnitude and phase angle of the gain due to the change in freq is called frequency response of the op-amp.

obtaining the Frequency Response:



$$V_o = \frac{1/j\omega C}{R_o + 1/j\omega C} \cdot A_{OL} V_d = \frac{A_{OL} V_d / j\omega C}{1 + R_o j\omega C}$$

$$\frac{V_o}{V_d} = \frac{A_{OL}}{1 + j\omega R_o C}$$

$$A_{OL} = \frac{A_{OL}}{1 + j\omega R_o C}$$

→ Consider the high freq model of the op-amp with a capacitor C at the Output..taking into account the Capacitive Effect present.

→ Let $-jX_c$ be the capacitive reactance due to capacitor C. From above fig, Using voltage divider rule,

$$V_o = -X_c \left[\frac{A_{OL} V_d}{R_o - jX_c} \right]$$

Now $-j = \frac{1}{j}$ and $X_C = \frac{1}{2\pi f C}$

$$V_o = \frac{\frac{1}{j2\pi f C}}{R_o + \frac{1}{j2\pi f C}} \cdot A_{OL} \cdot V_d$$

$$\therefore V_o = j \frac{A_{OL} \cdot V_d}{1 + j2\pi f C R_o}$$

Hence the open loop voltage gain as a function of frequency is

$$A_{OL}(f) = \frac{V_o}{V_d}$$

$$A_{OL}(f) = \frac{A_{OL}}{1 + j2\pi f R_o C}$$

Let $f_o = \frac{1}{2\pi R_o C}$

$$A_{OL}(f) = \frac{A_{OL}}{1 + j\left(\frac{f}{f_o}\right)}$$

Magnitude :

$$|A| = \frac{A_{OL}}{\sqrt{1 + \left(\frac{f}{f_o}\right)^2}}$$

Phase Angle :

$$\phi = -\tan^{-1}\left(\frac{f}{f_o}\right)$$

① Open loop gain A_{OL} is almost constant from 0 Hz to its break freq f_0

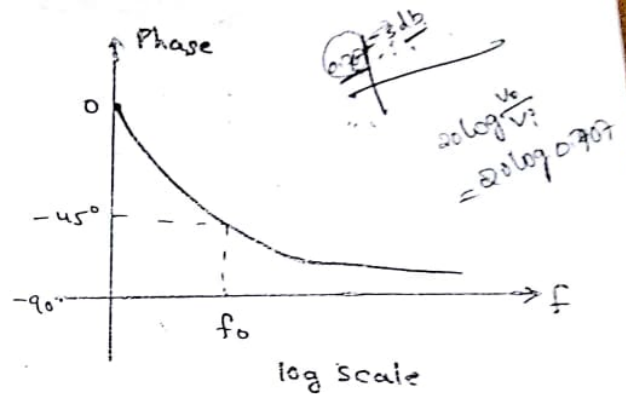
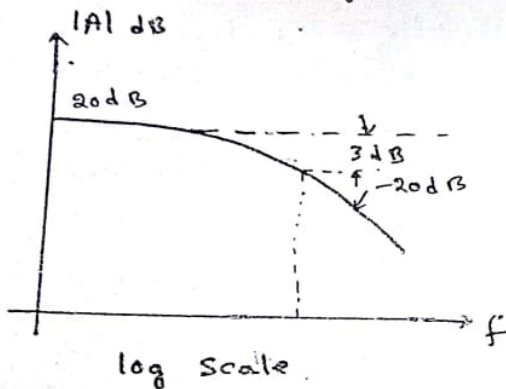
conditions: (i)

① if $f \ll f_0$, magnitude of gain is 20 dB/decade

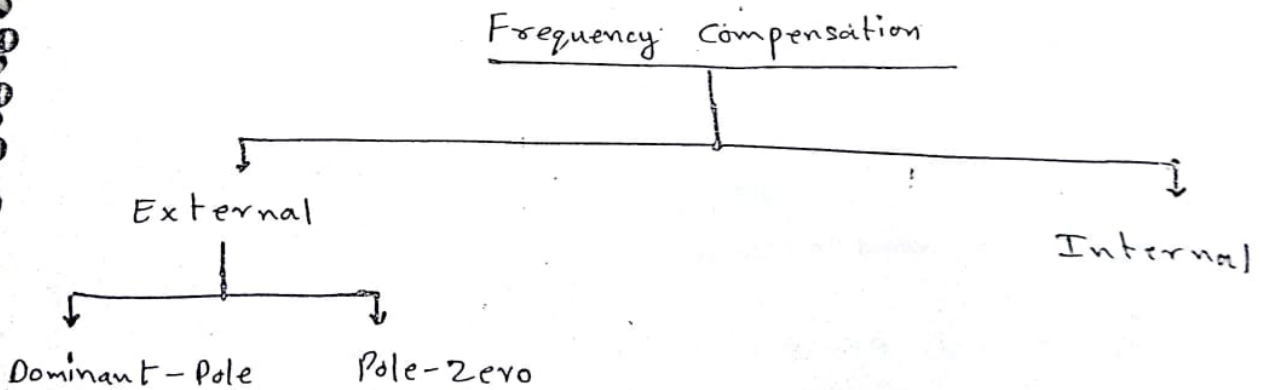
② if $f = f_0$, the gain is 3 dB down from its value at

~~0 Hz~~ Hence the frequency f_0 is also called as -3 dB frequency. It is known as corner frequency.

③ if $f \gg f_0$, magnitude of gain is -20 dB/decade

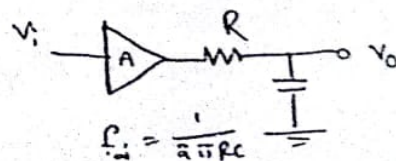


② Frequency Compensation :-



Dominant - Pole :-

→ If 'A' is the uncompensated transfer function of the



op-amp in open loop condition. Introduce a dominant pole by adding RC-network in series with op-amp.

→ Compensated Transfer function, A' becomes

$$A' = \frac{V_o}{V_i} = A \cdot \frac{-j/\omega C}{R - j/\omega C} = \frac{A}{1 + j(f_d/f_a)}$$

where $f_d = \frac{1}{2\pi RC}$

$$A' = \frac{A_{OL}}{(1 + j f/f_d) (1 + j f/f_1) (1 + j f/f_2) (1 + j f/f_3)}$$

$f_d \ll f_1 \ll f_2$

→ The value of capacitor C now can be calculated

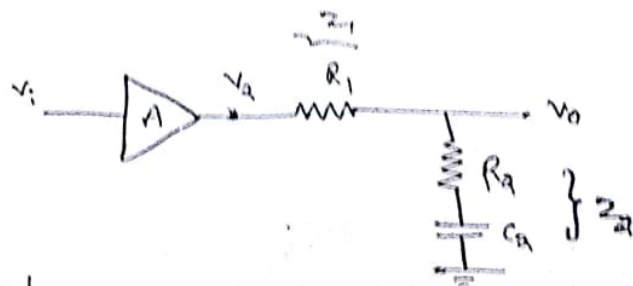
$$f_d = \frac{1}{2\pi RC}$$

Disadvantage:

- ① It reduces the open-loop Bandwidth drastically.
But the noise immunity of the system is improved.

Pole - Zero Compensation:

→ The Uncompensated Transfer function, A is atleast by adding both pole and a zero.



The zero should be at higher frequency than pole

$$\frac{V_o}{V_i} = \frac{Z_2}{Z_1 + Z_2} = \frac{R_2}{R_1 + R_2}$$

where $Z_1 = R_1$, $Z_2 = R_2 + \frac{1}{j\omega C_2}$

$$f_1 = \frac{1}{2\pi R_2 C_2} \quad f_0 = \frac{1}{2\pi (R_1 + R_2) C_2}$$

(3) Slew Rate :-

→ The slew rate is defined as the maximum rate of change of output voltage with time.

The slew rate is specified in $V/\mu\text{sec}$, thus

$$\text{Slew rate} = S = \left. \frac{dV_o}{dt} \right|_{\text{max}}$$

→ Slew rate indicates how fast o/p changes if i/p is also changing. It is specified by operating op-amp in Unity gain condition.

→ Slew rate for the op-amp whose maximum internal capacitor charging current is known

$$S = \frac{I_{\text{max}}}{C}$$

→ For IC741 the charging current is $15\mu\text{A}$ and the internal capacitor 30pF . Hence slew rate is

$$S = \frac{15 \times 10^{-6}}{30 \times 10^{-12}} = \frac{0.5}{10^{-6}} \text{ V/sec} = 0.5 \text{ V}/\mu\text{sec}$$

$$S = 0.5 \text{ V}/\mu\text{sec}$$

→ The op-amp speed is limited by slew rate.

→ An op-amp slew rate is related to its frequency response.

→ op-amp wide B.W. will have higher slew rate.

Op-amp Applications

-ve feedback

Linear

- ① Adder
- ② Subtractor
- ③ V-I Converter
- ④ I-V converter
- ⑤ Instrumentation
- ⑥ Voltage follower
- ⑦ Integrator
- ⑧ Differentiator

Non-Linear

- ① Rectifier
- ② Peak Detector
- ③ Clipper
- ④ clamper
- ⑤ log Amplifiers

+ve feedback

Schmitt Trigger

multi-vibrator

op-amp



* Differentiator :-

→ The ckt which provides the differentiation of i/p voltage at its o/p is called "Differentiator."

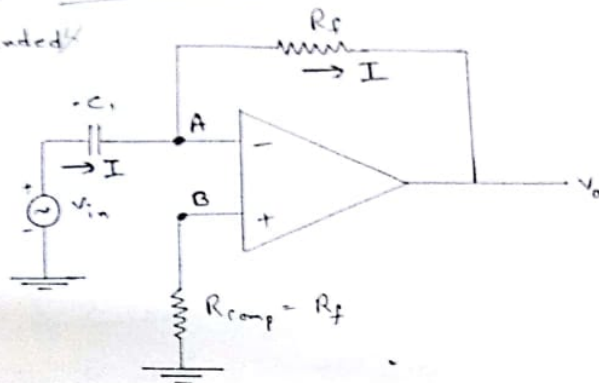
→ The differentiator ckt which does not use any active device is called "passive differentiator."

→ While the differentiator using an active device like op-amp is called an "active differentiator."

Ideal active op-amp Differentiator :-

→ The node B is grounded
the node A is
also at ground
potential hence
 $V_A = 0$

i.e., $V_A = V_B = 0$



→ WKT op-amp never allows any current into its terminals
So the i/p current I is pass through R_f from the i/p &
o/p side, we can write

i/p side & o/p

$$C_1 \frac{d}{dt} (v_{in} - V_A) = \frac{V_A - v_o}{R_f}$$

$$C_1 \frac{dv_{in}}{dt} = -\frac{v_o}{R_f} \quad [\because V_A = 0]$$

$$v_o = -C_1 R_f \frac{dv_{in}}{dt}$$

→ The eqn shows that the o/p is $C_1 R_f$ times differentiates
the i/p and product of $C_1 R_f$ is called time constant
of differentiator.

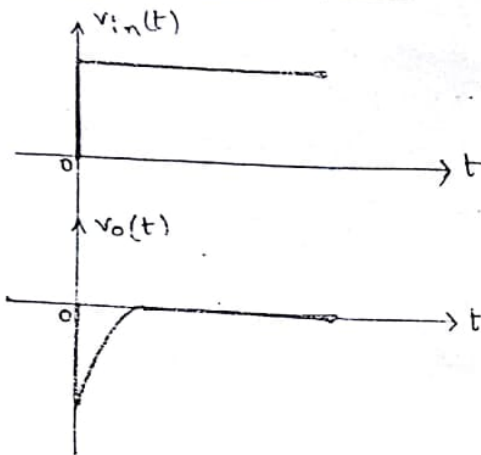
-ve sign indicates that there is a 180° phase shift b/w
i/p & o/p.

② The main advantages of such an active differentiator is the small time constant is required for differentiation.

Input and output Waveforms:

For simplicity of understanding Time constant ($R_f C_1$) is Unity. i.e. $R_f C_1 = 1$

① Step Input signal :- $\rightarrow$ Let i/p is step with magnitude of A unity



mathematically, $V_{in}(t) = A$ for $t \geq 0$

then o/p,
$$V_o(t) = -\frac{dV_{in}}{dt} = -\frac{dA}{dt} = 0$$

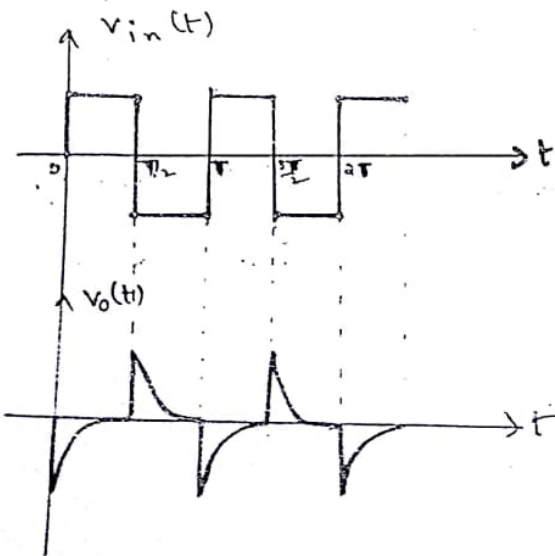
because 'A' is constant.

$\rightarrow$ Actually step i/p takes a finite time to rise from 0 to A volts.

$\rightarrow$ Due to this finite time, the differentiator o/p is not zero.

$\rightarrow$ The ckt acts as an Inverting differentiator, the -ve going ex. impulse appears at $t=0$ after that o/p zero.

② Square Wave input signal :-

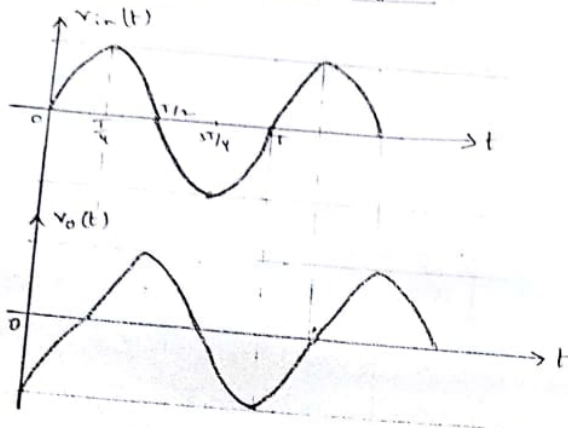


$$V_{in}(t) = A \quad 0 < t < \frac{T}{2} \quad V_o(t) = 0$$

$$= -A \quad \frac{T}{2} < t < T \quad -0$$

$V_{in}(t)$	$V_o(t)$
step	Ramp
Square	Train of Impulse
Sine wave	-ve cosine wave

③ sine wave input signal :-



$$v_{in}(t) = v_m \sin \omega t$$

$$v_o(t) = -\frac{d}{dt} (v_m \sin \omega t)$$

$$v_o(t) = -v_m \omega \cos \omega t$$

$$\text{at } t=0, \quad v_o(t) = -v_m \omega$$

$$t = \frac{T}{4}, \quad v_o(t) = 0$$

$$t = \frac{T}{2}, \quad v_o(t) = +v_m \omega$$

and so on

Frequency Response :-

Consider the op Egn of an Ideal Differentiator

$$v_o(t) = -R_f \cdot C_1 \frac{dv_{in}}{dt}$$

Taking Laplace Transform

$$v_o(s) = -s \cdot R_f \cdot C_1 \cdot v_{in}(s)$$

$$\text{But } s = j\omega$$

$$v_o(j\omega) = -j\omega R_f \cdot C_1 \cdot v_{in}(j\omega)$$

$$\frac{v_o(j\omega)}{v_{in}(j\omega)} = -j\omega R_f \cdot C_1$$

To get freq: response go to magnitude of gain

$$A = \left| \frac{v_o(j\omega)}{v_{in}(j\omega)} \right| = \left| -j\omega R_f C_1 \right|$$

③

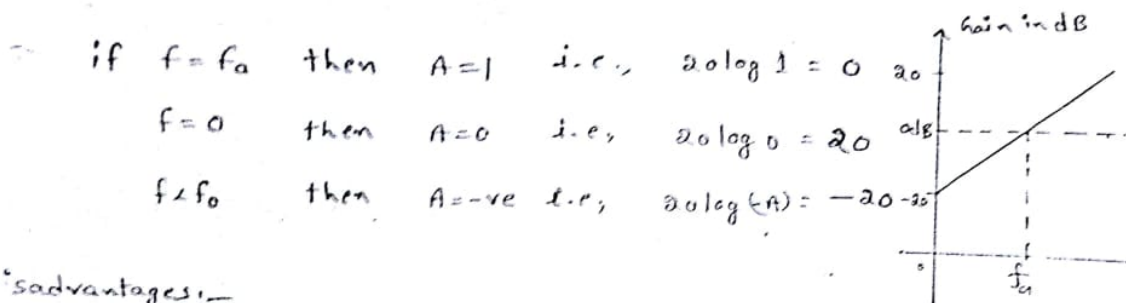
$$A = \omega R_f C_1$$

$$\boxed{A = 2\pi f R_f C_1} \quad (\because \omega = 2\pi f)$$

→ At very low freq such as d.c. $f=0$ the gain is zero.

$f \uparrow$ gain $\uparrow$

Gain can be written as $\boxed{A = \frac{f}{f_0}}$ $\left[\because f_0 = \frac{1}{2\pi R_f C_1} \right]$

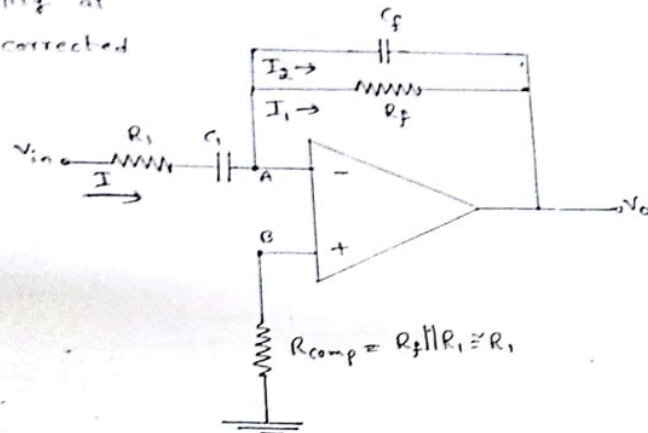


Disadvantages:-

- ① Differentiator ckt suffers from the limitations on its stability and noise problems at high frequency.
- ② $f \uparrow$ gain $\uparrow$ i.e., high c/p no stability.
- ③ I/p impedance $X_C = \frac{1}{2\pi f C_1}$ decrease as $f \uparrow$. this makes the ckt sensitive to noise.
- ④ These problems can be corrected using some additional parameters in differentiator ckt then that is Practical differentiator.

Practical Differentiator :-

→ The noise and stability at high freq can be corrected in the practical differentiator by using resistance R_f in series with C_f and capacitor C_f in parallel with resistance R_f .



→ The ckt having R_{comp} is for bias compensation.

→ Input current of op-amp is zero, there is no current at node B is ground potential due to virtual ground node A is also ground.

$$V_A = V_B = 0$$

At Node 'A' input side current eqn is

$$I = \frac{V_{in} - V_A}{Z_1} = \frac{V_{in}}{Z_1} \quad [\because V_A = 0]$$

$Z_1 = R_1$ in series with C_1 ...

In Laplace domain i.e., $Z_1 = R_1 + \frac{1}{j\omega C_1}$

$$Z_1 = R_1 + \frac{1}{s C_1} = \frac{1 + s R_1 C_1}{s C_1} \quad (\because s = j\omega)$$

$$\boxed{I = \frac{s C_1 V_{in}(s)}{(1 + s R_1 C_1)}} \quad \text{--- ①}$$

$$\text{New } I_1 = \frac{V_A - V_o}{R_f} = -\frac{V_o}{R_f}$$

$$\text{In Laplace } I_1 = \frac{-V_o(s)}{R_f} \quad \text{--- (2)}$$

$$I_2 = C_f \cdot \frac{d}{dt}(V_A - V_o) = -C_f \frac{dV_o}{dt}$$

$$\text{Laplace domain, } I_2 = -s C_f \cdot V_o(s) \quad \text{--- (3)}$$

Apply K.C.L. at node A

$$I = I_1 + I_2$$

$$\frac{s C_1 V_{in}(s)}{1 + s R_1 C_1} = \frac{-V_o(s)}{R_f} - s C_f V_o(s)$$

$$\frac{s C_1 V_{in}(s)}{1 + s R_1 C_1} = -V_o(s) \left[\frac{1 + s R_f C_f}{R_f} \right]$$

$$V_o(s) = \frac{-s R_f C_1 \cdot V_{in}(s)}{(1 + s R_f C_f)(1 + s R_1 C_1)}$$

If $R_f C_f = R_1 C_1$ the

$$V_o(s) = \frac{-s R_f C_1 V_{in}(s)}{(1 + s R_f C_f)^2}$$

(The time constant $R_f C_1$ is much greater than $R_i C_1$ (i.e.) $R_f C_1 \gg R_i C_1$ and hence the above eqn reduces to i.e. $R_f C_1 \gg R_i C_1$)

$$V_o(s) = -s R_f C_1 V_{in}(s)$$

converted into Time domain,

$$V_o(t) = -R_f \cdot C_1 \cdot \frac{dV_{in}(t)}{dt}$$

$$\left[\because s = \frac{d}{dt} \right]$$

Frequency Response :-

$$V_o(s) = \frac{-s R_f \cdot C_1 \cdot V_{in}(s)}{(1 + s R_i C_1)^2}$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{-s R_f C_1}{(1 + s R_i C_1)^2}$$

where $R_f C_1 = R_i C_1$

sub $s = j\omega$

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-j\omega R_f C_1}{(1 + j\omega R_i C_1)^2}$$

$$= \frac{-j2\pi f R_f C_1}{(1 + j2\pi f R_i C_1)^2}$$

$$\text{let } f_b = \frac{1}{2\pi R_i C_1} \quad \text{and} \quad f_a = \frac{1}{2\pi R_f C_1}$$

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$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-j\left(\frac{f}{f_a}\right)}{\left(1 + j\left(\frac{f}{f_b}\right)\right)^2}$$

where f_a & $f_b \rightarrow$ Two break frequencies

$$|A| = \frac{(f/f_a)}{\left[\sqrt{1 + (f/f_b)^2}\right]^2}$$

$$|A| = \frac{(f/f_a)}{1 + (f/f_b)^2}$$

① In case of high f to detect the high f for $f > f_b$ the $1/f$

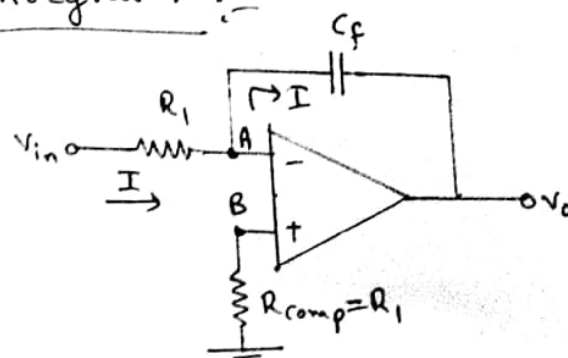
② $f < f_a$ modulates

* Integrator :-

The active integrator can be obtained by exchanging the positions of R and C in the basic differentiator.

Ideal Active Op-amp Integrator :-

→ The node B is grounded. the node A is also at ground from the concept of virtual ground
i.e., $V_A = V_B = 0$



→ As i/p current of op-amp is zero, the entire current I (1) flowing through R_1 also flow through C_f from input side

$$I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1} \quad \text{--- (1)}$$

from output side

$$I = C_f \cdot \frac{d(V_A - V_o)}{dt} \quad (\because V_A = 0)$$

$$= - C_f \frac{dV_o}{dt} \quad \text{--- (2)}$$

Equating two Egn's (1) & (2)

$$\frac{V_{in}}{R_1} = - C_f \frac{dV_o}{dt}$$

$$\frac{dV_o}{dt} = \frac{-1}{R_1 C_f} V_{in}$$

$$V_o = \frac{-1}{R_1 C_f} \int V_{in} \cdot dt$$

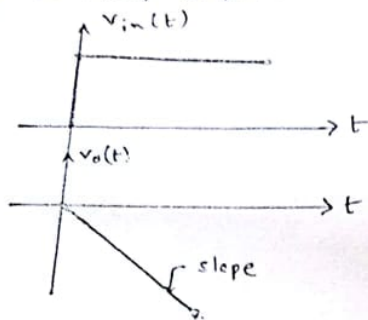
x/o/p is Integration of i/p.

The o/p is $\frac{-1}{R_1 C_f}$ times integral of i/p & $R_1 C_f$ is time constant of Integration.

I/p & o/p wave forms :-

for simplicity $R, C_f = 1$ and initial voltage $v_o(0) = 0$

① Step Input :-



$$v_{in}(t) = A \text{ for } t \geq 0$$

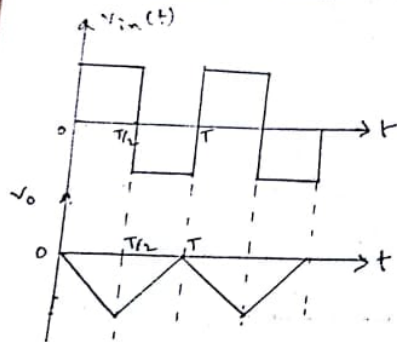
$$= 0 \text{ for } t < 0$$

$$v_o(t) = -\int_0^t v_{in}(t) dt = -\int_0^t A dt$$

$$= -A \int_0^t 1 dt = -A [t]_0^t = -At$$

$$\boxed{v_o(t) = -At}$$

② Square Wave input :-



$$v_{in}(t) = A \text{ for } 0 < t < T/2$$

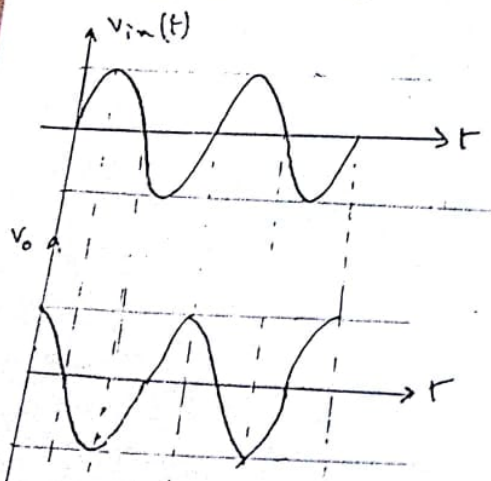
$$= -A \text{ for } T/2 < t < T$$

$$v_o = -At \text{ for } 0 < t < T/2$$

$$= At \text{ for } T/2 < t < T$$

v_{in}	v_o
Step	Ramp
Square	Triangular
Sine	Cosine

③ Sine Wave input :-



$$v_{in}(t) = v_m \sin \omega t$$

$$v_o = -\int v_{in} dt = -\int v_m \sin \omega t dt$$

$$= -v_m \left(-\frac{1}{\omega} \cos \omega t \right)$$

$$\boxed{v_o = \frac{v_m}{\omega} \cos \omega t}$$

Frequency Response of Ideal Integrator :-

Consider o/p eqn of Ideal Integrator

$$V_o(t) = \frac{-1}{R_i C_f} \int_0^t V_{in} dt$$

Take Laplace Transform

$$V_o(s) = \frac{-1}{R_i C_f s} V_{in}(s)$$

Sub $s = j\omega$

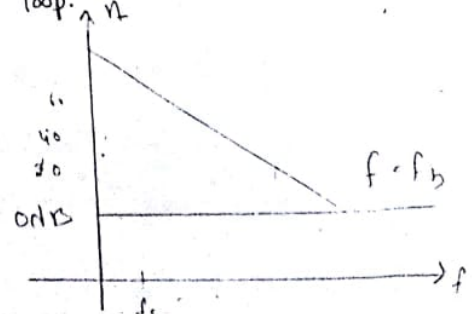
$$V_o(j\omega) = \frac{-1}{R_i C_f j\omega} V_{in}(j\omega)$$

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-1}{j\omega R_i C_f}$$

$$|A| = \left| \frac{V_o(j\omega)}{V_{in}(j\omega)} \right| = \left| \frac{-1}{j\omega R_i C_f} \right|$$

$$|A| = \frac{1}{\omega R_i C_f} = \frac{1}{2\pi f R_i C_f}$$

→ At very low freq i.e., d.c. signals ($f=0$) then gain(∞) then the because of capacitive reactance become very high for low freq. Hence its acts as open loop.



Error in Ideal Integrator

- The op-amp has i_p offset voltage & i_p offset current bcz of high gain these values get amplified and appeared at o/p as error.
- In the presence of i_p signal also the 2 component namely offset voltage and bias current contribute an error voltage at o/p.
- It is not possible to get a true integration of i_p signal at o/p distorted. And it is have less B.W.
- Due to all these limitations an Ideal Integrator is not used in practice.
- Some additional components required to Practical Integrator.

Practical Integrator:-

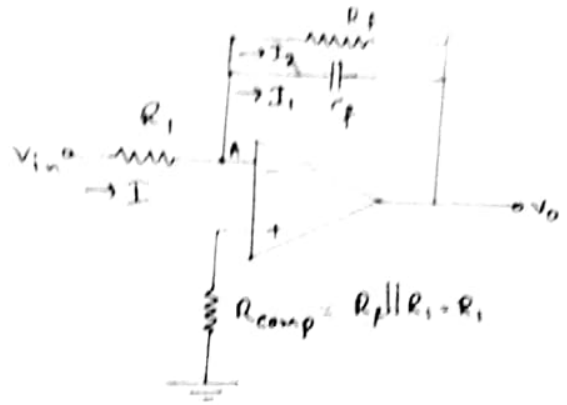
- The limitations of the Ideal integrator can be minimized in the practical integrator ckt.
- In practical integrator we use a resistor R_f in parallel with C_f and R_{comp} is used.
- R_{comp} is used to overcome the error voltage due to i_p offset voltage.
- As the i_p current of op-amp is zero. The node B is still at ground potential. Hence node A is also ground due to virtual ground.

So $V_A = V_B = 0$

The current eqn at 1/p side of Node A

$$I = \frac{V_{in} - V_A}{R_1} \quad (\because V_A = 0)$$

$$I = \frac{V_{in}}{R_1} \quad \text{--- (1)}$$



$$I_1 = C_f \frac{d}{dt} (V_A - V_o) = -C_f \frac{d}{dt} (V_o) \quad \text{--- (2)}$$

$$I_2 = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f} \quad \text{--- (3)}$$

At Node 'A' apply KCL

$$I = I_1 + I_2$$

$$\frac{V_{in}}{R_1} = - \left[C_f \frac{dV_o}{dt} + \frac{V_o}{R_f} \right]$$

Apply Laplace Transform

$$\frac{V_{in}(s)}{R_1} = -s C_f V_o(s) - \frac{V_o(s)}{R_f}$$

$$\begin{aligned} \frac{V_{in}(s)}{R_1} &= -V_o(s) \left[s C_f + \frac{1}{R_f} \right] \\ &= \frac{-V_o(s) (s C_f R_f + 1)}{R_f} \end{aligned}$$

$$V_o(s) = \frac{-V_{in}(s) \cdot R_f}{R_1 [s C_f R_f + 1]}$$

$$V_o(s) = \frac{-1}{\left[s R_1 C_f + \frac{R_1}{R_f} \right]} V_{in}(s)$$

if $R_f \gg R_1$ then neglect $\frac{R_1}{R_f}$

it acts as integrator

$$V_o(s) = \frac{-1}{s R_1 C_f} V_{in}(s)$$

$$V_o(t) = \frac{-1}{R_1 C_f} \int V_{in}(t) dt$$

Frequency Response :-

$$\frac{V_o(s)}{V_{in}(s)} = \frac{-R_f/R_1}{1 + s C_f R_f}$$

$$s = j\omega$$

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-R_f/R_1}{1 + j\omega C_f R_f}$$

$$A = \frac{-R_f/R_1}{1 + j 2\pi f C_f R_f}$$

$$\text{Let } f_a = \frac{1}{2\pi C_f R_f}$$

$$|A| = \frac{R_f/R_1}{\sqrt{1 + (f/f_a)^2}}$$

Applications of Practical Integrator:

- ① Analog computers
- ② Solving differential Equations.
- ③ Analog to Digital converters.
- ④ various signal wave shaping circuits.
- ⑤ Ramp Generators.

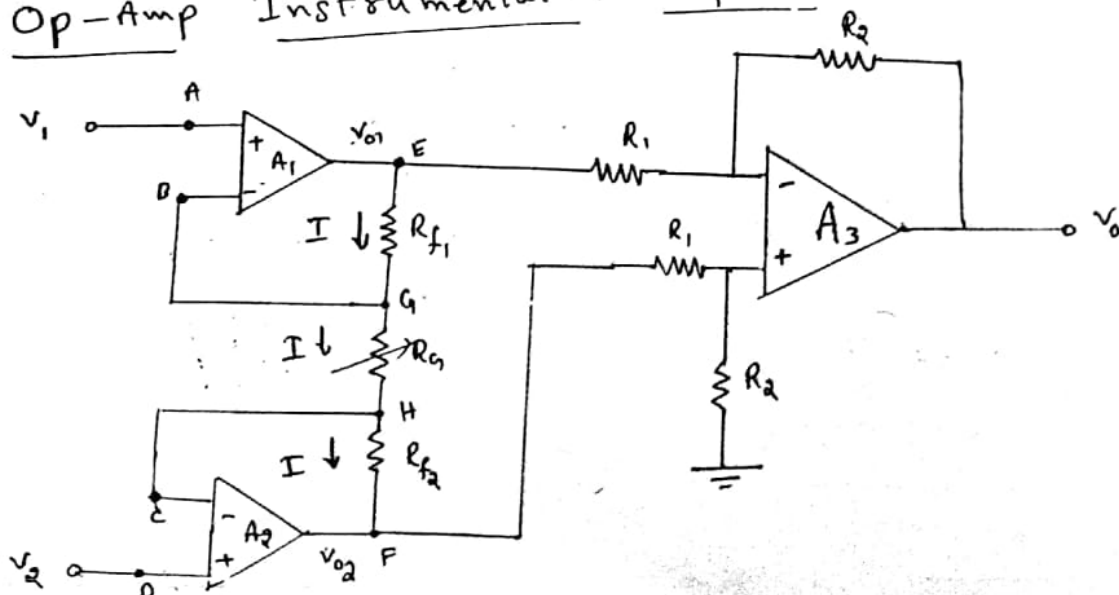
* Instrumentation Amplifier :-

Def:- The special amplifier which is used for such a low level amplification with high CMRR, high i/p impedance to avoid loading, low power consumption and some other features is called an "Instrumentation amplifier".

→ It is an integral part of modern Testing and Measurement instrumentation.

→ This is also called "Data Amplifier" and basically difference amplifier. voltage gain, $A = \frac{V_o}{V_e - V_i}$

Op-Amp Instrumentation Amplifier :-



→ The op-amp's A_1 and A_2 are the non-inverting amp's forming the i/p (or) first stage of instrumentation amp.

→ The op-amp A_3 is normal difference amp forming an o/p stage amplifier.

→ o/p of op-amp A_1 is V_{o1} and o/p of op-amp A_2 is V_{o2} .

→ The node 'A' potential of op-amp A_1 is V_1 form virtual ground the potential of node B is also V_1 & hence potential of G also V_1 .

→ The i/p current of op-amp A_1 and A_2 both are zero. Hence current I remains same through R_{f1} , R_G and R_{f2} .

→ The node D, potential of op-amp A_2 is V_2 Form virtual ground the potential of node C is also V_2 and hence potential of H is also V_2 .

→ The o/p stage is standard basic differential amp. Then the o/p of diff. amp is

$$V_o = \frac{R_2}{R_1} (V_{o2} - V_{o1}) \quad \text{--- (1)}$$

Let us findout expression for $V_{o2} \& V_{o1}$ interms of $V_1 \& V_2$, R_{f1} , R_{f2} & R_G .

Apply Ohm's law b/w nodes E and F. we get from diagram

$$I = \frac{V_{o1} - V_{o2}}{R_{f1} + R_G + R_{f2}}$$

$$\text{but } R_{f1} = R_{f2} = R_f$$

$$I = \frac{V_{o1} - V_{o2}}{2R_f + R_G} \quad \text{--- (2)}$$

From nodes G_1 and 11

$$I = \frac{V_{G_1} - V_{11}}{R_{G_1}} = \frac{V_1 - V_2}{R_{G_1}}$$

$$I = \frac{V_1 - V_2}{R_{G_1}} \quad \text{--- (3)}$$

Equating two eqn's (2) & (3)

$$\frac{V_{O1} - V_{O2}}{2R_f + R_{G_1}} = \frac{V_1 - V_2}{R_{G_1}}$$

$$\frac{V_{O2} - V_{O1}}{2R_f + R_{G_1}} = \frac{V_2 - V_1}{R_{G_1}}$$

$$V_{O2} - V_{O1} = \frac{(2R_f + R_{G_1})(V_2 - V_1)}{R_{G_1}} \quad \text{--- (4)}$$

sub eqn (4) in (1), we get

$$V_O = \frac{R_2}{R_1} \left[\frac{2R_f + R_{G_1}}{R_{G_1}} \right] (V_2 - V_1)$$

$$V_O = \frac{R_2}{R_1} \left[1 + \frac{2R_f}{R_{G_1}} \right] (V_2 - V_1)$$

Advantages:-

- ① With the variable resistance R_{G_1} the gain can be easily varied and all requirements satisfied.

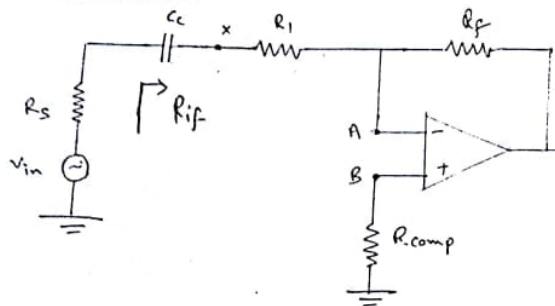
* A.C. amplifier:-

- The op-amp can amplify both the types of signals d.c. & a.c.
- The op-amp responding to a.c. signal is called A.C. amplifier.
- If the A.C. i/p signal is along with some d.c. level, it is necessary to use such an a.c. amplifier with a "coupling capacitor".

→ Two types of A.C. Amplifiers

- ① Inverting A.C. amplifier
- ② Non-inverting " "

① Inverting A.C. Amplifier:-



Gain for inv Amp

$$A = \frac{V_o}{V_i} = -R_f/R_i$$

$$\frac{V_o}{V_i} = \frac{-R_f}{R_i + j\omega C_c} = \frac{-R_f}{R_i(1 + j\omega R_i C_c)}$$

Apply Laplace transform to above

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_f/R_i}{(1 + \frac{1}{sR_i C_c})} = \frac{-R_f/R_i}{1 + \frac{1}{j\omega R_i C_c}}$$

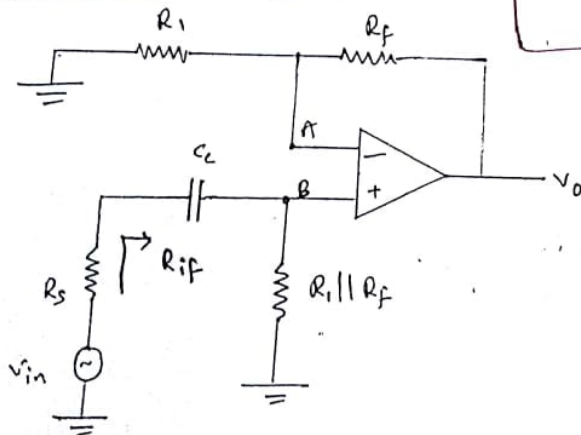
$$= \frac{-R_f/R_i}{1 + \frac{1}{j\omega R_i C_c}} = \frac{-R_f/R_i}{1 + \frac{1}{j\omega R_i C_c}}$$

$$= \frac{-R_f/R_i}{1 - j(f/f_c)}$$

$$f_c = \frac{1}{2\pi R_i C_c (R_s + R_i)}$$

lower cutoff freq

② Non-inverting A.C. Amplifier:-



$$|A| = \frac{|R_f/R_i|}{\sqrt{1 + (f/f_c)^2}}$$

$$A_f = 1 + \frac{R_f}{R_1}$$

* Comparator :-

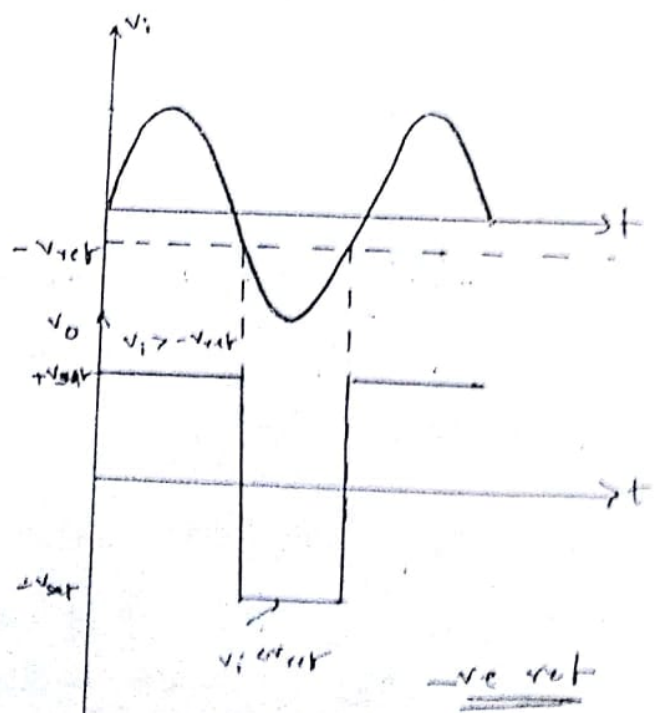
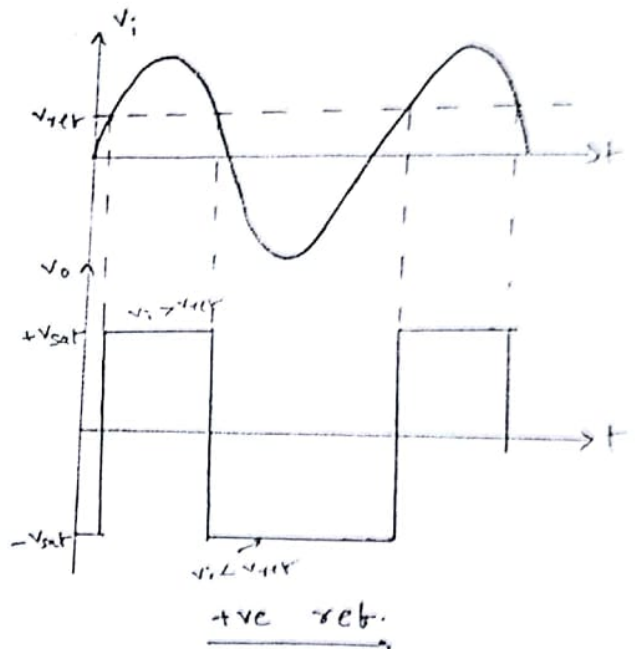
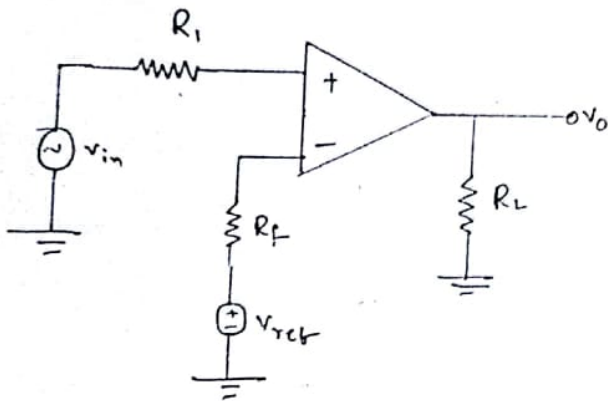
→ A comparator is a ckt which compares a signal voltage applied at one i/p of an op-amp with a known reference voltage at the other i/p.

→ Depending upon the i/p applied comparators are two types

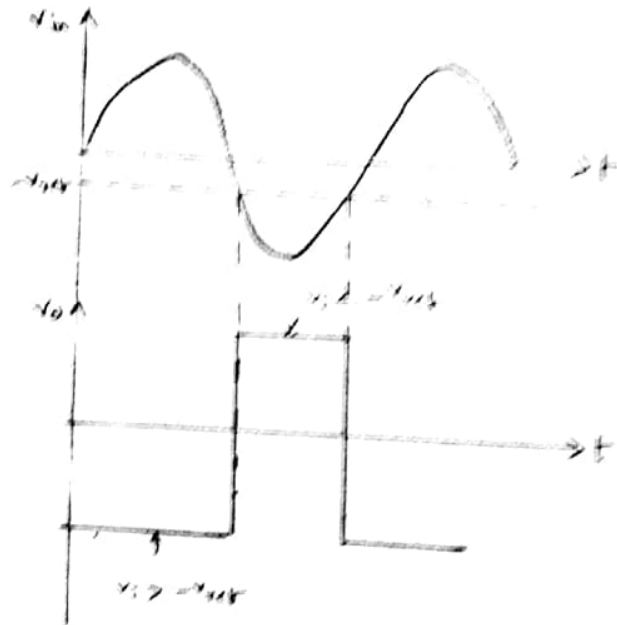
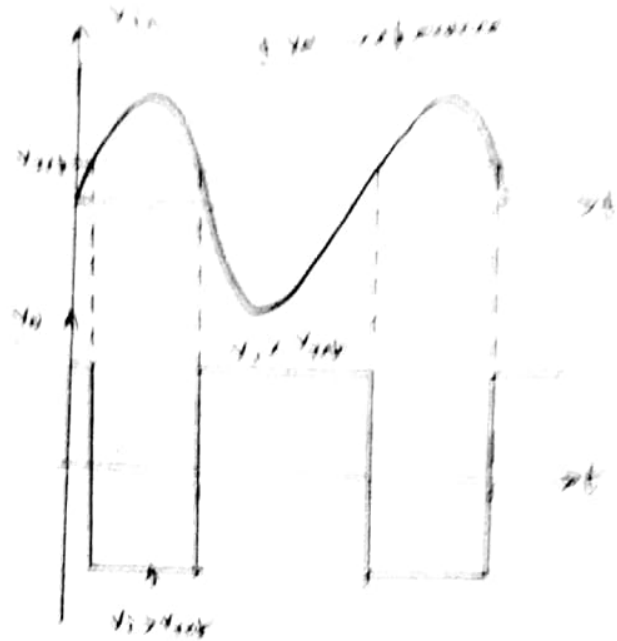
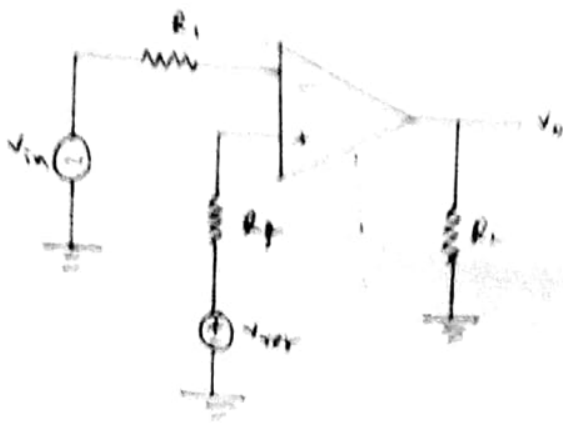
② Inverting comparator

① Non-inverting comparator.

① Non-Inverting comparator :-



(R) Inverting comparator



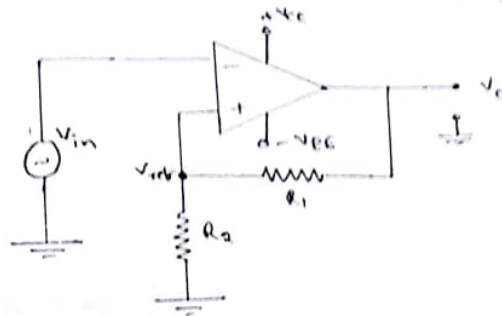
-ve reference

Schmitt Trigger (or) Regenerative Comparator:

- Unwanted noise causes the op to jump b/w high & low states.
- The comparator ckt used to avoid such unwanted triggering is called Regenerative Comparator (or) Schmitt Trigger which basically uses a +ve feedback.

→ When V_{in} is slightly +ve than V_{ref} , then o/p gets driven into -ve saturation $-V_{sat}$ level

→ When V_{in} becomes more -ve than $-V_{ref}$, then o/p gets driven into +ve saturation at $+V_{sat}$ level.

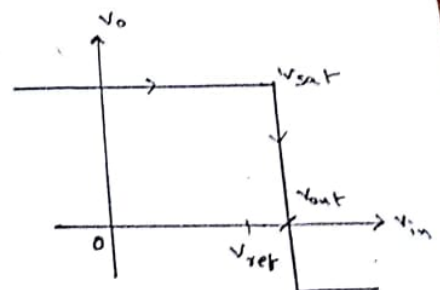


→ Thus o/p voltage is always at $+V_{sat}$ and $-V_{sat}$ but the voltage at which it change its state now can be controlled by the Resistance R_1 and R_2 . Thus V_{ref} can be obtained as per the requirement.

→ Now R_1 and R_2 forms a potential divider & we can write

$$\frac{V_0 = +V_{sat}}{+V_{ref}} = \frac{V_0 \cdot R_2}{R_1 + R_2} = \frac{+V_{sat} \cdot R_2}{R_1 + R_2} \quad (\text{+ve saturation})$$

$$V_{UT} = \frac{+V_{sat} \cdot R_2}{(R_1 + R_2)}$$



where $V_{UT} \rightarrow$ Upper Threshold Voltage

$$V_{in} > V_{UT} = +V_{sat}$$

$$V_{in} < V_{UT} = -V_{sat}$$

$$V_0 = -V_{sat}$$

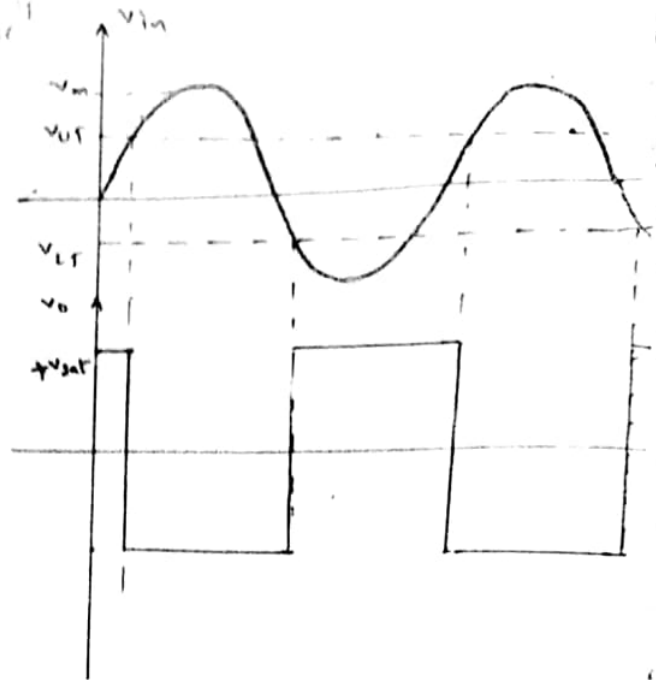
$$V_{LT} = \frac{-V_{sat} \cdot R_2}{(R_1 + R_2)}$$

Hysteresis (or) Dead Band (or) dead zone

$$H = V_{UT} - V_{LT}$$

$$= \frac{+V_{sat} \cdot R_2}{(R_1 + R_2)} - \left(\frac{-V_{sat} \cdot R_2}{R_1 + R_2} \right)$$

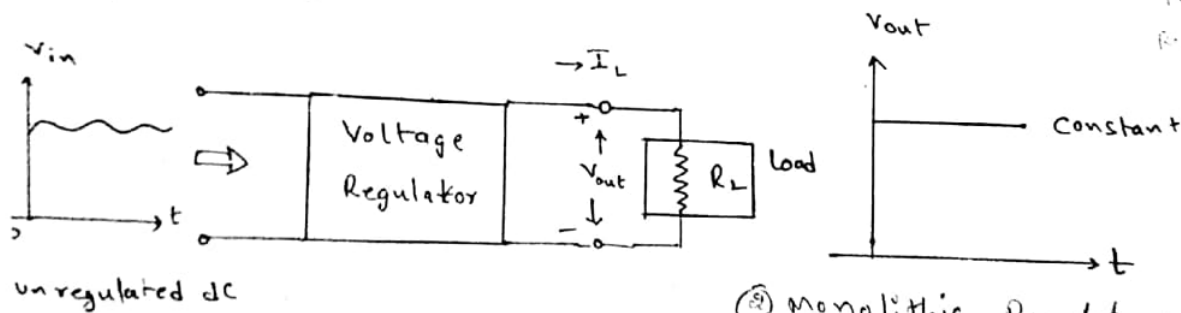
$$H = \frac{2 V_{sat} \cdot R_2}{R_1 + R_2}$$



* Introduction to voltage Regulator :-

→ The voltage regulator circuit keeps the output voltage constant inspite of changes in the load current (or) input voltage.

IC Voltage Regulator 723



② Monolithic Regulators are 78xx/79xx Series.

* Features of 723 Regulator :-

- 1) It works as voltage Regulator at o/p voltage ranging from 2 to 37 volts at currents upto 150mA.
- 2) It can be used at load currents greater than 150mA with use of suitable NPN or PNP external pass transistors.

- ③ Input and output short-circuit protection is provided.
- ④ It has good line and load regulation (0.03%)
- ⑤ Wide variety of applications of series, shunt, switching and floating regulator.
- ⑥ Low standby current drain.
- ⑦ Low temperature drift and high ripple rejection.
- ⑧ Small size, lower cost.
- ⑨ Relative ease with which power supply can be designed.
- ⑩ It provides a choice of supply voltage.

* Three Terminal Voltage Regulator:-

→ 78XX series are three terminal, +ve fixed voltage Regulator.

There are seven o/p voltage options available such as 5, 6, 8, 12, 15, 18 and 24V.

→ In 78XX, the last two numbers (XX) indicate the o/p voltage.

Eg:- 7815 represents a 15V regulator.

→ 79XX^{min} is also available with same features and extra (-ve voltage) two features. there are two extra voltage options -2V & -5.2V

UNIT-II (Op-Amp, IC-555 & IC 565 Applications)

- ① Introduction to Active filters
- ② characteristics of Band pass, Band reject & All pass filter.
- ③ Analysis of 1st order LPF & HPF Butterworth "
- ④ Wave^{form} Generators
 - Triangular wave
 - Sawtooth "
 - Square "
- ⑤ IC 555 Timer - Functional Diagram
- ⑥ Monostable and Astable operations
Applications
- ⑦ IC 565 PLL
 - Block Schematic
 - Description of Individual Blocks
 - Applications.

Op-Amp, IC-555 & IC 565 Applications

* Introduction to Active Filters:-

Filter:- A filter is a ckt that is designed to pass a specified band of frequencies while attenuating all the signals outside that band. It is a freq. selective ckt.

- Electric filters are used in circuits which require the separation of signals according to their frequencies,
- Filters are widely used in communication and signal processing and in one form (or) another in almost all sophisticated electronic instruments.

classification of Filters :-

- ① Analog or Digital Filter
- ② Passive or Active
- ③ Audio Frequency (AF) or Radio Frequency (RF)

① Analog (or) Digital Filter :-

Analog filters are designed to process analog signals, while digital filters process analog signals using digital techniques.

② Passive or Active filter

Depending on the type of elements used in their construction filters may be classified as passive or active.

Passive ^{filter} elements $\xrightarrow{\text{used}}$ Resistor, capacitor & Inductor

Active filter $\longrightarrow$ op-amp, Resistor & capacitor

$\rightarrow$ In active filters, Inductor not used because bulky, heavy, it generates magnetic fields.

③ Audio Frequency (AF) or Radio Frequency (RF) :-

Depending upon frequency Range.

$\rightarrow$ Audio frequency filters are also known as low freq. filters.

This type of filters uses R & C.

$\rightarrow$ Radiofrequency filters are also known as High freq. filters.

This type of filters uses I & C, (or) crystal.

Practical Filters (Active Filter) :-

The practical filters are classified into diff. types based on the range of freq they allow to pass without any attenuation.

① Low Pass Filter (LPF)

② High Pass Filter (HPF)

③ Band Pass Filter (BPF)

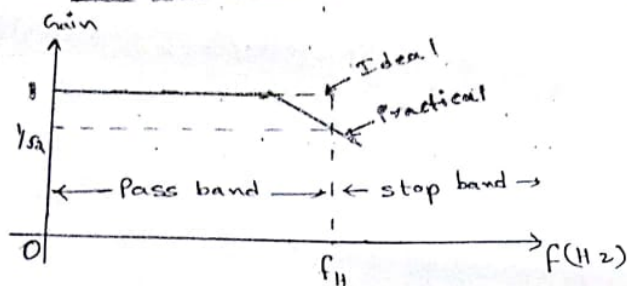
④ Band elimination filter (or) Band stop Filter (BSF) or Band Rejected filter

⑤ All Pass Filters

(2)

* Characteristics of Filters :-

① Low Pass Filter (LPF) :-

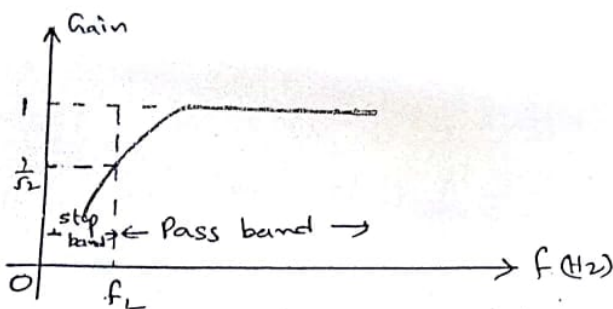


→ A LPF passes the freq's from 0 to f_H i.e., gain constant and it blocks (or) attenuates the freq's above f_H (The freq response of LPF)

Ideal and Practical

$0 < f < f_H \rightarrow$ Pass band
 $f > f_H \rightarrow$ stop band

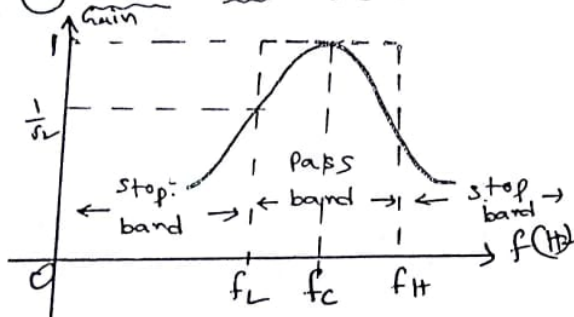
② High Pass Filter (HPF) :-



→ A HPF passes the freq's above f_L and attenuates all freq's below f_L .

$0 < f < f_L \rightarrow$ stop band
 $f > f_L \rightarrow$ Pass band

③ Band Pass Filters (BPF) :-

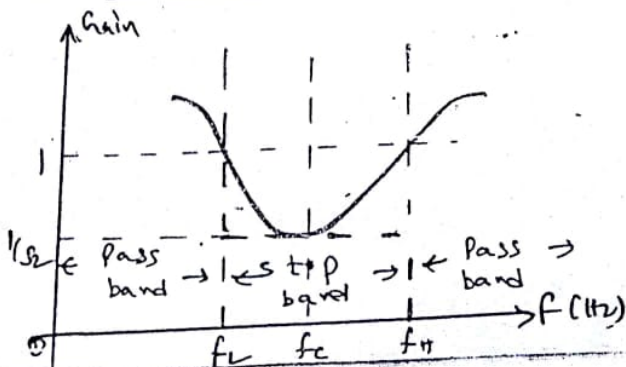


→ A filter which passes freq's from f_L to f_H and attenuates all other freq's known as BPF.

→ It has two stop bands & one Pass band i.e., b/w f_L & f_H .

$0 < f < f_L$ and $f_H < f < \infty \rightarrow$ stop band
 $f_L < f < f_H \rightarrow$ pass band

④ Band stop Filters or Band Rejected Filter (BRF) or Band eliminate Filter or Notch filter



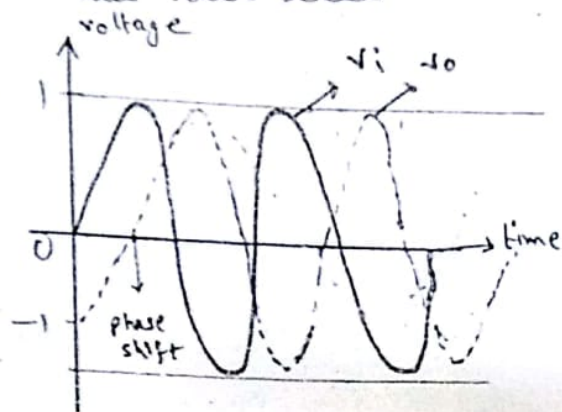
→ This filter

when $f = f_c$

operation is exact opposite to the operation of BPF. It has Two pass bands & one stop band.

$0 < f < f_L$ & $f_H < f < \infty \rightarrow$ Pass band
 $f_L < f < f_H \rightarrow$ stop band.

⑤ All Pass Filters :-



→ The all pass filter pass all the freq's but it produces the phase shift b/w i/p & o/p.

→ The i/p & o/p voltages equal in Amplitude for all freq but with the phase shift b/w the two.

→ The freq upto which the i/p & o/p amplitude remains same is decide by the Unity Gain Bandwidth (UGB) of op-amp Used.

Butterworth Approximation :-

The filter in which denominator polynomial of its transfer function is a Butterworth polynomial is called Butterworth filter.

* First Order Low Pass Butterworth Filter :-

→ The first order LPF is realised by RC ckt. Used along with an op-amp. used in non-inverting configuration.

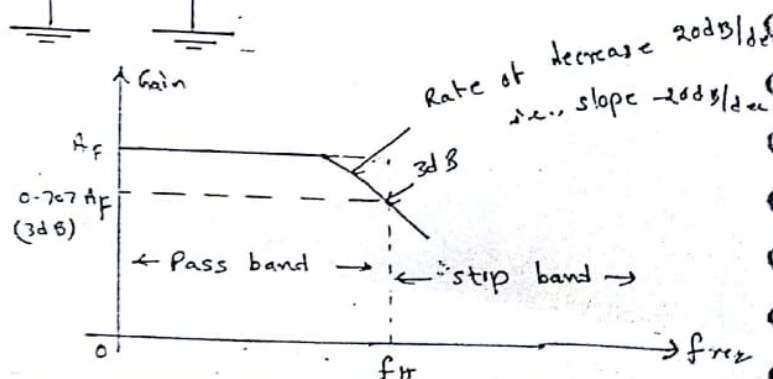
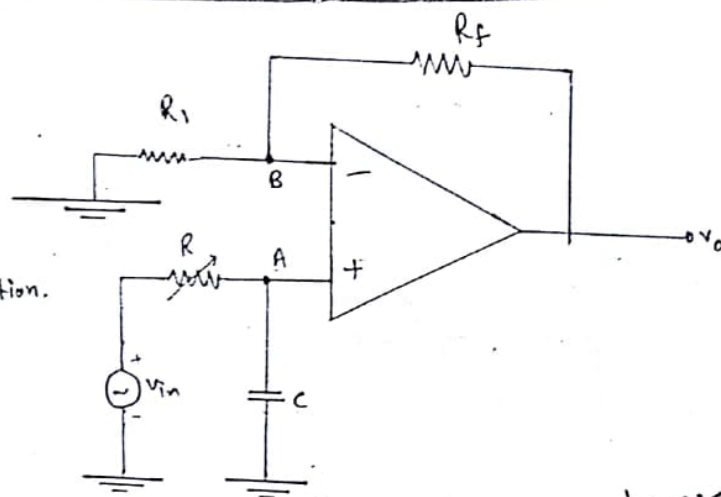
→ This is also called one pole LPF.

→ The resistances R_f and R_1 decide the gain of filter in pass band.

$f < f_H \rightarrow$ Gain const.

$f = f_H \rightarrow 3dB$

$f > f_H \rightarrow$ decrease



Analysis:- The impedance of the capacitor C is $-jX_c$ where X_c is the capacitive reactance given by

$$X_c = \frac{1}{2\pi fC} \quad \text{--- (1)}$$

By the potential divider rule, the voltage at the non-inverting i/p terminal 'A' which is voltage across capacitor

$$V_A = \frac{-jX_c}{R - jX_c} \cdot V_{in}$$

$$= \frac{\frac{-j}{2\pi fC}}{R - \frac{j}{2\pi fC}} \cdot V_{in} \quad [\because \text{from (1)}]$$

$$= \frac{-j}{2\pi fRC - j} \cdot V_{in}$$

$$= \frac{V_{in}}{1 - \frac{2\pi fRC}{j}}$$

But $-j = \frac{1}{j}$ and $\frac{-1}{j} = j$

$$V_A = \frac{V_{in}}{1 + j2\pi fRC} \quad \text{--- (2)}$$

V_{in} is applied at non-inverting terminal then i.e.,
Non-inverting op-amp o/p voltage.

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_A$$

$$= \left(1 + \frac{R_f}{R_i}\right) \frac{V_{in}}{1 + j2\pi fRC} \quad [\because \text{from ②}]$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{A_F}{1 + j(f/f_H)}} \rightarrow \text{This is Transfer fun of filter.}$$

where $A_F \rightarrow 1 + \frac{R_f}{R_i} = \text{Gain of filter in pass band}$

$$f_H \rightarrow \frac{1}{2\pi RC}$$

$f \rightarrow \text{Operating frequency}$

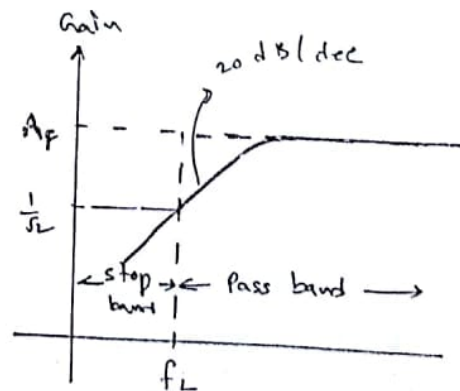
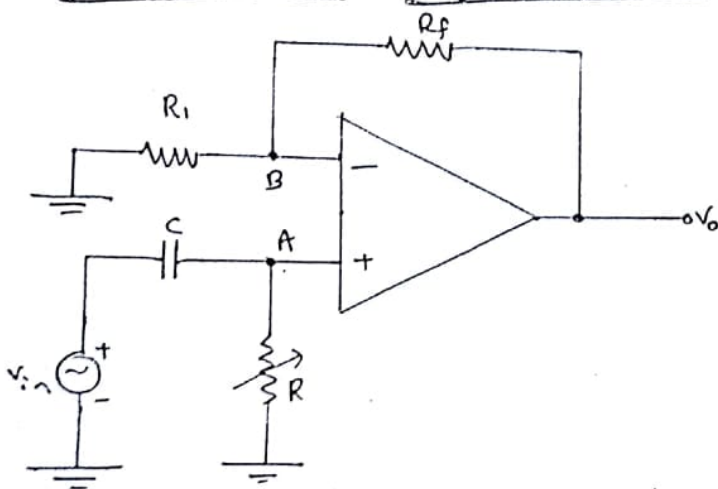
Magnitude :

$$\boxed{\left| \frac{V_o}{V_{in}} \right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}}}$$

Phase angle :-

$$\boxed{\phi = -\tan^{-1}(f/f_H)}$$

First order High Pass Butterworth Filter :-



→ A HPF is a ckt that attenuates all the signals below a specified cut-off frequency denoted as f_c .

→ A HPF ckt can be obtained by interchanging freq. determining resistor and capacitor in LPF ckt.

→ The freq's greater than f_c are allowed to pass but the maximum freq which is allowed to pass is determined by the closed loop bandwidth of op-amp.

Analysis:-

→ Impedance of capacitor is $-jX_c = -j\left(\frac{1}{2\pi f_c}\right)$ where f is i/p operating freq.

→ Apply voltage divider Rule at non-inverting terminal of op-amp

$$V_A = V_{in} \left[\frac{R}{R - jX_c} \right]$$

$$= V_{in} \left[\frac{R}{jX_c \left(\frac{R}{-jX_c} + 1 \right)} \right]$$

But $-\frac{1}{j} = j \Rightarrow \frac{1}{-jX_c} = \frac{j}{X_c} = \frac{j}{\left(\frac{1}{2\pi f_c}\right)} = j2\pi f_c$

$$V_A = V_{in} \left[\frac{-R/jX_c}{(-R/jX_c) + 1} \right]$$

$$V_A = V_{in} \left[\frac{j2\pi f_c R}{1 + j2\pi f_c R} \right]$$

$$V_A = V_{in} \left[\frac{j(f/f_c)}{1 + j(f/f_c)} \right]$$

where $f_c = \frac{1}{2\pi RC}$
cut-off freq

V_{in} is applied at non-inverting terminal then i.e., non-inverting op-amp o/p voltage is

$$V_o = A_F \cdot V_{in}$$

$$= A_F \cdot V_{in} \left[\frac{j(f/f_c)}{1+j(f/f_c)} \right]$$

$$\boxed{\frac{V_o}{V_{in}} = A_F \left[\frac{j(f/f_c)}{1+j(f/f_c)} \right]}$$
 $\rightarrow$ This is Transfer function of filter.

magnitude:

$$\left| \frac{V_o}{V_i} \right| = \frac{A_F \cdot f/f_c}{\sqrt{1 + (f/f_c)^2}}$$

* Waveform Generators :- ① Triangular Rectangular Wave Generator

$\rightarrow$ The o/p of an integrator is triangular if its i/p is square wave i/p. While o/p of a schmitt trigger is -square wave for any i/p.

$\rightarrow$ Thus if o/p of schmitt trigger is applied to i/p of integrator & o/p of integrator as i/p to schmitt trigger then the ckt works as a triangular/Rectangular wave generator.

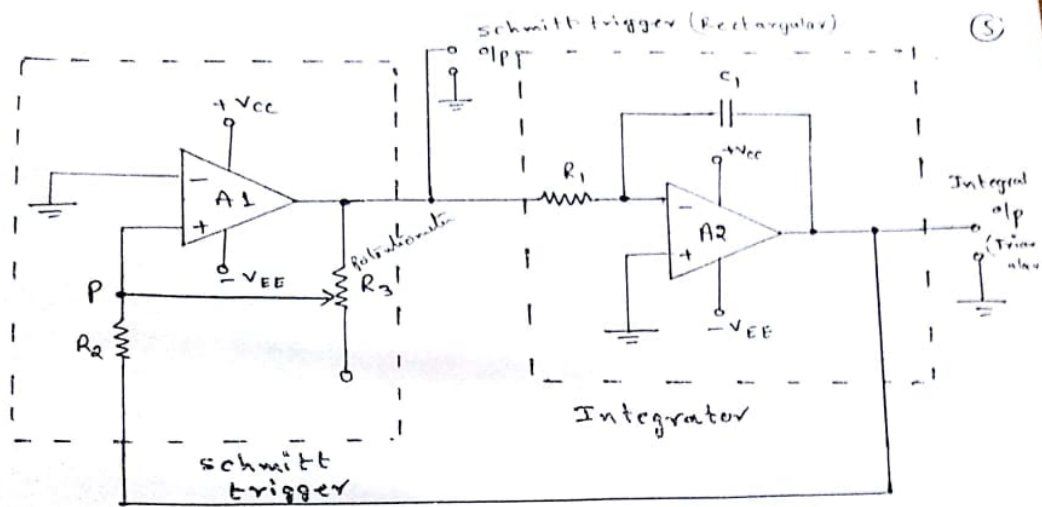
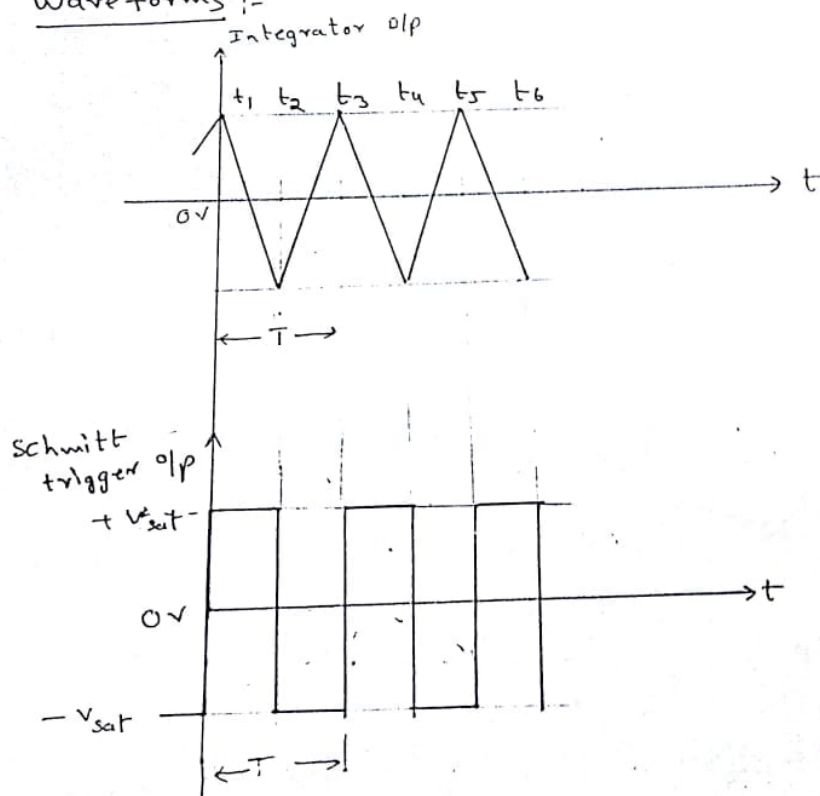


Fig. Triangular/Rectangular Wave Generator

Waveforms :-



→ The ckt acts as free running waveform generator producing triangular and rectangular o/p waveforms.

Frequency and Amplitude Determination

When schmitt trigger op is at $+V_{sat}$, the effective voltage at point P shown in the circuit diagram is given by

$$-V_{ramp} + \frac{R_2}{R_2 + R_3} [+V_{sat} - (-V_{ramp})]$$

When effective voltage at P becomes equal to zero, we can write above eqn as

$$-V_{ramp} + \frac{R_2}{R_2 + R_3} [+V_{sat} - (-V_{ramp})] = 0$$

$$-V_{ramp} + \frac{R_2}{R_2 + R_3} (V_{ramp}) + \frac{R_2}{R_2 + R_3} (+V_{sat}) = 0$$

$$\left[\frac{-(R_2 + R_3) + R_2}{R_2 + R_3} \right] V_{ramp} = - \frac{R_2}{R_2 + R_3} (+V_{sat})$$

$$- \frac{R_3}{R_2 + R_3} V_{ramp} = - \frac{R_2}{R_2 + R_3} (+V_{sat})$$

$$-V_{ramp} = - \frac{R_2}{R_3} (+V_{sat})$$

||¹/₂, when schmitt trigger op is at $-V_{sat}$, we can write

$$V_{ramp} = - \frac{R_2}{R_3} (-V_{sat})$$

The peak to peak amplitude of the triangular wave can be given as

$$V_{o(pp)} = +V_{ramp} - (-V_{ramp}) \quad (6)$$

$$= \frac{-R_2}{R_3} (-V_{sat}) - \frac{-R_2}{R_3} (+V_{sat})$$

If $|+V_{sat}| = |-V_{sat}|$ then, we can write

$$V_{o(pp)} = \frac{R_2}{R_3} V_{sat} + \frac{R_2}{R_3} V_{sat}$$

$$= \frac{2R_2}{R_3} V_{sat}$$

The time taken by the op to swing from $-V_{ramp}$ to $+V_{ramp}$ (or) $+V_{ramp}$ to $-V_{ramp}$ is equal to half the time period $T/2$. This time can be calculated from the integrator op eqn as follows:

$$V_{o(pp)} = \frac{-1}{R_1 C_1} \int_0^{T/2} (-V_{sat}) dt$$

$$= \left(\frac{V_{sat}}{R_1 C_1} \right) \frac{T}{2}$$

$$T = \frac{2 R_1 C_1 V_{o(pp)}}{V_{sat}}$$

Substituting value of $V_{o(pp)}$, we get

$$T = \frac{2 R_1 C_1 \left(\frac{2R_2}{R_3} V_{sat} \right)}{V_{sat}}$$

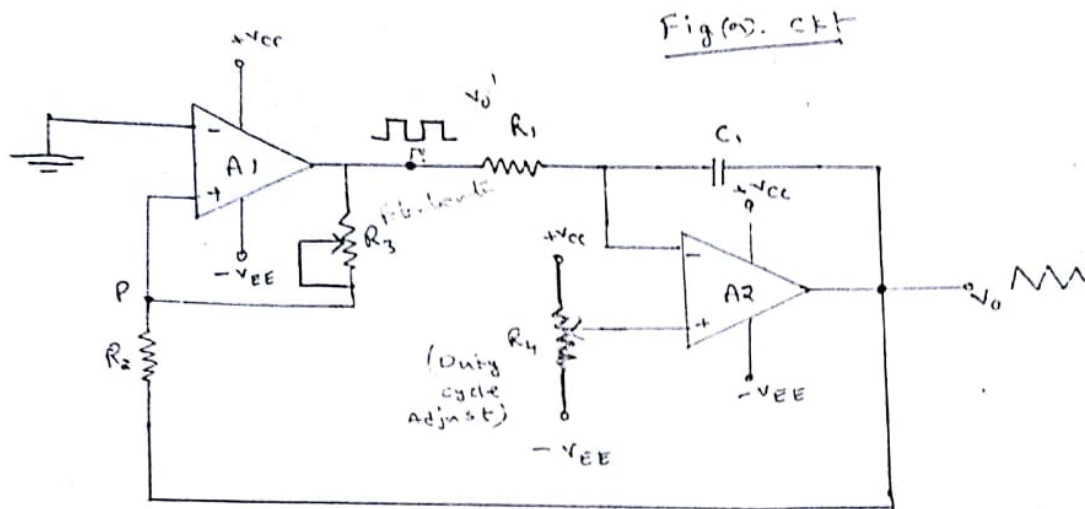
$$= \frac{4 R_1 C_1 R_2}{R_3}$$

Therefore, the freq. of oscillation can be given as,

$$f_0 = \frac{1}{T}$$

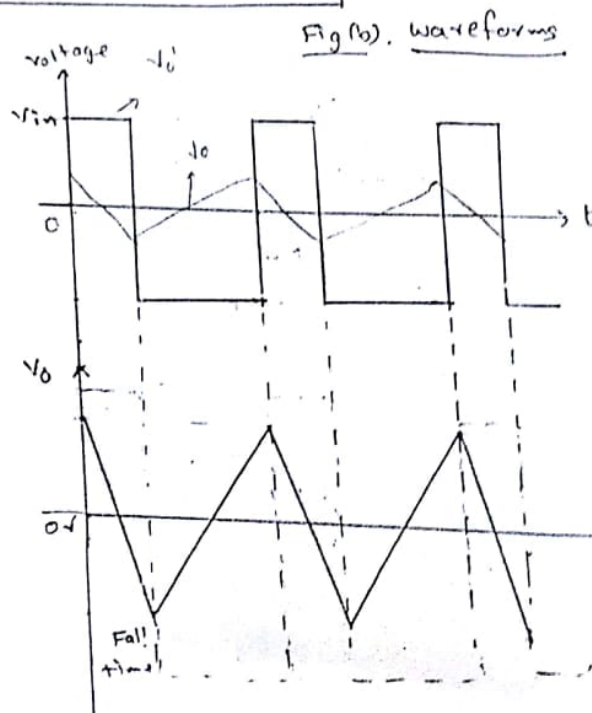
$$\therefore f_0 = \frac{R_3}{4R_1C_1R_2}$$

② Sawtooth Wave Generator:-



→ The difference b/w the triangular and sawtooth waveforms is that the rise time of the triangular wave is always equal to its fall time.

i.e., The same amount of time is required for the triangular wave to swing from $-V_{ramp}$ to $+V_{ramp}$ as from $+V_{ramp}$ to $-V_{ramp}$.



→ The sawtooth waveform has unequal rise and fall times. (1)
That is, it may rise positively many times faster than it falls negatively, or vice versa.

→ The triangular wave generator of Fig. a. can be converted into a sawtooth wave generator by injecting a variable d.c. voltage into the non-inverting terminal of the integrator A_2 .

→ This can be accomplished by using the potentiometer and connecting it to the V_{CC} and $-V_{EE}$ as shown in Fig. a.

→ Depending on the R_4 setting, a certain d.c. level is inserted in the output of A_2 .

→ Now, suppose that the output of A_1 is a square wave and the potentiometer R_4 is adjusted for a certain d.c. level.

→ This means that the output of A_2 will be a triangular wave, riding on some d.c. level that is a function of the R_4 setting.

→ The duty cycle of the square wave will be determined by the polarity and amplitude of this d.c. level.

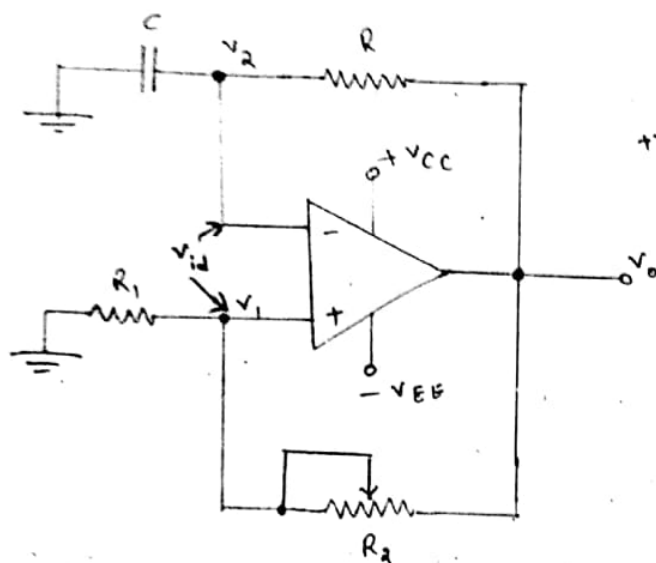
→ A duty cycle less than 50% will ^{if} (then) cause the output of A_2 to be a sawtooth. (see Fig. b).

→ With the wiper at the center of R_4 , the output of A_2 is a triangular wave.

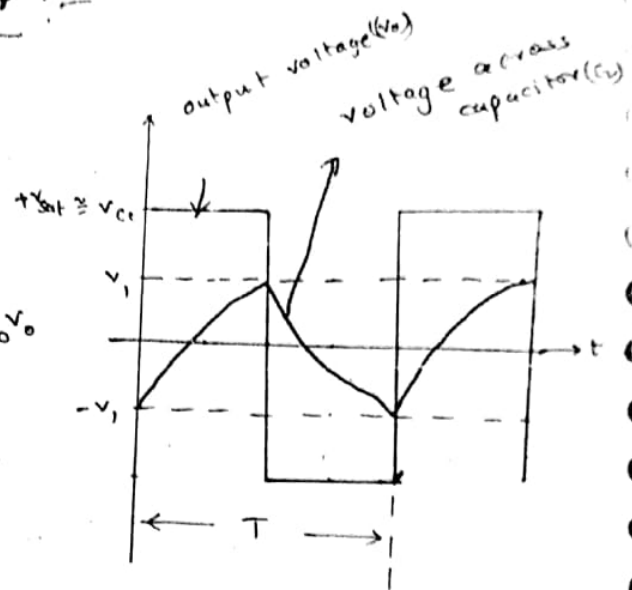
→ For any other position of R_4 wiper, the output is a sawtooth waveforms.

- Specifically as the R_4 wiper is moved toward $-V_{EE}$, the rise time of the sawtooth wave becomes longer than the fall time. (as in Fig b).
- On the other hand, as the wiper is moved toward $+V_{CC}$, the fall time becomes longer than the rise time.
- Also, the frequency of the sawtooth wave decreases as R_4 is adjusted toward $+V_{CC}$ or $-V_{EE}$.
- However, the amplitude of the sawtooth wave is independent of the R_4 setting.

③ Square Wave Generator :-



Fig(a). ckt diagram



Fig(b). Wave forms

- The difference b/w sine wave oscillators & square wave op's are generated when the op-amp is forced to operate in the saturation region.

→ That is, the output of the op-amp is forced to swing repetitively b/w +ve saturation $+V_{sat} (\approx +V_{cc})$ and -ve saturation $-V_{sat} (\approx -V_{cc})$ resulting in the square-wave output. This square wave generator is called a "free-running" (or) "Astable multivibrator".

→ The o/p of the op-amp in this ckt will be in +ve (or) -ve saturation, depending on whether the differential voltage (V_{id}) is -ve (or) +ve, respectively.

Assume that the voltage across capacitor C is zero volts at the instant the DC supply voltage $+V_{cc}$ and $-V_{cc}$ are applied. This means that the voltage at the inverting terminal is zero initially.

→ At the same instant, however, the voltage V_i at the noninverting terminal is a very small finite value that is a function of the output offset voltage V_{oot} and the values of R_1 and R_2 resistors.

→ Thus the differential input voltage V_{id} is equal to the voltage V_i at the noninverting terminal. Although very small, voltage V_i will start to drive the op-amp into saturation.

Example: op-amp's o/p at -ve saturation, $-V_{sat}$. The voltage V_i across R_1 is also -ve, since

$$V_i = \frac{R_1}{R_1 + R_2} (-V_{sat})$$

Op-amp's o/p at +ve saturation $+V_{sat}$, the voltage V_1 at the non-inverting i/p is

$$V_1 = \frac{R_1}{R_1 + R_2} (+V_{sat})$$

The time period T of the o/p waveform is given by

$$T = 2RC \ln \left(\frac{2R_1 + R_2}{R_2} \right)$$

$$f_0 = \frac{1}{2RC \ln \left(\frac{2R_1 + R_2}{R_2} \right)} \quad \left[\because f_0 = \frac{1}{T} \right]$$

The above eqn indicates that the freq of the o/p f_0 is not only a fun. of the RC time constant but also of the relationship b/w R_1 and R_2 .

Example:- if $R_2 = 1.16 R_1$, f_0 becomes

$$f_0 = \frac{1}{2RC}$$

IC 555 Timer

Introduction :-

- In most of Industries, operations are scheduled according to specific time requirements.
- In process industry, Raw material is processed in different stages in each stage, Raw material is processed for a particular time period.

Eg:- ① Process may be the heating process and heat may be required to be applied for 5 mins.

② In automatic cameras one snap can be setting proper time period.

- To achieve such Timing Requirements, the IC555 is popularly used to build the timing circuits.

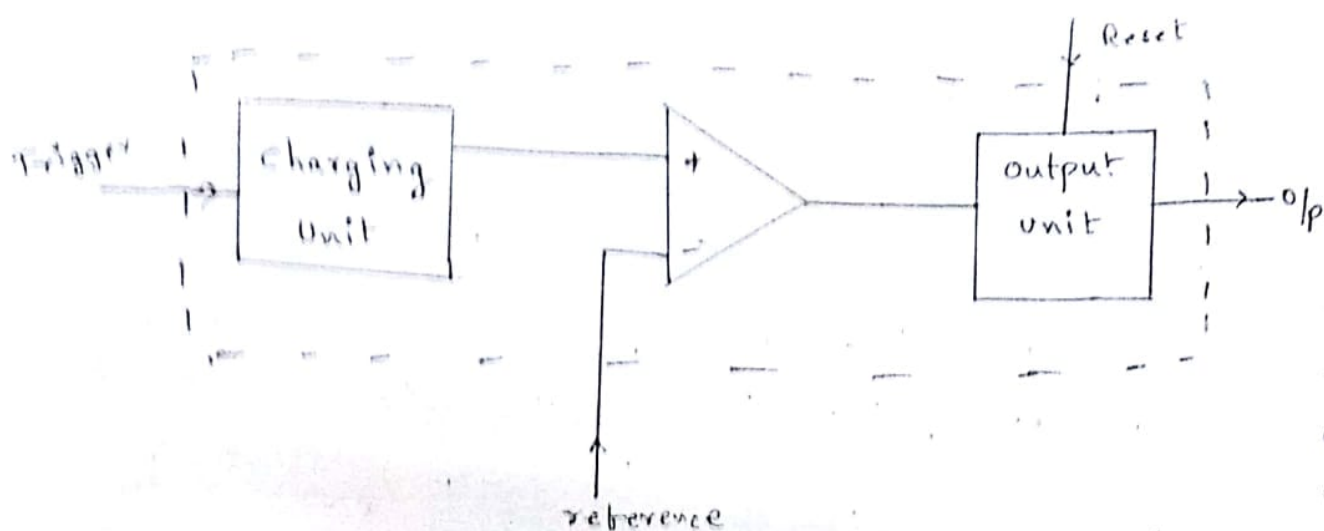
Time Constant :-

Time required by the capacitor voltage to rise from 0 to 0.63 of its final steady state value during charging.

Block Diagram of Timer :-

It consists of 3 i/p signals, 1 o/p signal and 3 units

- ① charging unit
- ② comparator
- ③ o/p unit.



Working principle:-

It can be observed that o/p remains high for time which is required by the capacitor to charge upto control voltage, through R. Thus by varying R or C, the o/p pulse width can be varied. This is working principle of timer IC 555

IC 555 Timer :-

→ IC 555 Timer is a highly stable device, for generating accurate time delay (or) oscillation.

→ IC 555 Timer is most versatile linear integrated device introduced by signetics corporation in 1970
 IC ⁵⁵⁵ (SE555/NE555).

Applications :-

→ It is basically a monolithic Timer circuit which can be used in many applications such as

- ① Monostable multivibrator
- ② Astable multivibrator
- ③ Linear Ramp & square wave Generator
- ④ Missing pulse detector
- ⑤ Pulse Generator
- ⑥ Burglar Alarm
- ⑦ Traffic light control
- ⑧ voltage monitor etc

→ A single 555 timer can provide time delay ranging from microseconds to hours. (10)

→ IC 555 Timer contains the following elements:

- ① A Relaxation Oscillator
- ② R-S Flip-flop
- ③ Two Comparators
- ④ Discharge Transistor.

Pin diagram of IC 555 Timer :-

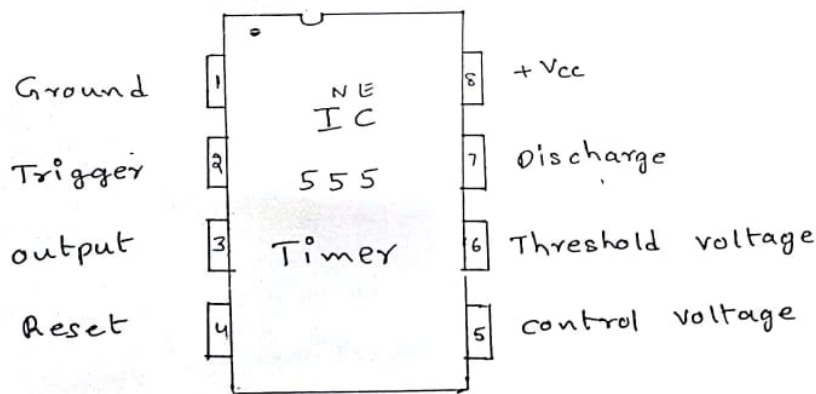


Fig. 8 pin diagram

Description of Functional Diagram :-

→ Three $5\text{ k}\Omega$ internal resistors act as voltage divider, providing bias voltage of $(2/3)V_{cc}$ to the Upper Comparator (U_C) and $(1/3)V_{cc}$ to the Lower Comparator (L_C), where V_{cc} is the supply voltage.

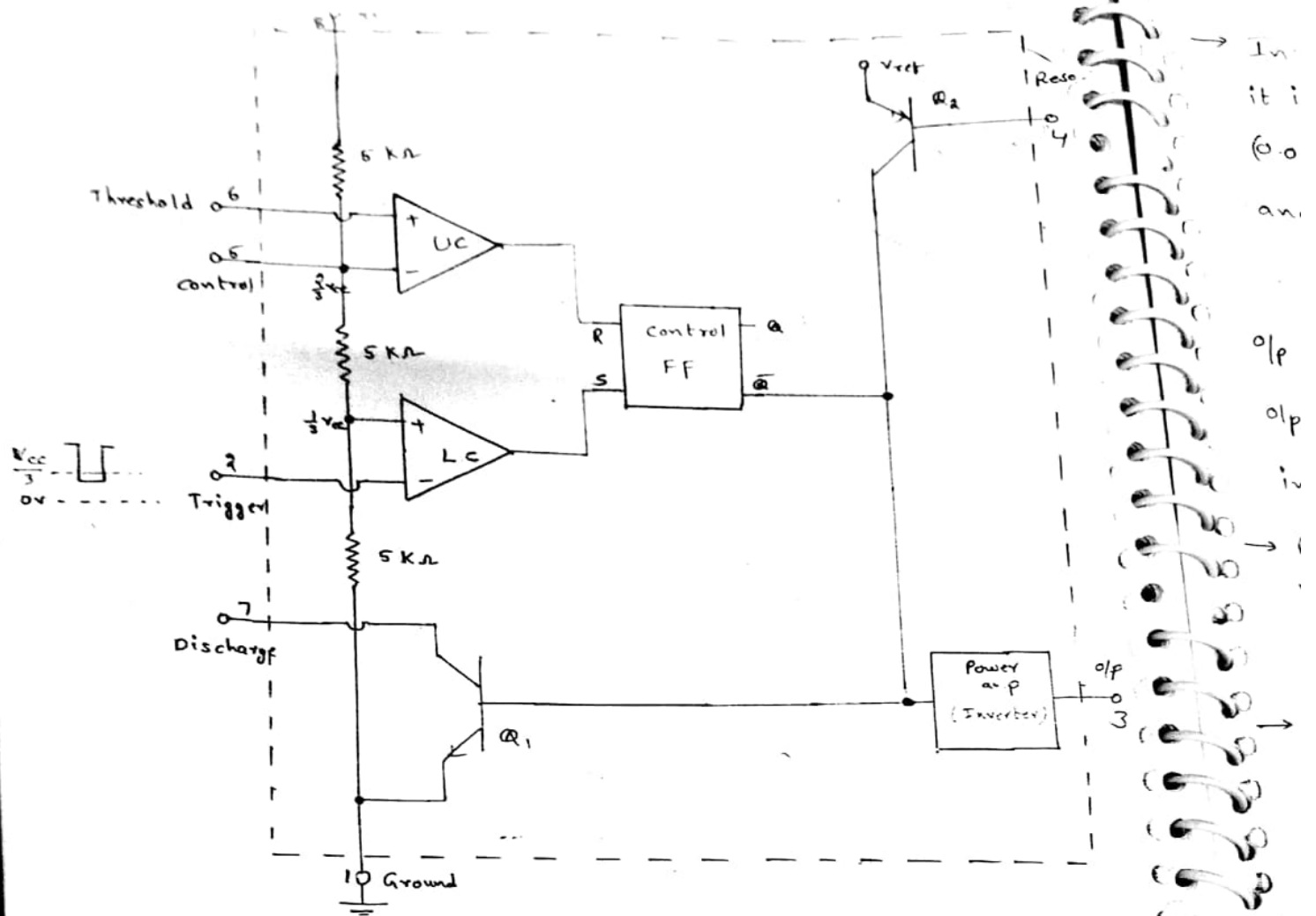


Fig. Functional diagram of 555 Timer

- Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval.
- It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5).

- In applications, where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 μ F) be connected b/w control voltage terminal (pin 5) and ground to by-pass noise (or) ripple from the supply.

In the standby (stable) state, the o/p $\bar{a}$ of the control Flip-Flop (FF) is HIGH. This makes the o/p Low because of power amplifier which is basically an inverter.

- A -ve going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e., $\frac{V_{CC}}{3}$).

- At the -ve going edge of the trigger, as the trigger pulse through ($\frac{V_{CC}}{3}$), the o/p of the lower comparator goes HIGH and sets the FF ($a=1, \bar{a}=0$).

- During the +ve excursion, when the threshold voltage at pin 6 passes through $(2/3)V_{CC}$, the o/p of the upper comparator goes HIGH and resets the FF ($a=0, \bar{a}=1$).

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator.

- This overriding reset is effective when the reset i/p is less than about 0.4V

- When this reset is not used, it is returned to V_{cc} .
- The transistor Q_2 serves as a buffer to isolate the reset input from the FF and transistor Q_1 .
- The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{cc} .
- 555 timer used supply voltage V_{cc} is 5V and V_{ee} is 0V.

Description of Pins Function:-

Pin 1: Ground:

All the voltages are measured w.r.t this terminal.

Pin 2: Trigger:

- The IC 555 uses two comparators. The voltage divider consists of three equal resistances.
- Due to voltage divider, the voltage of non-inverting terminal of comparator 2 is fixed at $V_{cc}/3$.
- The inverting i/p of comparator 2 which compared with $V_{cc}/3$, is nothing but trigger i/p brought out as pin number 2.
- When the trigger i/p is slightly less than $V_{cc}/3$ the comparator 2 o/p goes high. This o/p is given to reset i/p of RS flip-flop. So high o/p of comparator 2 resets the flip-flop.

Pin 3: O_c

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Pin 3: Output:

The complementary signal output ($\bar{Q}$) of the flip-flop goes to pin 3 which is the o/p. The load can be connected in two ways. One b/w pin 3 and Ground while other b/w pin 3 and pin 8.

Pin 4: Reset:

- This is an interrupt to the timing device.
- When pin 4 is grounded, it stops the working of device and makes it off.
- Thus, pin 4 provides on/off features to the IC 555.
- This reset input overrides all other functions within the timer when it is momentarily grounded.

Pin 5: Control Voltage Input:

- In most of the applications, external control voltage i/p is not used.
- This pin is nothing but the inverting i/p terminal of comparator 1.
- The voltage divider holds the voltage of this i/p at $\frac{2}{3}V_{cc}$
- This is reference level for comparator 1 with which threshold is compared.
- If reference level required is other than $\frac{2}{3}V_{cc}$ for comparator 1 then external i/p is to be given to pin 5.

→ If external i/p applied to pin 5 is alternating then the reference level for comparator 1 keeps on changing above and below $\frac{2}{3} V_{CC}$. Due to this, the variable pulse width o/p is possible. This is called pulse width modulation, which is possible due to pin 5.

Pin 6: Threshold:

- This is the non-inverting i/p terminal of comparator 1.
- The external voltage is applied to this pin 6.
- When this voltage is more than $\frac{2}{3} V_{CC}$, the comparator 1 o/p goes high.
- This is given to the set i/p of R-S flip-flop.
- Thus high o/p of comparator 1 sets flip-flop.
- This makes Q of flip-flop high and $\bar{Q}$ low. Thus the o/p of IC 555 at pin 3 goes low.

Remember that o/p at pin 3 is $\bar{Q}$ which is complementary o/p of FF. In short

For threshold $> \frac{2}{3} V_{CC}$, FF $\rightarrow$ Reset $Q \rightarrow$ low, o/p at pin 3 $\rightarrow$ low

For Trigger $< \frac{1}{3} V_{CC}$, FF $\rightarrow$ set, $Q \rightarrow$ high, o/p at pin 3 $\rightarrow$ high

Pin 7: Discharge:

- This pin is connected to the collector of the discharge transistor Q_D .

→ When the o/p is high then Q is low and transistor is off.

→ It acts as an open ckt to the external capacitor C to be connected across it, so capacitor C can charge/as described earlier.

→ When o/p is low, Q is high which drives the base of Q_d high, driving transistor Q_d in saturation.

→ It acts as short ckt, shorting the external capacitor C to be connected across it.

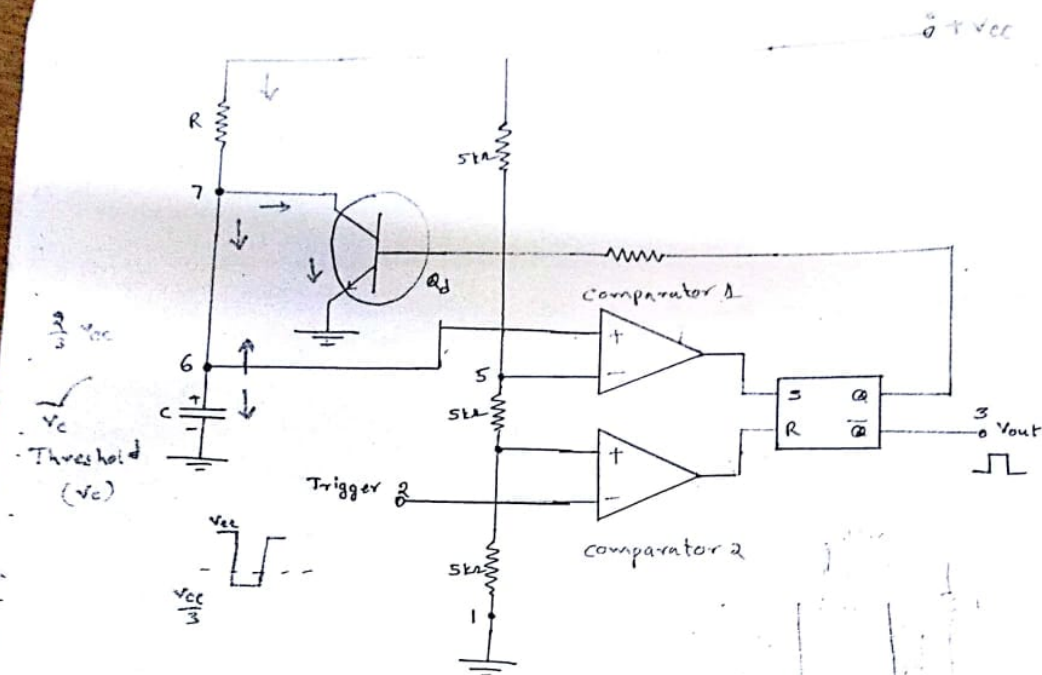
Pin 8: supply $+V_{cc}$:

The IC 555 timer can work with any supply voltage b/w 4.5V and 16V.

* Monostable Operation:—

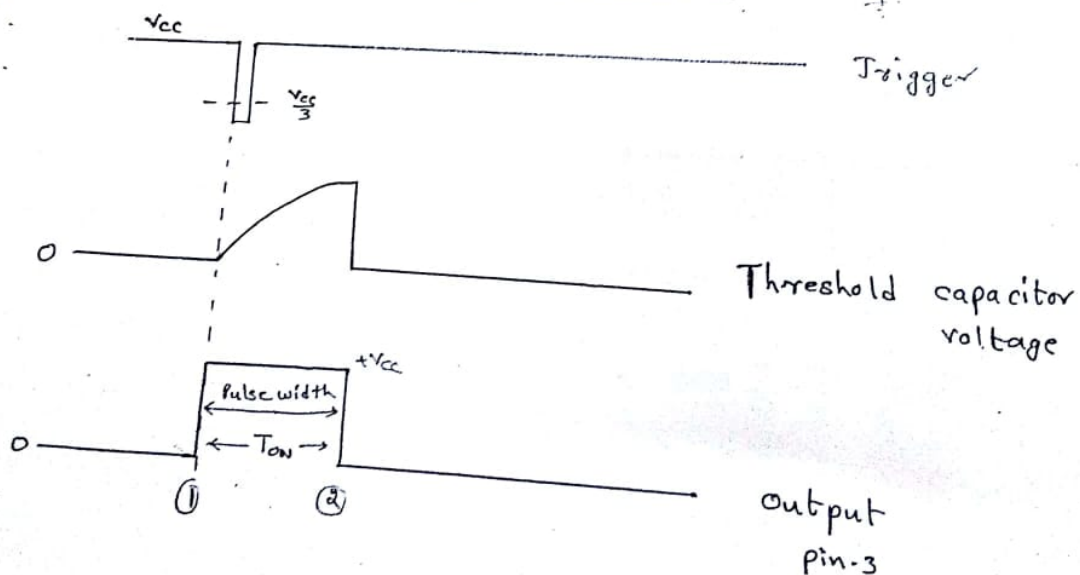
→ The IC 555 timer can be operated as a monostable multivibrator by connecting an external resistor and a capacitor.

→ The ckt has only one stable state. When trigger is applied, it produces a pulse at the o/p and returns back to its stable state. The duration of the pulse depends on the values of R and C . As it has only one stable state, it is called one shot multivibrator.



Fig(a). Monostable operation of 555

Fig(b). Waveforms of monostable operation



NK Nani

Operation :-

The flip-flop is initially set i.e., $\bar{a}$ is high. This drives the transistor Q_1 in saturation. The capacitor discharges completely and voltage across it is nearly zero. The output at pin 3 is low.

When a trigger input, a low going pulse is applied, then circuit state remains unchanged till trigger voltage is greater than $\frac{1}{3}V_{cc}$. When it becomes less than $\frac{1}{3}V_{cc}$, then comparator 2 o/p goes high. This resets the Flip-flop so Q goes low and $\bar{a}$ goes high. Low Q makes the transistor Q_1 off. Hence capacitor starts charging through resistance R (as shown by green color arrows).

The voltage across capacitor increases exponentially. This voltage is nothing but the threshold voltage at pin 6. When this voltage becomes more than $\frac{2}{3}V_{cc}$, then comparator 1 o/p goes high. This sets the flip-flop i.e., Q becomes high and $\bar{a}$ low. This high Q drives the transistor Q_1 in saturation. Thus capacitor C quickly discharges through Q_1 (as shown by red color arrows).

So it can be noted that V_{out} at pin 3 is low at start, when trigger is less than $\frac{1}{3}V_{cc}$ it becomes high and when threshold is greater than $\frac{2}{3}V_{cc}$ again becomes low, till next trigger pulse occurs. So a

rectangular wave is produced at the output. The pulse width of this rectangular pulse is controlled by the charging time of capacitor. This depends on the time constant RC . Thus RC controls the pulse width.

Derivation of Pulse width:-

The voltage across capacitor increases exponentially and is given by,

$$V_c = V_{cc}(1 - e^{-t/CR})$$

If $V_c = \frac{2}{3} V_{cc}$

Then $\frac{2}{3} V_{cc} = V_{cc}(1 - e^{-t/CR})$

$$\frac{2}{3} - 1 = -e^{-t/CR}$$

$$\frac{1}{3} = e^{-t/CR}$$

$$-\frac{t}{CR} = -1.0986$$

$$t = +1.0986 RC$$

$$t \approx 1.1 RC$$

where

$C \rightarrow$ Seconds

$R \rightarrow$ ohms

$t \rightarrow$ seconds

Thus, we can say that voltage across capacitor will reach $\frac{2}{3}V_{CC}$ in approximately 1.1 times, time constant i.e., $1.1RC$.

Thus the pulse width denotes as W is given by

$$W = 1.1RC$$

* Applications of Monostable Multivibrator :-

① Frequency Divider :-

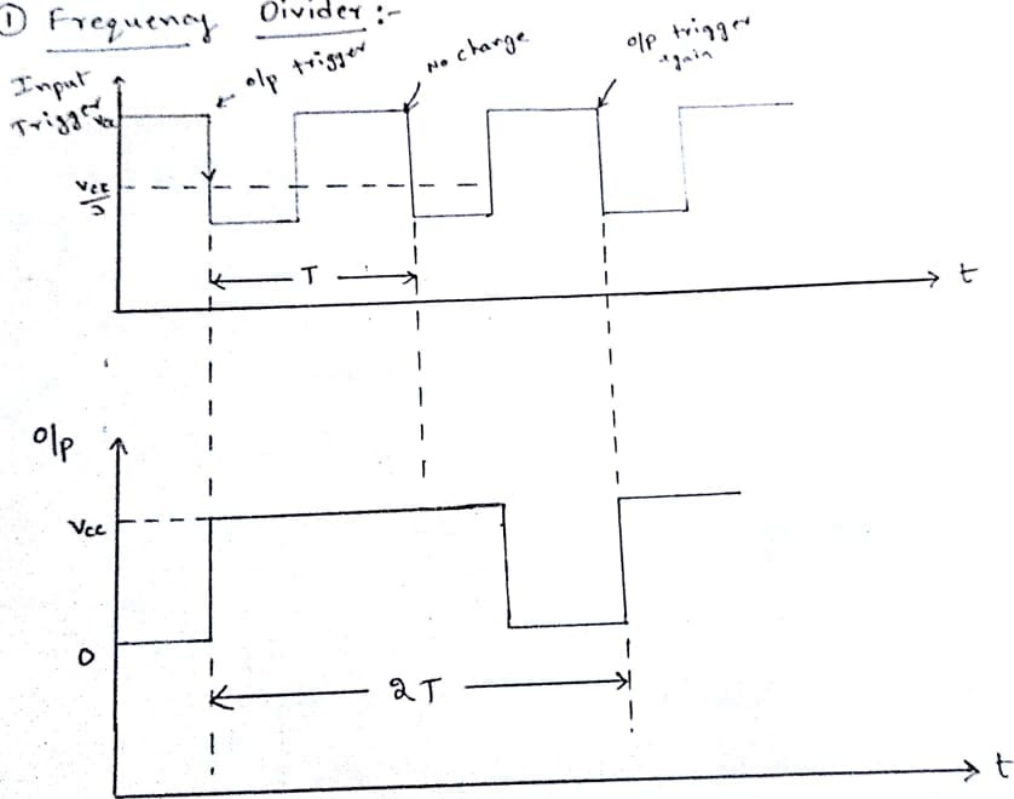


Fig. I/p & o/p waveforms of the Monostable Multivibrator as a divide-by-2 circuit

→ In monostable multivibrator, application of trigger pulse gives a +ve going pulse on the o/p. The same monostable ckt can be used as a frequency divider if the timing interval is adjusted to be longer than the period of the i/p signal.

The monostable multivibrator will be triggered by the first -ve going edge of the trigger i/p, which will make o/p to go in its high state.

→ The o/p will remain high for the period equal to 'timing interval'.

→ As timing interval is greater than time period of the trigger i/p, o/p will still be high when the second -ve going pulse occurs.

→ The monostable will be re-triggered on the third -ve-going pulse. Therefore, monostable triggers on every other pulse of the trigger i/p, so there is only one o/p for every two i/p pulses, thus trigger signal is divider by 2.

→ In this way, by adjusting the timing interval, the monostable ckt can be made integral fractions of the frequency of the i/p trigger signal.

(2) Pulse Width Modulation (PWM) :-

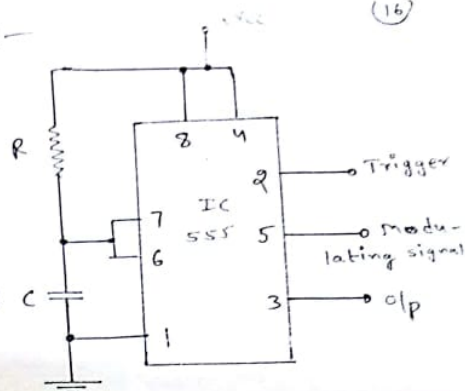
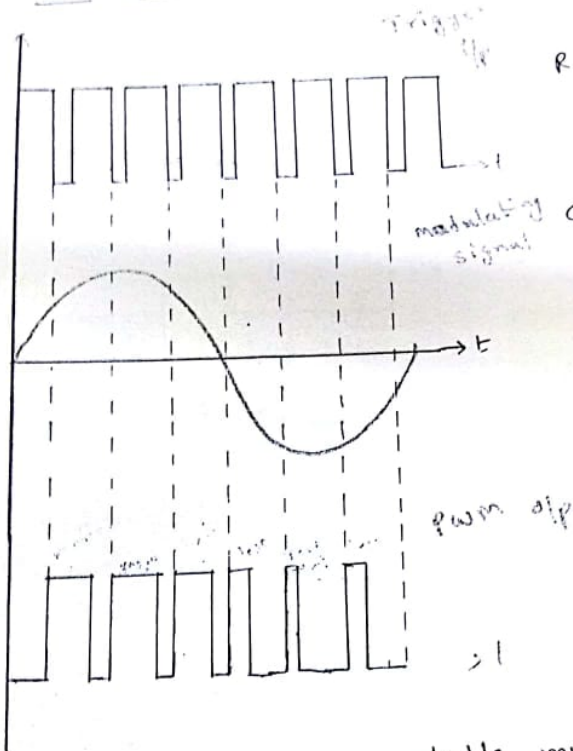
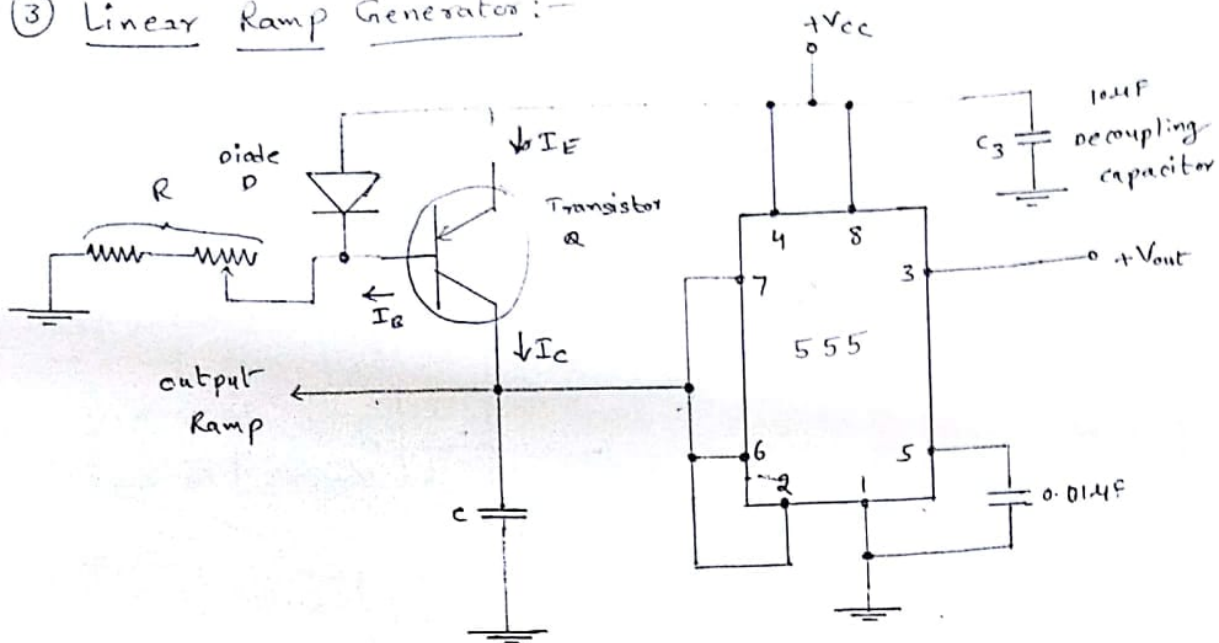


Fig-a. PWM

- It is basically a monostable multivibrator with a modulating i/p signal applied at the control voltage input (pin. 5)
- Internally, the control voltage is adjusted to the $\frac{2}{3} V_{CC}$.
- Externally applied modulating signal changes the control voltage, and hence the threshold voltage level of the Upper Comparator (Comparator 1).
- As a result, time period required to charge the capacitor upto threshold voltage level changes, giving pulse width modulated signal at the o/p.

Note:- The o/p waveform that the pulse duration varies according to the modulating signal level, but the freq. of the o/p pulses is same as that of the trigger i/p signal.

③ Linear Ramp Generator:-

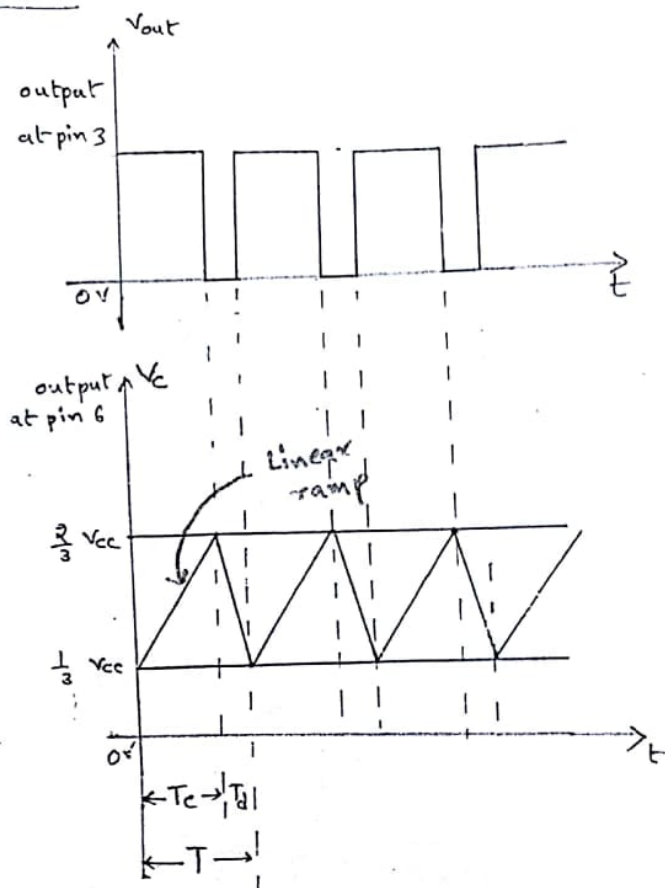


Fig(a) Linear Ramp Generator

→ When a capacitor is charged with a constant current source then linear ramp is obtained.
This concept is used in linear ramp generator.

→ The ckt is used to obtain constant current I_c in a current mirror circuit, using transistor Q and diode D.

→ The current I_c , charges capacitor C at a constant rate towards $+V_{cc}$.



Fig(b). Waveforms of Ramp Generator

→ But when voltage at pin 6 i.e., capacitor voltage V_C becomes $(\frac{2}{3} V_{CC})$, the comparator makes internal transistor Q_1 ON within no time

→ But while discharging when V_C becomes $(\frac{1}{3} V_{CC})$, the second comparator makes Q_1 OFF and C starts its charging again.

→ As discharging time of capacitor C is very small, the time period of ramp is assumed practically same as that of charging time of capacitor.

④ Pulse Position Modulation (PPM): V_{CC}

→ In PPM, the amplitude and width of the pulses are kept constant, while the position of each pulse with reference to the position of a reference pulse, is changed according to the instantaneous sampled value of the modulating signal.

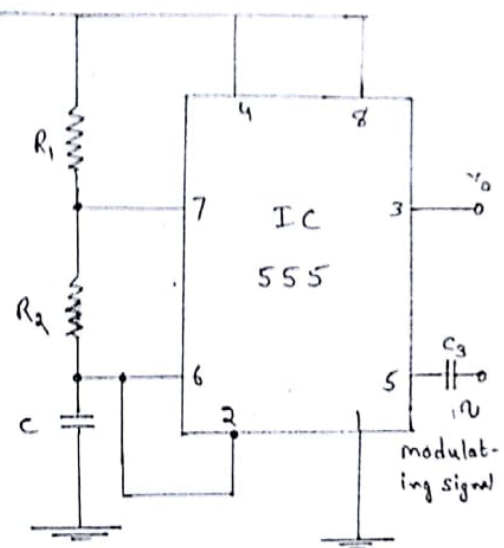


Fig (a). PPM

→ Both width and period of pulses vary with the modulating signal. Due to modulating signal at pin 5, the UTP level changes to,

$$UTP = \frac{2V_{CC}}{3} + V_{mod}$$

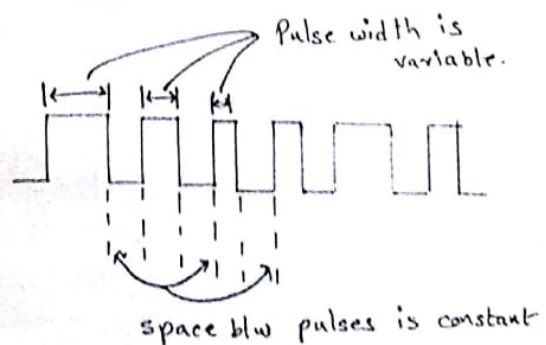


Fig (b). waveforms of o/p of PPM

→ When V_{mod} increases, the UTP level increases and hence pulse width also increases.

→ If V_{mod} decreases, UTP level decreases and pulse width also decreases. Thus the pulse width varies as shown in the Fig 4

→ The circuit is used in communication applications for transferring voice or data.

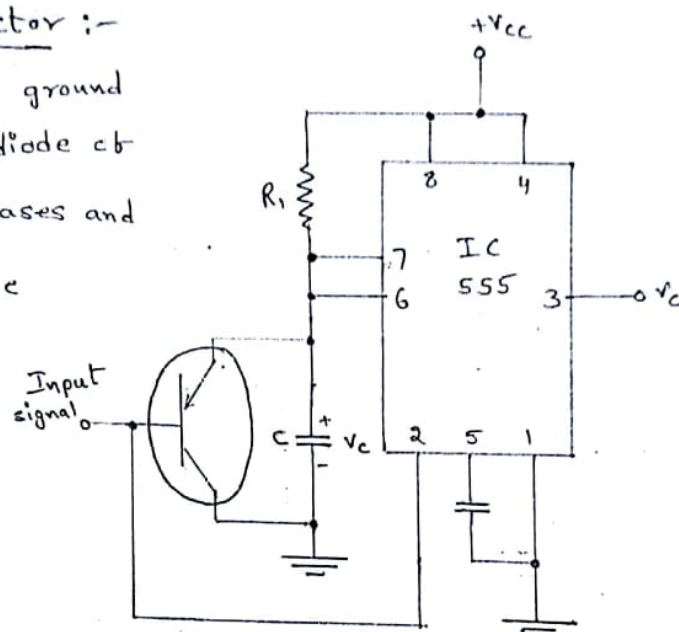
⑤ Missing Pulse Detector :-

→ When signal input is at ground level (0V), the emitter diode of transistor T₁ forward biases and clamps capacitor voltage V_c to 0.7V.

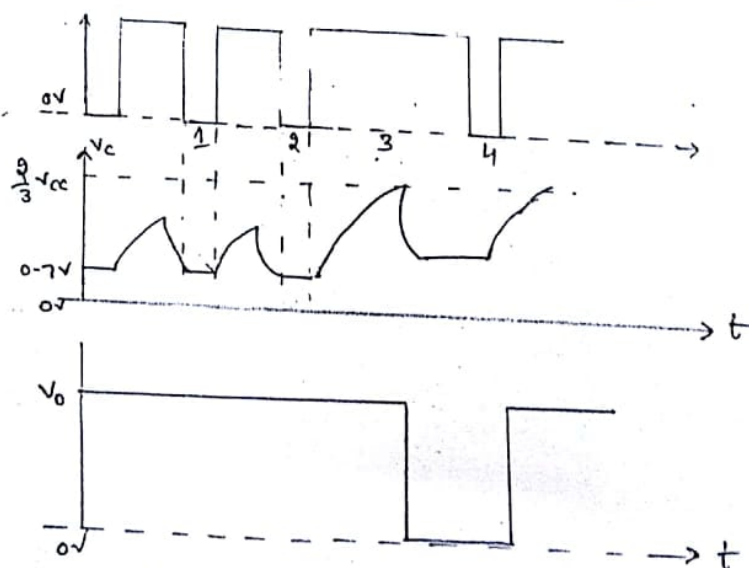
→ This forces o/p voltage to stay in its high state.

→ When signal i/p goes high, the transistor cuts off and capacitor C begins to charge.

→ If i/p signal again goes low before the 555 completes its timing cycle,



Fig(a). Missing Pulse detector



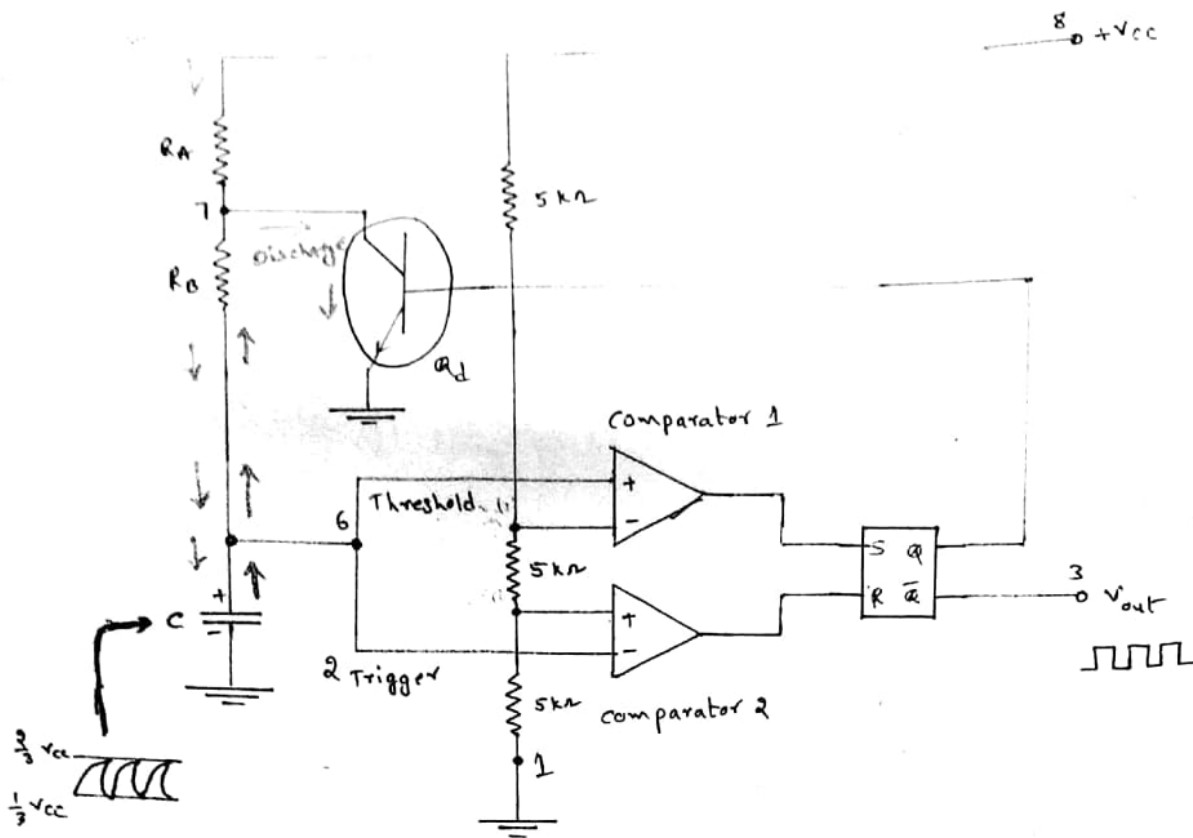
Fig(b). Waveform for Missing Pulse detector.

the voltage across C is reset to 0 V

- The, however, if signal does not go low before the 555 completes its timing cycle, the 555 enters its normal state and output voltage goes low.
- For this circuit timing interval is adjusted such that it is slightly larger than the period of i/p signal.
- The continuous low going pulses of the period less than the timing interval do not allow capacitor to charge upto $\frac{2}{3} V_{cc}$.
- As a result, o/p voltage remains high.
- In case of missing pulse (pulse u), capacitor charges upto $\frac{2}{3} V_{cc}$ and forces o/p voltage in to its low state, as shown in the fig. b.
- This type of circuit can be used to detect a missing heart beat.

* Astable Operations:-

- The threshold i/p is connected to the trigger i/p .
- Two external resistances R_A, R_B and a capacitor C is used in the circuit.
- This circuit has no stable state. The circuit changes its state alternately. Hence the operation is also called free running nonsinusoidal oscillator.



Fig(a). Astable operation of 555

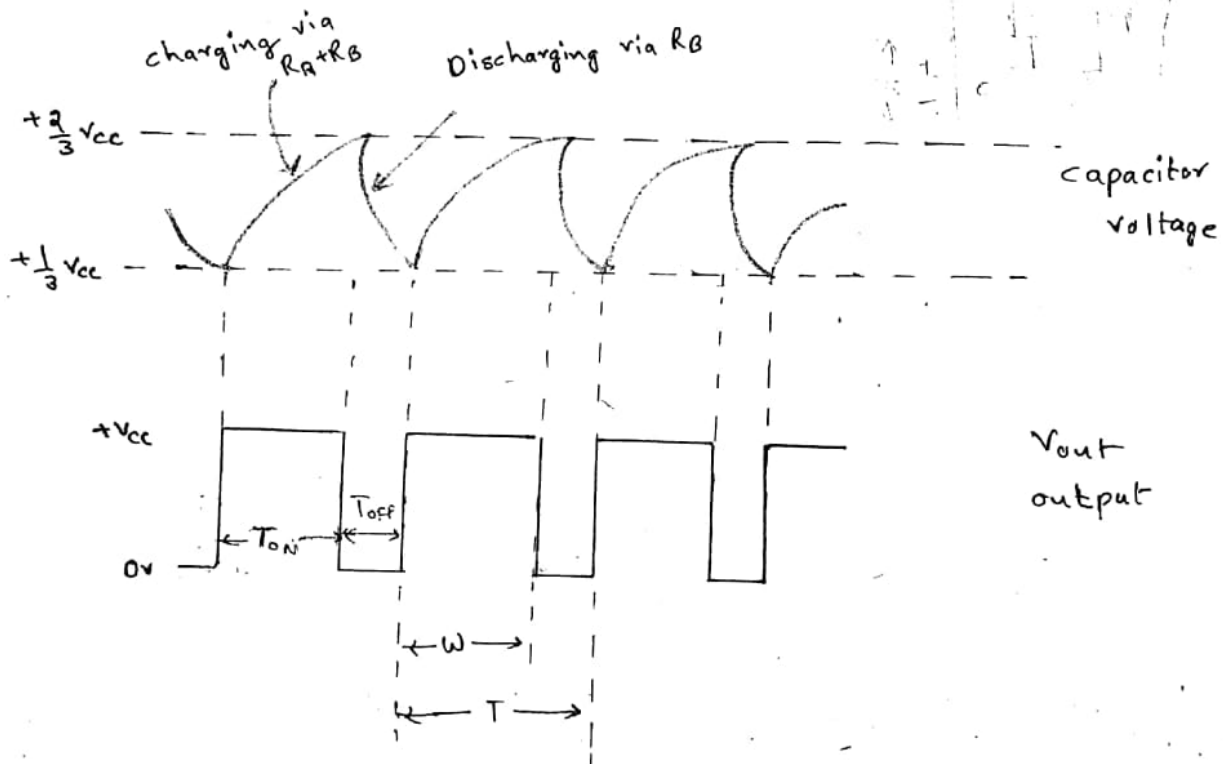


Fig.(b). Waveforms of Astable Operation

Operation :-

- When the flip-flop is set, Q is high which drives the transistor Q_d in saturation and the capacitor gets discharged.
- Now the capacitor voltage is nothing but the trigger voltage. So while discharging, when it becomes less than $\frac{1}{3} V_{CC}$, comparator 2 o/p goes high.
- This resets the flip-flop hence Q goes low and $\bar{Q}$ goes high.
- The low Q makes the transistor off. Thus capacitor starts charging through the resistances R_A, R_B and V_{CC} .
- (The charging path is shown by Green arrows in the Fig. a.)
- As total resistance in the charging path is $(R_A + R_B)$, the charging time constant is $(R_A + R_B)C$.
- The capacitor voltage is also a threshold voltage.
- While charging, capacitor voltage increases i.e., the threshold voltage increases.
- When it exceeds $\frac{2}{3} V_{CC}$, then the comparator 1 o/p goes high which sets the flip-flop. The flip-flop o/p Q becomes high and o/p at pin 3 i.e., $\bar{Q}$ becomes low.
- High Q drives transistor Q_d in saturation and capacitor starts discharging through resistance R_B and transistor Q_d .
- This path is shown by red arrows in the fig.
- Thus the discharging time constant is $R_B C$.
- When capacitor voltage becomes less than $\frac{1}{3} V_{CC}$, comparator 2

output goes high, resetting the flip-flop. This cycle repeats.

→ Thus when capacitor is charging, o/p is high while when it is discharging the o/p is low. The o/p is a rectangular wave. The capacitor voltage is exponentially rising and falling.

Derivation of Duty cycle :-

→ Generally the charging time constant is greater than the discharging time constant. Hence, at the o/p , the waveform is not symmetric.

→ The high o/p remains for longer period than low o/p .

→ The ratio of high o/p period and low o/p period is given by a mathematical parameter called duty cycle.

Def:- The ratio of ON time i.e., high o/p to the total time of one cycle.

$$\%D = \frac{w}{T} \times 100 \%$$

where $w \rightarrow$ Time for o/p is high $= T_{on}$
 $T \rightarrow$ Time of one cycle

$$D = \frac{w}{T} \quad \text{i.e.,}$$

The charging time for the capacitor is given by

$$T_c = \text{charging time} = 0.693 (R_A + R_B) C$$

→ while the discharge time is given by,

$$T_d = \text{Discharge time} = 0.693 R_B C$$

→ Hence the time for one cycle is,

$$T = T_c + T_d = 0.693 (R_A + R_B) C + 0.693 R_B C$$

$$T = 0.693 (R_A + 2R_B) C$$

→ while $W = T_c = 0.693 (R_A + R_B) C$

$$\therefore \% D = \frac{W}{T} \times 100 = \frac{0.693 (R_A + R_B) C}{0.693 (R_A + 2R_B) C} \times 100$$

$$\% D = \frac{(R_A + R_B)}{(R_A + 2R_B)} \times 100$$

→ while the frequency of oscillations is given by,

$$f = \frac{1}{T} = \frac{1}{0.693 (R_A + 2R_B) C} \quad \text{i.e.,}$$

$$f = \frac{1.44}{(R_A + 2R_B) C} \text{ Hz}$$

* Note :- If R_A is much smaller than R_B , duty cycle approaches to 50% and o/p waveform approaches to square wave.

Applications :-

- ① Square wave Generator
 - ② Voltage controlled Oscillator (VCO)
 - ③ Frequency shift keying (FSK)
- } → These two discussed in IC 565 PLL.

* Application of Astable Multivibrator:-

① Square Wave Generator:-

→ It can be observed from the expression of duty cycle that in astable operation "exact 50% duty cycle" is "not possible" to achieve.

→ To get exactly 50% duty cycle i.e.,

square wave of it is necessary to modify the astable timer ckt,

→ In the modified ckt, the capacitor "C charges through R and diode D" and discharges through R_B ."

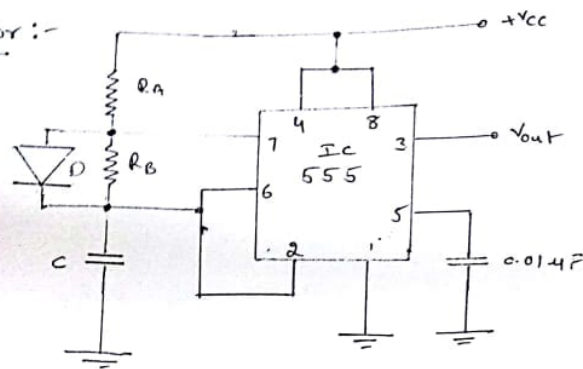
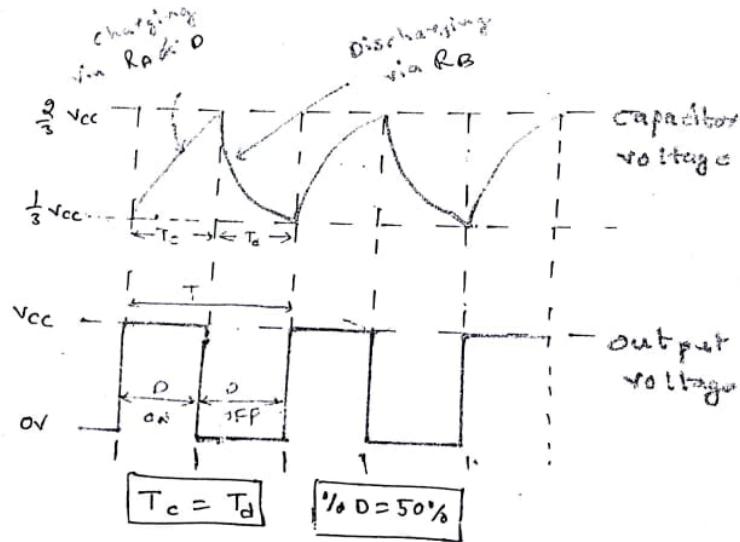


Fig.(a) Square Wave Generator



Fig(b). Waveforms

→ To obtain square wave (50% duty cycle) resistance

R_B is adjusted such that it is equal to the summation of resistance R_A and the forward resistance of diode D.

→ Usually, Potentiometer is used for exact adjustments of resistors.

IC 565 PLL Phase Locked Loop (1)

PLL (Phase Locked Loop): A phase locked loop is basically a closed loop system designed to lock the o/p frequency and phase to the freq and phase of an i/p signal.

* Block schematic or Block diagram of IC 565 PLL

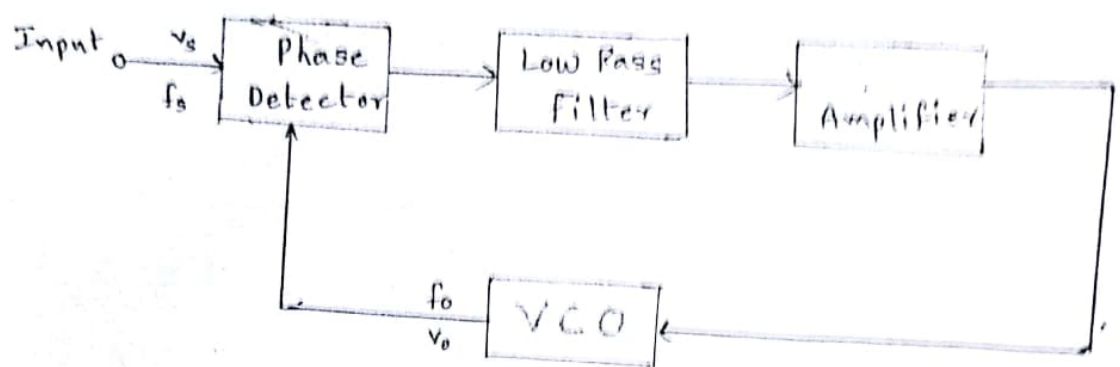


Fig. Block Diagram of PLL.

- Block diagram consist of
- * Phase Detector
 - * Low pass filter
 - * Error amplifier
 - * VCO (Voltage Controlled oscillator)

Operation :-

- The phase detector compares the i/p freq f_s with the feedback freq f_o and generates an o/p signal which is a fun of the diff b/w the phases of the two i/p signals.
- The o/p signal of the phase detector is a dc voltage.

- The op of phase detector is applied to Low Pass filter (LPF) to remove high freq noise from the d.c. voltage.
- The op of LPF without high freq noise is often referred to as amplifier (or) error amplifier (or) error voltage (or) Control voltage for VCO.

(2)

A voltage controlled oscillator (VCO) is an oscillator ckt in which the freq of oscillations can be controlled by an externally applied voltage.

- The VCO provides the linear relationship b/w the applied voltage & the oscillation frequency.
- Applied voltage is called control voltage.
- When control voltage is zero, VCO is in free-running mode and its op freq is called as center freq (f_0).
- The non-zero control voltage results in a shift in the VCO freq from its free-running freq, f_0 to a freq f , given by $f = f_0 + K_v V_c$

where $K_v \rightarrow$ voltage to freq transfer co-eff of the VCO.

- The error or control voltage applied as an i/p to the VCO, forces the VCO to change its op freq in the direction that reduces the difference b/w the i/p freq & the op freq of VCO.

This action, commonly known as capturing⁽²⁵⁾, continues till the o/p freq. of VCO is same as the i/p signal frequency.

(3)

→ Once the two freq's are same, the ckt is said to be locked.
→ In locked condition, phase detector generates a constant dc level which is required to shift the o/p freq. of VCO from centre freq. to the i/p frequency.

→ Once locked, PLL tracks the freq. changes of the i/p signal. Thus, a PLL goes through three states: free running, Capture and Phase lock.

Lock range:- When PLL is in lock, it can track freq. changes in the incoming signal. The range of freq's over which the PLL can maintain lock with the incoming signal is called the lock range or tracking range of the PLL. It is usually expressed as a percentage of f_0 , the VCO frequency.

Capture range:- The range of freq's over which the PLL can acquire lock with an i/p signal is called the capture range. It is also expressed as a percentage of f_0 .

Pull-in time:- The capture of an i/p signal does not take place as soon as the signal is applied, but it takes finite time. The total time taken by the PLL to establish a lock is called pull-in time. This depends on the initial phase &

they diff the two signal as well as in the overall loop again and the bandwidth of the low pass filter.

(11)

Phase Detector/Comparator Block of PLL :

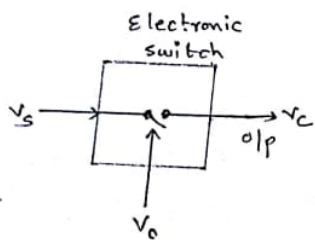
There are two types of phase detectors: ① Analog
② Digital.

① Analog Phase Detector:- Two types

(i) Switch type phase detector

(ii) Balanced modulator type phase detector.

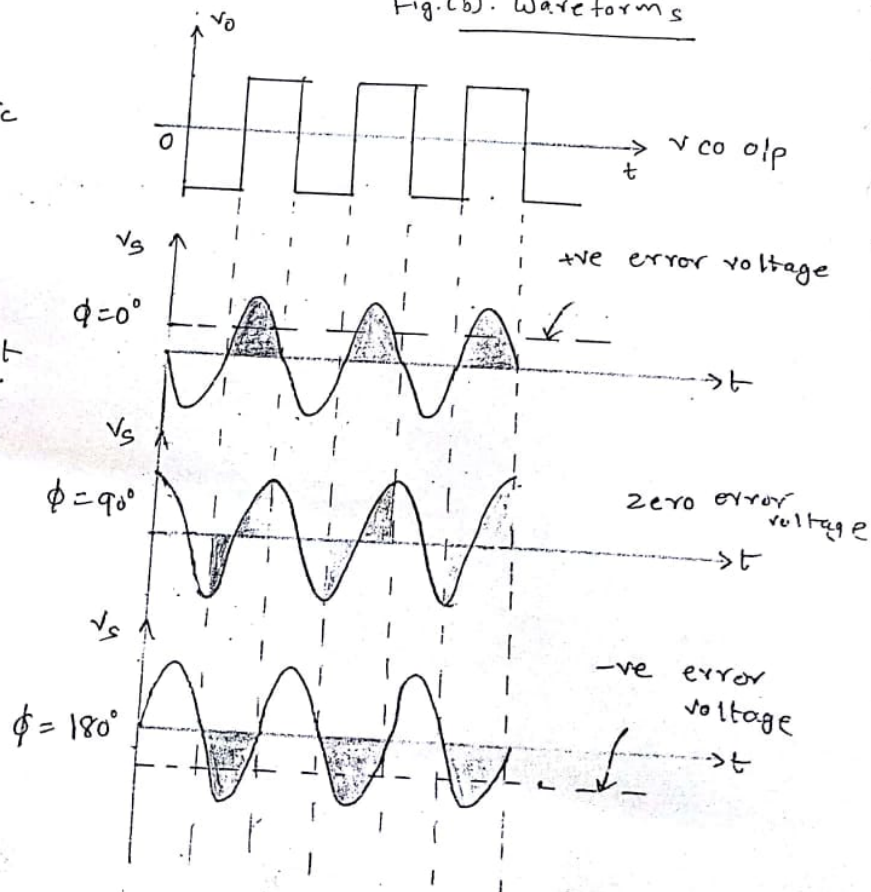
① (i) Switch type Phase Detector:-



(From VCO):

Fig.(a). Basic ckt

Fig.(b). Waveforms



Phase detector consists of electronic switch⁽⁴³⁾.
The switch is opened and closed by signal coming from VCO.
The switch is closed when VCO o/p is +ve, otherwise it is open.

(5)

The o/p of phase detector at different phase angles of i/p signal

When $\phi = 0$, i.e., when the i/p signal V_s is in phase with VCO o/p V_o , the o/p waveform V_e will be +ve half sinusoids (shaded portion).

When $\phi = 90^\circ$, the o/p waveform V_e contains half portion of -ve cycle and half portion of +ve cycle.

When $\phi = 180^\circ$, the o/p waveform V_e contains -ve half sinusoids.

→ The average o/p voltages (error voltage) at different phase angles of i/p signal are shown in respective figures by dotted line.

→ It may be seen that the error voltage is zero when the phase shift b/w the two inputs (V_s and V_o) is 90° .

→ This is a perfect lock condition. For phase shifts 0° and the error voltage is +ve and -ve, respectively.

→ The detector is called a half wave detector, since the phase information for only one-half of the i/p waveforms is detected and averaged.

→ A phase detector actually multiplies the i/p signal ($V_s = V_s \sin(2\pi f_s t)$) by the VCO signal ($V_o = V_o \sin(2\pi f_o t + \phi)$).

The o/p of multiplication is an error signal and it is given as

$$V_e = KV_s V_o \sin(2\pi f_s t) \sin(2\pi f_o t + \phi) \quad (6)$$

where $K \rightarrow$ phase detector gain or attenuation constant

$$V_e = \frac{KV_s V_o}{2} [\cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi)]$$

$$f_s = f_o$$

At lock condition

$$V_e = \frac{KV_s V_o}{2} [\cos(-\phi) - \cos(2\pi \times 2f_o t + \phi)]$$

→ The above Eqn shows that the phase detector o/p contains double freq term and a d.c. term. The d.c. term $(KV_s V_o / 2) \cos \phi$ varies as a function of phase ϕ , i.e., $\cos \phi$ b/w the two signals.

→ The double freq term is filtered by the low pass filter and d.c. term is applied to the modulating i/p terminal of a VCO.

→ The dc term i.e., the dc error voltage is zero at $\phi = 90^\circ$. Therefore, for perfect lock condition $f_s = f_o$ and $\phi = 90^\circ$

② Digital Phase Detector :- Phase Detector Using XOR Gate :-

XOR gate can be used as a digital phase detector.

When both signal f_s & f_o are square waves.

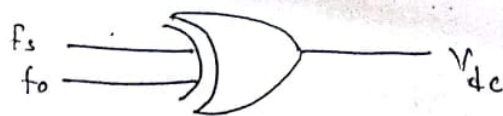


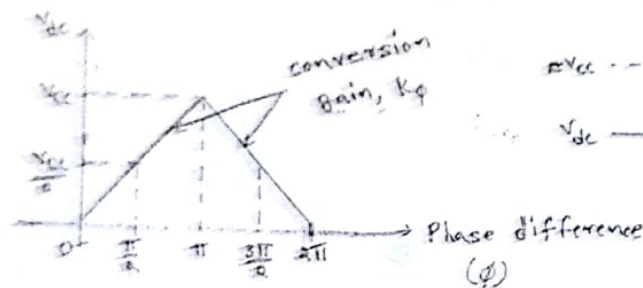
Fig-(a) XOR as a digital phase detector

→ When the o/p of XOR gate is high when only one of the i/p signals is high

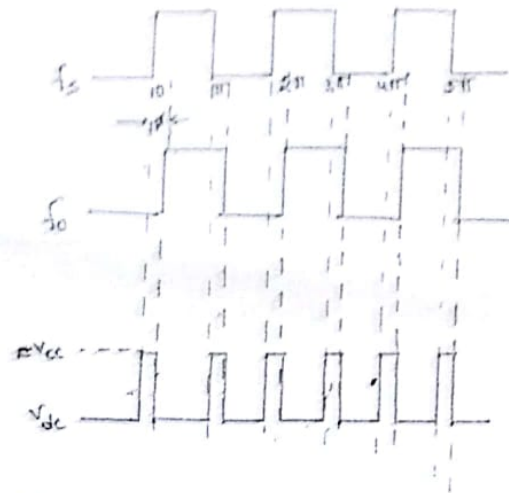
(7)

→ From Fig. (b), it can be realized

that when $\phi = 0$, $V_{dc} = 0$ and when $\phi = \pi$, $V_{dc} = V_{cc}$. The relationship b/w V_{dc} and Phase difference ϕ is plotted below.



Fig(b) Input/output waveforms



→ The slope of the curve gives the conversion ratio K_ϕ of the phase detector. It is given by

$$K_\phi = \frac{V_{cc}}{\pi}$$

For $V_{cc} = 5V$, $K_\phi = \frac{5}{\pi} = 1.591 \text{ V/rad}$

Filters used in PLL :-

The filter section of PLL can be made up of two types of filters: ① Loop filter & ② sideband filter

① Loop filter - Loop filter controls the fundamental loop characteristics such as loop bandwidth, locking time and transient response by establishing values for the loop natural frequency and the damping factor.

- The error signal from the phase detector tends to be in the form of pulse appearing at the rate of f_s .
- Due to this freq. f_i and its lower harmonics present as a major spectrum component and that must be removed by filtering. Loop filter provides attenuation to these freq's.

(8)

② Sideband filter:-

Sideband filter provides additional filtering of the error signal to generate a stable and clean control voltage to the VCO.

- It provides attenuation to sidebands that are created due to disturbances on line.
- These disturbances freq. modulate the VCO and cause undesired frequencies (or) sidebands.

Voltage Controlled Oscillator (VCO) IC 566 :-

- A VCO is an oscillator ckt in which the freq. of oscillations can be controlled by an externally applied voltage.

- The VCO provides the linear relationship b/w the applied voltage and the oscillation freq. Applied voltage is called control voltage.

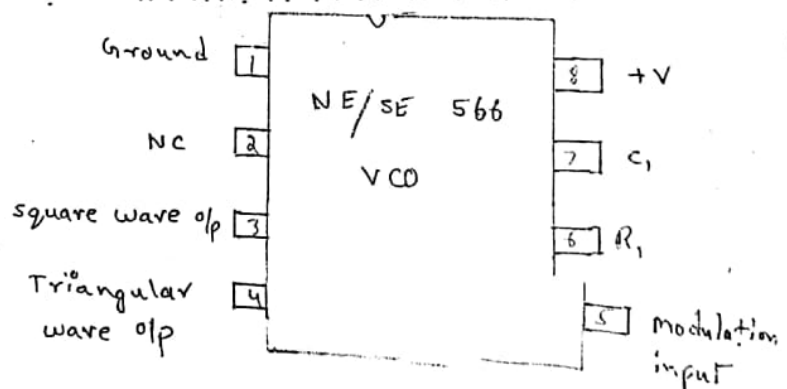
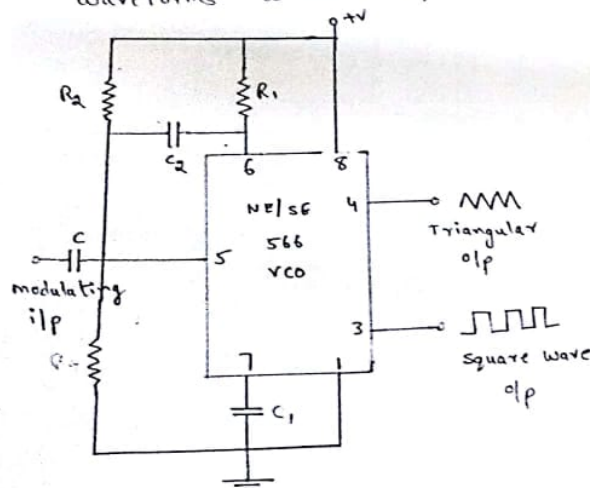


Fig. Pin diag. of IC 566 VCO

→ The control of freq with the help of control voltage is also called voltage to frequency conversion. Hence VCO is also called voltage to frequency converter.

→ Practically VCO is used to produce square and triangular waveforms whose freq is controlled by control voltage.



Features of 566 VCO:-

- ① Wide supply voltage range 10V to 24V.
- ② Very linear modulation characteristics.
- ③ High temperature stability.
- ④ Excellent power supply rejection.
- ⑤ 10 to 1 freq range with fixed C_1 .
- ⑥ The freq can be controlled by means of current, voltage, resistor & capacitor.

Application of VCO :-

- ① FM modulation.
- ② Signal Generation (Triangular or square wave).
- ③ Function " .
- ④ Frequency shift Keying (FSK) demodulator.
- ⑤ In frequency multipliers
- ⑥ Tone generation.
- ⑦ Converting low freq signals such as EEG and EKG into audio frequency range signals.

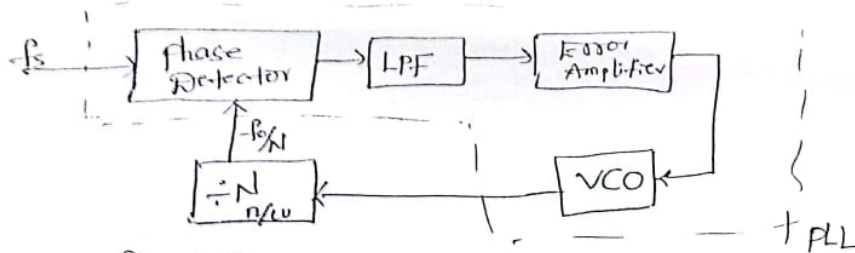
Ic 565 PLL Applications :-

- ① Frequency Multiplier
- ② Frequency Synthesizer
- ③ FM Demodulator
- ④ Frequency shift keying (FSK) Demodulator.
- ⑤ AM Detection.
- ⑥ Frequency Translation.

565 PLL Applications: $\rightarrow$

1) Frequency multiplier/division:

A divide by N network is inserted b/w the VCO o/p and the phase comparator i/p.



$$\therefore f_o = N f_s$$

* It is also used for freq division

$$f_o = \frac{f_s}{m}$$

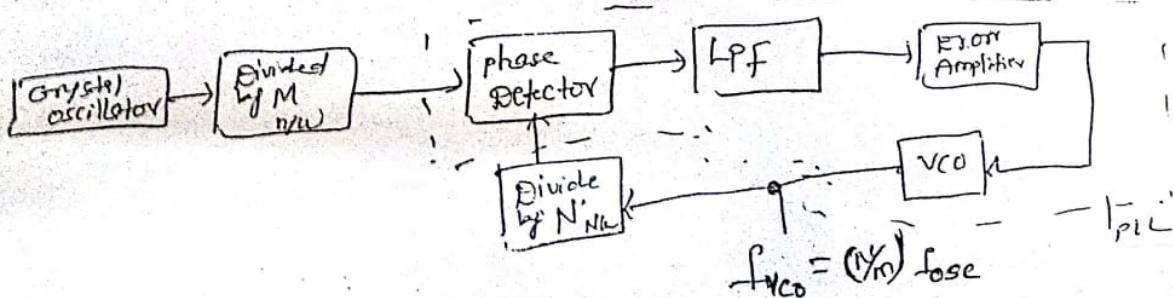
* The IC 7490 is a 4-bit binary counter. It is configured as a divide by 10 circuit.

2) Frequency synthesizer:

It can produce a precise series of frequencies that are derived from a stable crystal controlled oscillator.

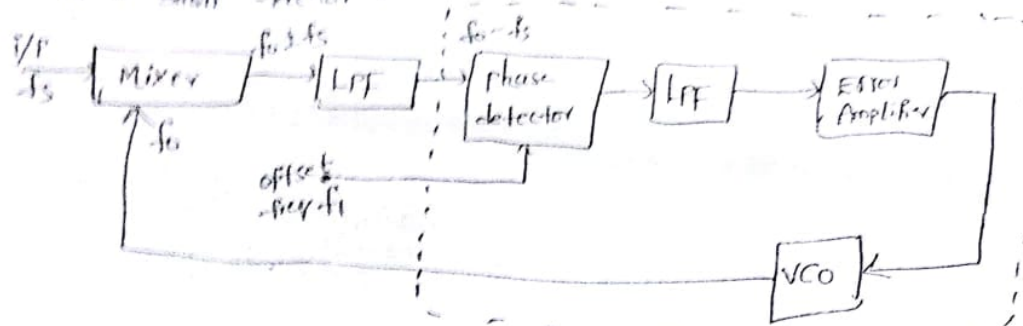
* It is similar to frequency multiplier circuit except that divide by M n/w is added at the i/p of PLL.

* When the PLL is locked in on the divided down oscillator freq we will have $\frac{f_{osc}}{m} = \frac{f_{vco}}{N}$ then $f_{vco} = \left(\frac{N}{m}\right) f_{osc}$



Frequency translation $\rightarrow$

The frequency translation means shifting the frequency of an oscill. by a small factor.



* PLL consists of mixer, LPF and PLL. The i/p freq f_s which has to be shifted is applied to mixer. Another i/p to the mixer is the o/p voltage of VCO f_o .

* The o/p of mixer is the ~~o/p voltage~~ contains sum and difference signal $(f_o + f_s)$.

* The LPF connected at the o/p of mixer rejects $(f_o + f_s)$.

* The $(f_o + f_s)$ is applied to the phase detector. Another i/p for phase detector is the offset freq f_1 .

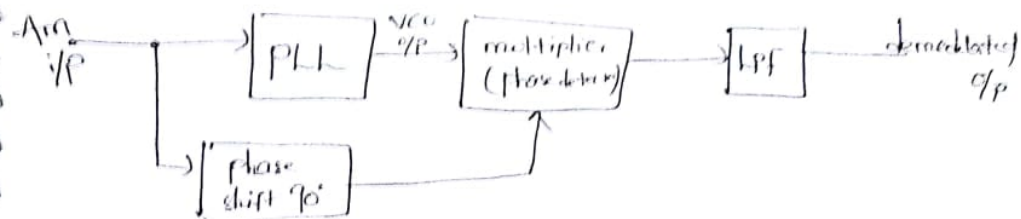
* In the locked mode, the VCO o/p freq is adjusted to make two i/p freq of phase detector equal.

$$i.e. f_o + f_s = f_1$$

$$f_o = f_s + f_1$$

By adjusting offset freq f_1 we can shift the freq of oscillator to desired value.

Am De-tection $\rightarrow$ or Demodulation $\rightarrow$



1) The PLL is Locked to the carrier freq of the incoming Am signal.

2) Once locked the o/p freq of VCO is same as the carrier freq but it is in unmodulated form.

3) The modulated signal with 90° phase shift and the unmodulated carrier from o/p of PLL are fed to the multiplier.

4) VCO o/p is always 90° out of phase with the incoming Am signal. Under locked condition, both the signals applied to the multiplier are in same phase.

5) Therefore o/p of multiplier contains both the sum and diff signals. The LPF connected at o/p of multiplier rejects high freq components gives demodulated o/p.

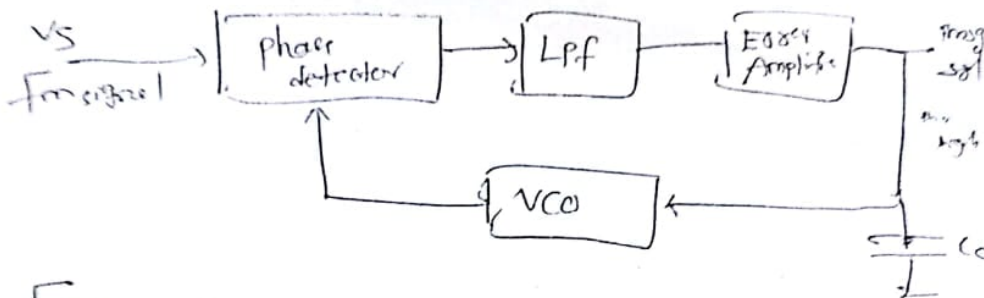
FM Demodulator :-

If PLL is Locked to a FM signal, the VCO tracks the instantaneous frequency of the i/p signal.

When PLL is locked in on the fm signal, the VCO freq follows the instantaneous freq of fm signal, and the error voltage or VCO control voltage is proportional to the deviation of the i/p freq from the centre freq.

* The AC component of error voltage or control voltage of VCO will represent a true replica of the modulating voltage that is applied to FM carrier at the transmitter.

* The faithful reproduction of modulating voltage depends on the linearity b/w the instantaneous frequency deviation and the control voltage of VCO.

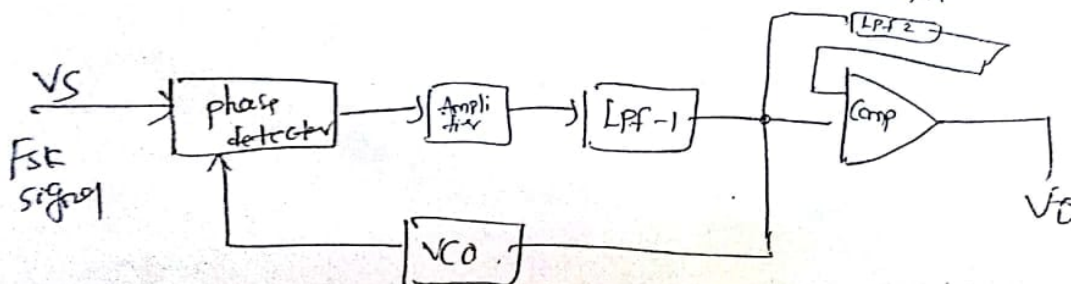


FSK demodulator:-

In Digital data Communication and Computer peripheral, binary data is transmitted by means of a carrier frequency.

* This type of data transmission is called FSK.

* In this data transmission, on the receiving end, two carrier frequencies are converted into 1 and 0 to get original data. This process is called FSK demodulation.



UNIT - III (Data Conversion)

① Introduction

② Basic DAC techniques

③ Different types of DACs

→ Weighted resistor DAC

→ R-2R ladder DAC

→ Inverted R-2R DAC

④ Different types of ADC's

→ Parallel comparator type ADC

→ Counter type ADC

→ Successive Approximation ADC

→ Dual slope ADC

⑤ DAC and ADC specifications.

Data Converters

* Introduction :-

Most of the information carry signals such as voltage, current, charge, temperature, pressure and time are available in the analog form. However, for processing, transmission and storage purposes, it is often more convenient to express such signals in the digital form. When expressed in the digital form, they provide better accuracy and reduce noise.

Moreover, the development in the microprocessor technology has made it compulsory to process data in the digital form. Since digital systems such as microprocessors use a binary system of ones and zeros, we have to convert signal from analog form to digital form. The circuit that performs this conversion is called an analog to digital (A/D) converter.

On the other hand, a digital to analog (D/A) converter is used when a binary output from a digital system must be converted to some equivalent analog voltage (or) current.

Example:- If in a particular system a computer is used as a controller, the controlling signal produced by the computer is always digital. The system to be controlled requires

the analog signal hence in between the computer and the system to be controlled the digital to analog converter is must.

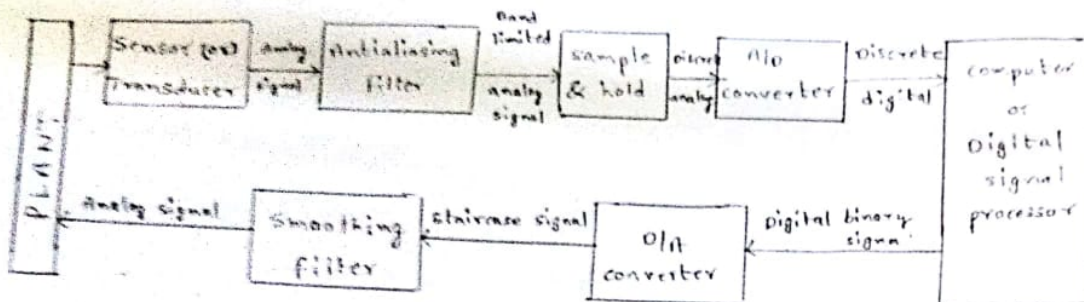


Fig. Circuit showing application of A/D and D/A converter

* Basic DAC Techniques:-

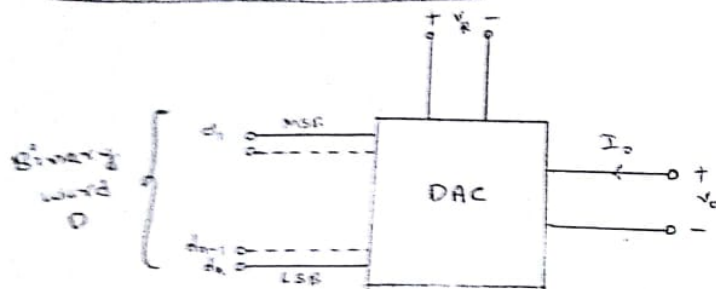


Fig. Schematic of a DAC

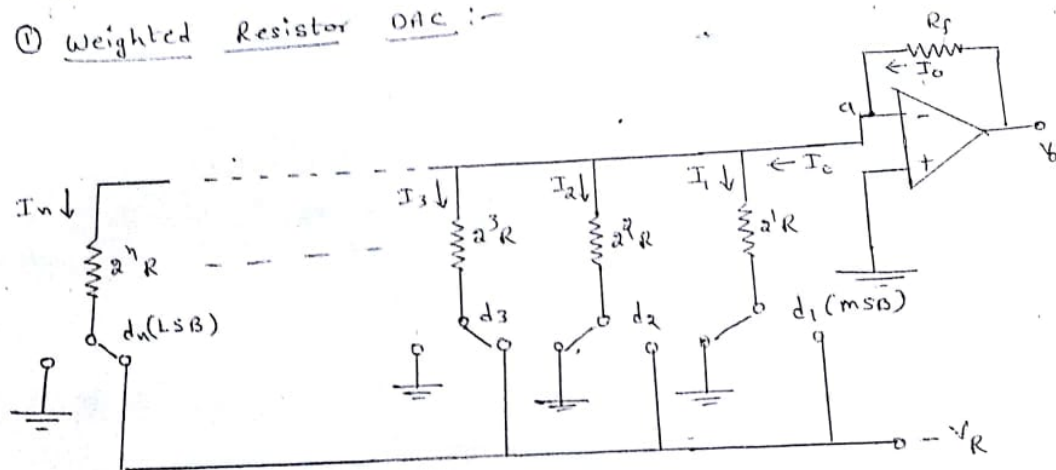
- The I_p is an n -bit binary word D and is combined with a reference voltage V_R to give an analog o/p signal.
- The o/p of a DAC can be either a voltage or current.
- For a voltage o/p DAC, the D/A converter is mathematically described as

$$V_o = K V_{FS} (d_1 a^{-1} + d_2 a^{-2} + \dots + d_n a^{-n}) \quad \text{--- (1)}$$

where, $V_o \rightarrow$ output voltage
 $V_{fs} \rightarrow$ Full scale output voltage
 $R \rightarrow$ scaling factor usually adjusted to unity
 $d_n \rightarrow$ n-bit binary fractional word with the decimal point located at the left
 $d_1 \rightarrow$ Most Significant Bit (MSB) with a weight of $V_{fs}/2$
 $d_n \rightarrow$ Least Significant Bit (LSB) " " " " $V_{fs}/2^n$

* Different Types of DAC's :- 3 types

① Weighted Resistor DAC :-



→ The binary weighted resistor DAC uses an op-amp to sum n binary weighted currents derived from a reference voltage V_R via current scaling resistors $2R, 4R, 8R, \dots, 2^n R$

→ It has n - Electronic switches $d_1, d_2, \dots, d_n$ controlled by binary i/p words.

→ These switches are "Single Pole Double Throw" (SPDT) type
 → If the binary i/p to a particular switch is '1', it connects the resistances to the reference voltage ($-V_R$).

→ If the i/p bit is 0, the switch connects the resistor to ground.

→ The o/p current is

$$I_o = I_1 + I_2 + \dots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \dots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R} [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}]$$

The o/p voltage

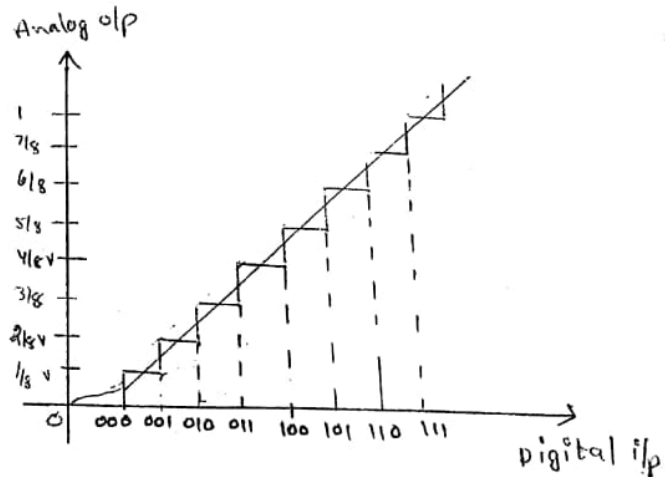
$$V_o = I_o R_f$$

$$V_o = V_R \frac{R_f}{R} [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}] \quad \text{--- (2)}$$

Compare Eqn (1) & (2) if $R_f = R$ then $K=1$ & $V_{FS} = V_R$

→ It uses a -ve reference voltage, then the analog o/p voltage is +ve.

Digital i/p	d_1	d_2	d_3
D_1	0	0	0
D_2	0	0	1
D_3	0	1	0
D_4	0	1	1
D_5	1	0	0
D_6	1	0	1
D_7	1	1	0
D_8	1	1	1



→ Op-amp also connect in non-inverting mode. It acts as I-V converter.

Drawbacks

- (1) As the increases $2^2 R, 2^3$ Small
- (2) For volt

(2) R

→ In res

→ By of

→

Drawbacks,

(1) As the no of bits increases, the range of resistance increases. For 8 bit, the resistors required are $2^1 R$, $2^2 R$, $2^3 R$, & $2^8 R$ large resistor is 128 times the small one.

(2) For 12 bit largest $R = 6.12 \text{ M}\Omega$ & small is $R = 2.5 \text{ k}\Omega$ due to voltage drop across such large R effect the accuracy.

(R) R-2R Ladder DAC (Voltage Switching Mode DAC):-

→ In the weighted resistor DAC, we require wide range of resistors to avoid this we are using R-2R ladder.

→ By using R-2R ladder type DAC where only two values of resistors are required i.e., R from $2.5 \text{ k}\Omega$ to $10 \text{ k}\Omega$

→ Consider a 3 bit DAC 100 where switch position $d_1 d_2 d_3$ corresponds to the binary word

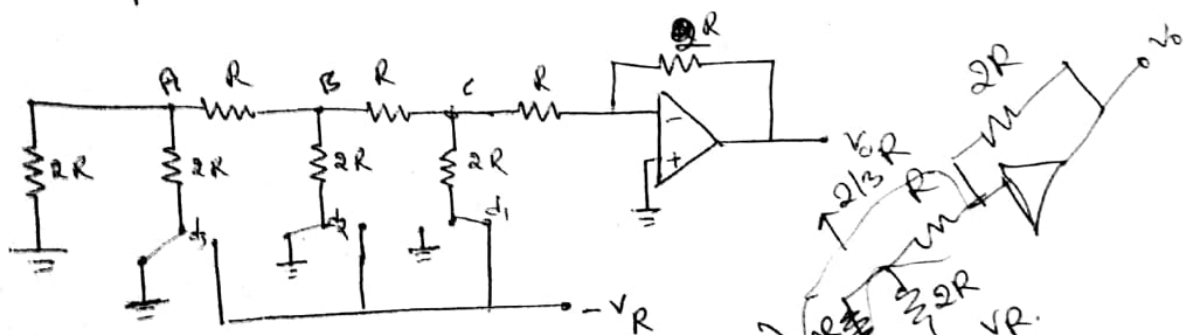


Fig. (a)

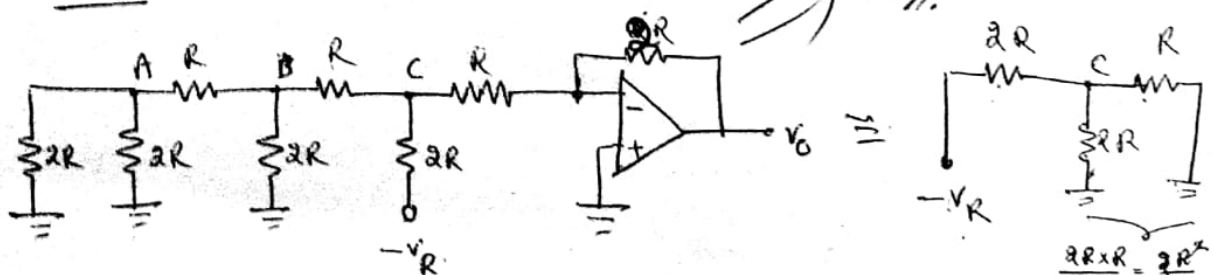
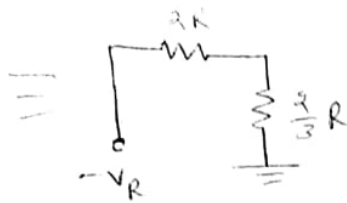


Fig. (b). Equivalent CKT



By voltage divider rule $\Rightarrow \frac{-V_R \left(\frac{2}{3}R\right)}{2R + \frac{2}{3}R} = -\frac{V_R}{4}$

Op-amp is Inverting op-amp,

$$V_o = -\frac{2R}{R} \left(-\frac{V_R}{4}\right)$$

$$\left[\because V_o = -\frac{R_F}{R_i} V_{in} \right]$$

$$= \frac{V_R}{2}$$

$$V_o = \frac{V_{FS}}{2}$$

③ Inverted R-2R Ladder (Current Steering Mode):-

③ In Inverted R-2R Ladder MSB and LSB positions are interchanged.

③ In this, each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground.

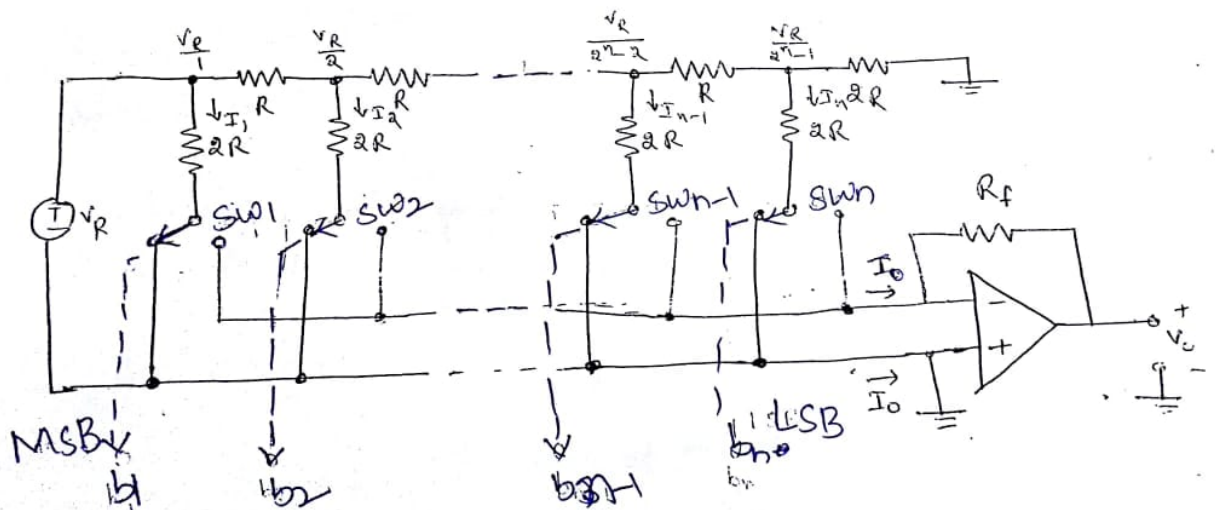
① In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. More power dissipation causes heating, which in turn, creates non-linearity in DAC. This is a serious problem and can be avoided completely in 'Inverted R-2R Ladder type DAC'.

Note:- Both the terminals of switches are at ground potential, current flowing in the resistances are constant & Independent of switch position.

Case 1:- When logic '0' when switch d_i is at logic '0' i.e., to left, the current through $2R$ resistor flows to ground.

Case 2:- When logic '1' When switch d_i is at logic '1' i.e., to the right, the current through $2R$ resistor sinks to the virtual ground.

for digital i/p $d_i = 0$ connected to ground
 $= 1$ for $-V_R$



$$I_1 = \frac{V_R}{2R}$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

⋮

$$I_n = \frac{V_R 2^{n-1}}{2R} = \frac{I_1}{2^{n-1}}$$

$$\therefore V_o = -I_1 R_f$$

$$= -R_f (I_1 + I_2 + I_3 + \dots + I_n)$$

$$= -R_f \left[b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \dots + b_n \frac{V_R}{2^n R} \right]$$

$$V_o = \frac{-V_R R_f}{R} \left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n} \right]$$

when $R_f = R$,

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

Specifications of DAC :-

- ① Resolution:- Resolution = 2^n
The ratio of a change in o/p voltage resulting from a change of 1 LSB at the digital inputs.

→ For an n-bit DAC, it can be given as

$$\text{Resolution} = \frac{V_{\text{FS}}}{2^n - 1}$$

Ex:-

8-bit DAC

Resolution = $2^8 = 256$

where $V_{\text{FS}} \rightarrow$ Full scale o/p voltage

$$V_{\text{FS}} = 10.2, \text{ Resolution} = \frac{10.2}{2^8 - 1} = \frac{10.2}{255} = 40 \text{ mV/LSB}$$

∴ An i/p change of 1 LSB causes the o/p to change by 40mV.

② Accuracy
Voltage

Example

③ Linearity

the
i/p
→ Act

the

its

the

④

sn

(3) Accuracy:- It is a comparison of actual output voltage with expected o/p. It is expressed in percentage.
 Example:- The accuracy of the should be, at worst, $\pm \frac{1}{2}$ of its last 1/2 the full scale voltage is 10.23 then for an 8-bit DAC accuracy can be given as

$$\text{Accuracy} = \frac{\% \text{ Volts}}{(2^n - 1) \times 2} = \frac{10.2}{(2^8 - 1) \times 2} = \frac{10.2}{255 \times 2} = 20 \text{mV}$$

(3) Settling Time (Conversion Time):- The time required for the DAC o/p to go from zero to full scale as the binary i/p is the binary i/p is changed from all 0's to all 1's. Actually, the settling time is measured as the time for the DAC o/p to settle within $\pm \frac{1}{2}$ step size ($\frac{1}{2} \text{LSB}$) of its final value.

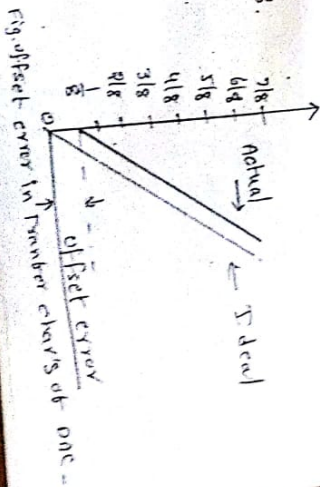
Typical values:- 50 ns to 10 μ s.

(4) Dynamic Range:- The ratio of the largest o/p to the smallest o/p, excluding zero. It is expressed in dB.

$$\text{Dynamic range} = 20 \log_{10} \approx 6 \text{ n}$$

Typical values:- 66 to 72 dB.

(5) Offset Error:- The non-zero level of the o/p voltage when all inputs are zero.

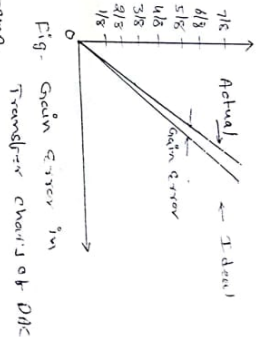


→ It is due to the presence of offset voltage in op-amp and leakage currents in the current switches.

⑥ Gain Error :-

The difference b/w the calculated gain of the current to voltage converter and the actual gain achieved.

→ It is due to the errors in the feedback resistor on the current to voltage converter op-amp.



⑦ Non-linearity (Linearity Error) :-

The non-linearity error is the amount by which the actual o/p differs from the ideal straight-line o/p. The different types of non-linearity are:

- Integral non-linearity
- Differential " "

⑧ Stability :-

The performance of converter changes with temperature, voltage and power supply variations.

→ So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

→ These parameters represent the stability of the converter.

⑨ None

none

where

Pin :

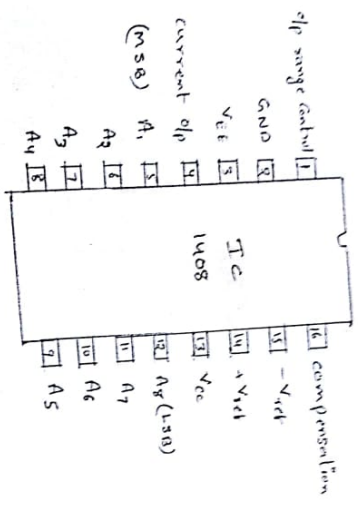
op amp

curr (ms)

→ 1

① Monotonicity :-
 A converter is said to have good monotonicity if it does not miss any step function when stepped through its entire range by a converter.

Pin diagram of IC 1408 DAC :-



Important electrical characteristics for IC 1408 :-

- (1) Ref. current - 2mA
- (2) Supply Voltage - 4.5V to 15V
- (3) Settling Time - 300ns
- (4) Full scale o/p current - 1.992mA
- (5) Accuracy - 0.1%

- The 1408 is an 8 bit R/2R ladder type D/A converter compatible with TTL and CMOS logic.
- It is designed to use where the o/p current is linear product of an eight bit digital word.
- IC 1408 consists of a reference current amplifier, an R/2R ladder and eight high speed current switches.
- It has eight i/p data lines A1(A5B) through A8(A5B) which control the positions of current switches.

A/D Converters :-

→ The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary words. Thus the A/D converter is exactly opposite function to that of the D/A converter.

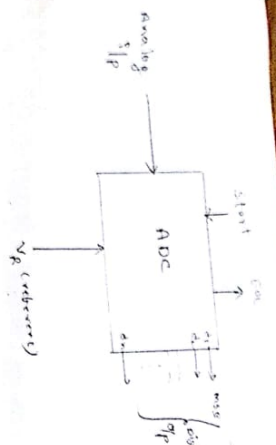


Fig. 1. Functional diagram of ADC

→ The block schematic of ADC provides the function just opposite to that of a DAC.

→ It accepts an analog I/P voltage V_a and produces an o/p binary word $d_1, d_2, \dots, d_n$ or functional value D .

$$\therefore D = d_1 2^{n-1} + d_2 2^{n-2} + \dots + d_n 2^0$$

LSB

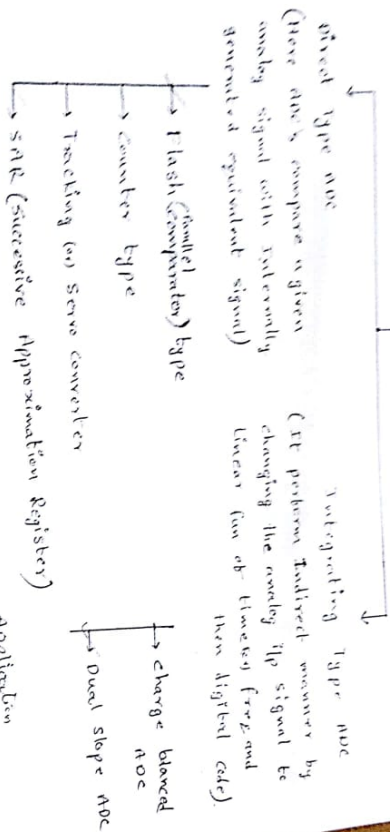
→ An ADC usually has two additional control lines the start I/P to tell the ADC when to start the conversion.

→ the EOC (End of Conversion) o/p to announce when the conversion is complete.

→ ADC are designed for microprocessor interfacing (or) to directly drive LED or LED display.

Different type of ADC

ADC (A/D to conversion technique)



Applications:-

- ① SAR is most widely used.
- ② Data logger, and Instrumentation
- ③ Flash is accurate measurement
- ④ Digital meter
- ⑤ Panel "
- ⑥ monitoring system.

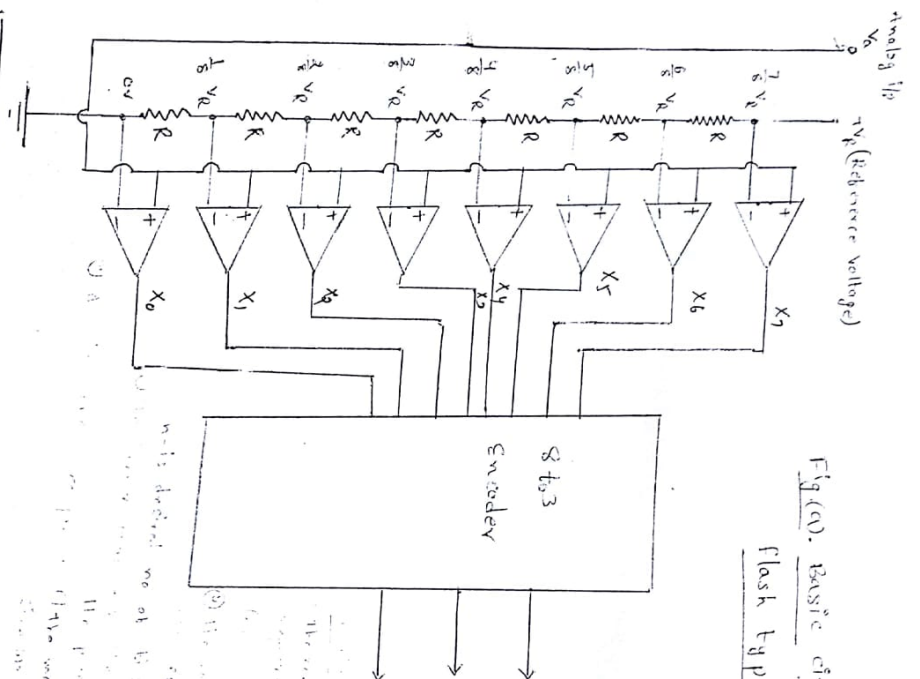
① Flash (or) Parallel Comparator Type (or) Fastest ADC :-

→ It is the simplest ADC at the same time Fastest & most expensive technique.

→ It consists of a resistive divider network, 8 op-amp comparators and 8 to 3 line encoder (3-bit Priority Encoder).

→ At each node of the resistive divider, a comparison voltage is available.

Fig (a). Basic of
Flash type



Input voltage (V _i)	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
0 to V _R /8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
V _R /8 to 2V _R /8	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
2V _R /8 to 3V _R /8	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
3V _R /8 to 4V _R /8	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
4V _R /8 to 5V _R /8	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0
5V _R /8 to 6V _R /8	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0
6V _R /8 to 7V _R /8	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
7V _R /8 to V _R	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

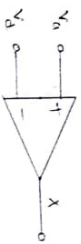


Fig. (b) Comparator

Voltage input	logic clip X
$V_A > V_d$	$X = 1$
$V_A < V_d$	$X = 0$
$V_A = V_d$	Previous Value

Fig. (c). Truth Table

→ All the resistors are of equal value, the voltage levels available at the nodes are equally divided b/w the reference voltage V_R and Ground.

→ The purpose of the ckt is to compare the analog i/p voltage V_A with each of the node voltages.
Adv: High speed, as the conversion take place simultaneously rather than sequentially.

2) Counter Type ADC:-

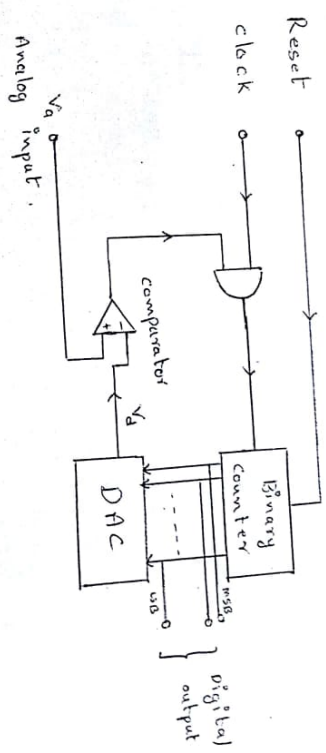


Fig. (a). A counter type A/D converter

→ The principle is to adjust the ADC's i/p code until the DAC's o/p comes with in $(\pm 1/2)$ LSB to the analog i/p V_A which to be converted to binary digital form.

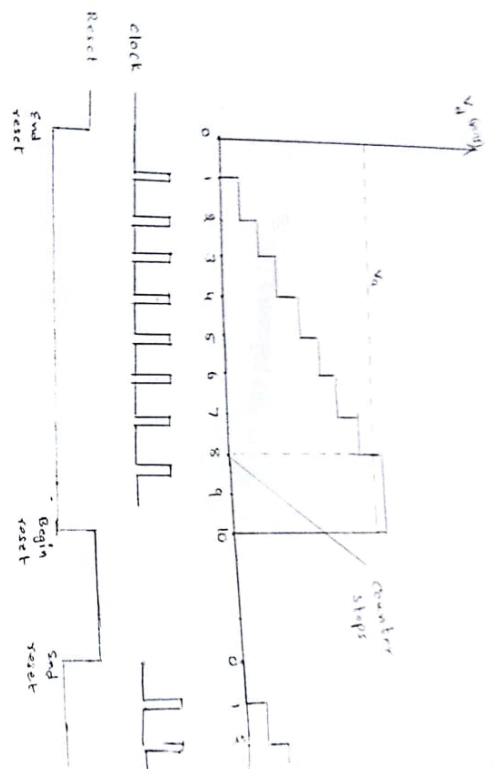


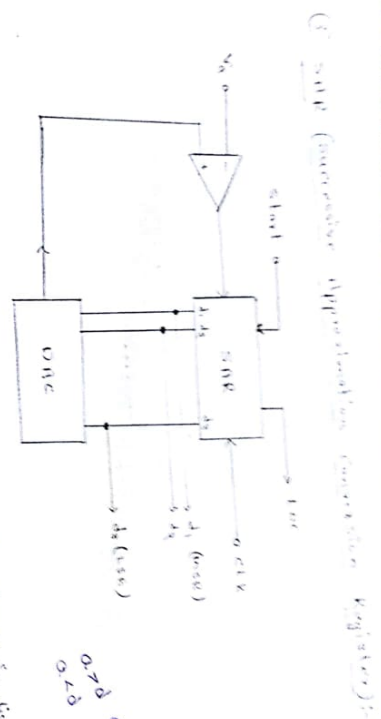
Fig (b). DAC output staircase waveform

→ Thus in addition to the DAC, we need suitable logic circuitry to perform the code search and a comparator of adequate quality to announce when the DAC output has come within $(\pm 1/2)$ LSB to V_a .

→ The counter is reset to zero. Count by the reset pulse the release of RESET, the clock pulses are counted by the binary counter.

→ These pulses go through the AND gate which is enabled by the voltage comparator high output.

- The number of pulses counted increases with time.
- The binary word representing this count is used as the i/p of a D/A converter whose o/p is a staircase.
- The analog o/p V_d of DAC is compared to the analog i/p V_a by the comparator.
 - If $V_a > V_d$, the o/p of the comparator becomes high and the AND gate is enabled to allow transmission of the clock pulses to the counter.
 - When $V_a < V_d$, the o/p of the comparator becomes low and the AND gate is disabled.
 - It will stop the counting at the time $V_a \leq V_d$ and the digital o/p of the counter represent the analog i/p voltage V_a .
- For a new value of analog i/p V_a , a 2nd reset pulse is applied to clear the counter.
- Upon the End of the Reset, the counting begins again.
- The Counter freq must be low enough to give sufficient time for the DAC to settle and for the comparator to respond.
- The conversion time can be as long as $(2^n - 1)$ clock periods depending upon the magnitude i/p of voltage V_a .
- For instance a 12-bit system with 1 MHz clock freq, the counter will take $(2^{12} - 1)$ use = 4.095 ms to convert a full scale i/p .

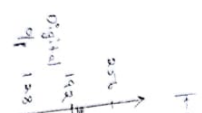


Fig(c). Functional diagram of the Successive Approximation ADC

correct digital representation	SNR o/p V_A at different stages in the conversion	Comparator o/p
11010100	1 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 1 1 1 0 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 1 0 0 0 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1	1 0 1 0 1 0 1 0

Fig(b). Successive Approximation Conversion Sequence for a

Typical Analog Input



Fig(c)

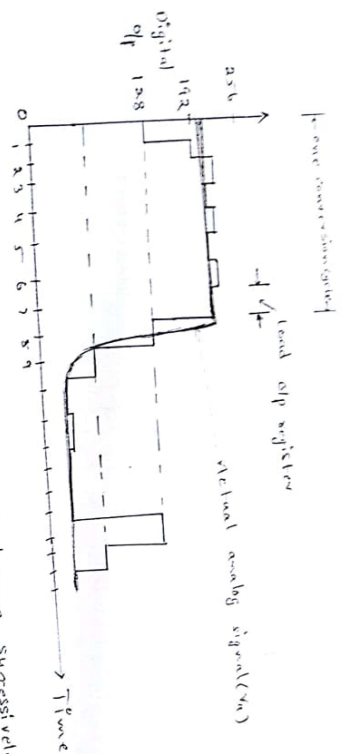


Fig. (c). The D/A o/p voltage is seen to become successively closer to the actual analog i/p voltage

- The successive approximation technique uses a very efficient code search strategy to complete n -bit conversion in just n -clock periods.
- An n -bit converter would require 2^n clock pulses to obtain a digital o/p.
- The ckt uses a SAR to find the required value of each bit by Trial and Error method.
- The ckt operates as follows. With the arrival of the start command the SAR sets the MSB $d_1 = 1$ with all other bits to zero's so that the trial code 10000000.
- The o/p of V_d is from DAC is now compared with analog i/p V_A .
- If V_A is greater than the DAC o/p V_d then 10000000 is less than the correct digital representation. The MSB is left at 1 and the next LSB made 1 and further tested.

→ If V_a is less than the D/A output then 1000 0000 is greater than the correct digital representation. So reset MSB to 0 and go on to next LSB.

→ This procedure is repeated for all subsequent bits, one at a time. Until all bit positions have been tested.

→ Whenever the D/A output crosses V_a the comparator changes state and this can be taken as the EOC command.

→ It can be seen that the D/A output voltage becomes successively closer to actual analog input voltage. It requires pulses to establish the accurate output regardless of the value of analog input.

→ One additional clock pulse is used to load output register.

4) Dual-slope ADC :-

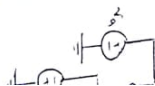
→ It is also known as Dual-Ramp converter.

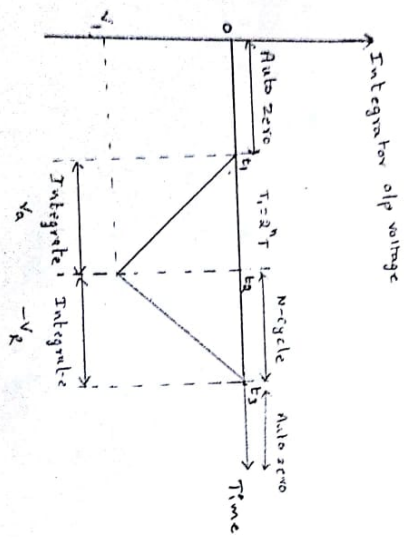
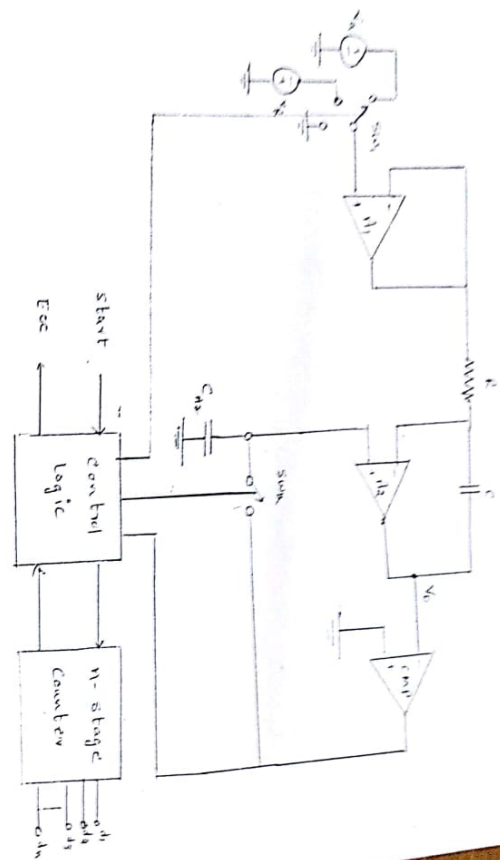
→ The analog part of the circuit consists of a High input impedance buffer A_1 , integrator A_2 and a voltage comparator.

→ The converter first integrates the analog input signal V_a for a fixed duration of 2^n clock periods.

→ Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero.

→ The number (N) of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code.





Operation :-

- Before the start command arrives, the switch sw_1 is connected to ground and sw_2 is closed.
- Any offset voltage present in the A_1, A_2 & comparator loop after integration, appears across the capacitor C_{A2} till the threshold of the comparator is achieved.
- The capacitor C_{A2} thus provides automatic compensation for the input-offset voltages of all the three amplifiers.
- When sw_1 opens, C_{A2} acts as a memory to hold the voltage required to keep the offset nulled.
- At the arrival of the start command at $t = t_1$, the control logic opens sw_1 and connects sw_2 to V_A and enables the counter starting from zero.
- The ckt uses an n -stage ripple counter and therefore the counter resets to zero after counting 2^n pulses.
- The analog voltage V_A is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero.
- If the clock period is T_1 , the integration takes place for a time $T_1 = 2^n \times T$ and the op is a Ramp going downwards.
- The counter resets itself to zero at the end of the interval T_1 and the switch sw_1 is connected to the reference voltage ($-V_R$)

→ The op voltage V_o will now have a positive slope.

→ As long as V_o is $-V_R$, the op of the comparator is +ve and the control logic allows the clock pulse to be counted

→ When V_o becomes just zero at time $t=t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter.

→ The counter at t_3 is proportional to the analog ip voltage

V_a

$$T_1 = t_3 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}}$$

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}}$$

for an Integrator.

$$\Delta V_o = \left(\frac{-1}{RC} \right) V_R \Delta t$$

The voltage V_o will be equal to V_1 at the instant t_2

$$V_1 = \left(\frac{-1}{RC} \right) V_R (t_2 - t_1)$$

$$V_1 = \left(\frac{-1}{RC} \right) (-V_R) (t_2 - t_3)$$

$$V_R (t_2 - t_1) = V_R (t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$
& $(t_3 - t_1) = N$

$$V_a (2^n) = V_R (N)$$

$$V_a = \frac{V_R \cdot N}{2^n}$$

ADC Specifications & Performance Parameters of ADC:-

1) Resolution:-

$$\text{Resolution} = 2^n$$

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

where $V_{FS} \rightarrow$ Full Scale I/P Voltage
 $n \rightarrow$ no. of bits

2) Quantization Error:-

$$Q_E = \frac{V_{FS}}{(2^n - 1) 2}$$

3) Gain and Offset Errors:-

Offset Error:- It is the difference b/w the actual and ideal first transition voltages.

The term offset, implies that all conversions are off by an equal amount.

$\rightarrow$ On the other hand, the gain error is the difference b/w the actual full scale transition voltage & the ideal full-scale transition voltage

4) Gain and Offset Drifts:-

Gain Drift:- Change in the Full-scale transition voltage measured over the entire operating temp range. (Units - $\frac{\text{ppm}}{^\circ\text{C}}$)

Offset Drift:- change due to temp in the analog zero for an ADC converter operating in bipolar mode. (Units - ppm/°C)

5) Settling Time (Conversion Time)

The total time required to convert an analog signal into its digital output.

→ It depends on the conversion technique used and the propagation delay of circuit components.

6) Sampling frequency and aliasing phenomenon:-

Sampling frequency, $f_s \geq 2f_{max}$

→ If the sampling frequency is less than $2f_{max}$ (Nyquist rate), then the faithful reproduction of original signal is not possible. However, in such cases, spurious signals called aliasing are produced.

→ The frequency of aliased signal is the difference b/w the signal frequency and the sampling frequency. This problem is called aliasing and it is removed in all practical ADC converters by using anti-aliasing filters.

7) Differential Non-linearity (DNL):-

$$DNL = CCW - ICW \quad \text{where } CCW \rightarrow \text{current code width}$$
$$ICW \rightarrow \text{Ideal} \quad " \quad "$$

8) Integral Non-linearity (INL):-

→ It is a measure of the maximum deviation of the actual ADC transfer function from a straight line drawn through the first and last code transition after correction for offset and gain errors.

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Unit IV (Digital Integrated Circuits)

IV (a)

- ① Classification of Integrated Circuits
- ② Comparison of Various logic families
- ③ CMOS transmission gate
- ④ IC Interfacing
 - TTL driving CMOS &
 - CMOS driving TTL

IV (b) - Combinational Logic IC's

- ⑤ Specifications and Applications of TTL - 74XX Series IC
- " " " CMOS - 40XX "

Code Converters

Decoders

Demultiplexers

LED & LCD decoders with drivers

Encoders (7.4)

Priority Encoders (7.4.3)

Multiplexers (7.5)

Demultiplexers (7.6)

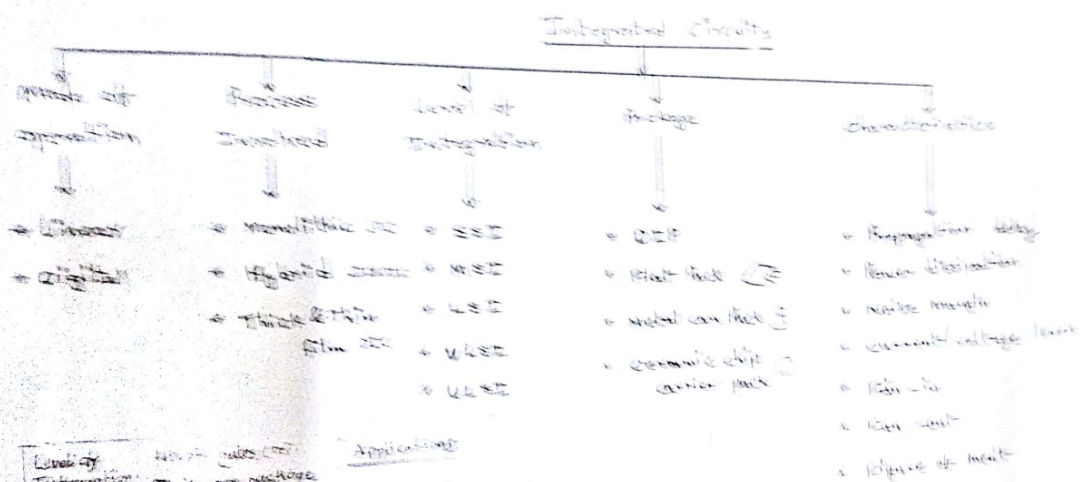
Priority Generators / checkers (7.7)

Parallel binary Adder / subtractor (7.8)

Magnitude Comparators. (7.9)

Integrated Circuits :-

① Classification of Integrated Circuits



Level of Integration	No. of gates, Transistors per package	Applications
SSI	1-20 gates	Logic gates & flip-flops
MSI	20-200 gates	Counters, Multiplexers, Registers, ALU, etc.
LSI	200-20,000	Memory, Microprocessors, etc.
VLSI	> 10,00,000	Adv. MP's, large memories, large IC's
ULSI	one billion, 10 ⁹ Transistors	64 bit MP's, Image sensors, etc.

Characteristics:

1) Propagation Delay (t_p):

The propagation delay of a gate is basically the time interval between the application of an input pulse and occurrence of the resulting output pulse.

→ The propagation delay is a very important characteristic of logic circuits because it limits the speed at which they can operate.

→ The shorter propagation delay, the higher the speed of the circuit and vice-versa.

→ The propagation delay is determined using two basic time intervals:

1. t_{PLH} : It is delay time measured when output is changing from logic 0 to logic 1. State (Low to High).



2. t_{PHL} : It is delay time measured when output is changing from logic 1 to logic 0 state (High to Low).

→ When t_{PLH} and t_{PHL} are not equal, the larger value is considered as a propagation delay time for that logic gate.

$$\text{i.e., } t_p = \max(t_{PLH}, t_{PHL})$$

2) Power Dissipation:

The amount of power that an IC dissipates is determined by the average supply current I_{cc} that it draws from the Vcc supply.

→ It is the product of I_{cc} and Vcc.

Average I_{cc} cycle operation with half of

$I_{cc(sat)}$

Average Power

P_{avg}

3) Noise

In digital by a pair of different



get the can is

Average I_{cc} is determined based on the 50% duty cycle operation of the gate (low half of the time and High half of the time).

$$I_{cc(avg)} = \frac{I_{ccH} + I_{ccL}}{2}$$

where I_{ccH} → value of I_{cc} for low gate output

Average power dissipation as I_{ccH} → value of I_{cc} for high gate output

$$P_{D(avg)} = I_{cc(avg)} \times V_{cc}$$

3. Noise Margin & current/voltage levels:-

In digital circuits, the binary 0 and 1 are represented by a pair of voltage levels. Each logic family has a different standard.

Family	logic 0	logic 1
TTL	0V	+5V
ECL	-1.7V	-0.9V
CMOS	0V	3-15V

Table. Ideal Voltage levels

In Practical, it is difficult to get these ideal voltages. Stray electric and magnetic field can induce voltages on the connecting wires and logic circuits.

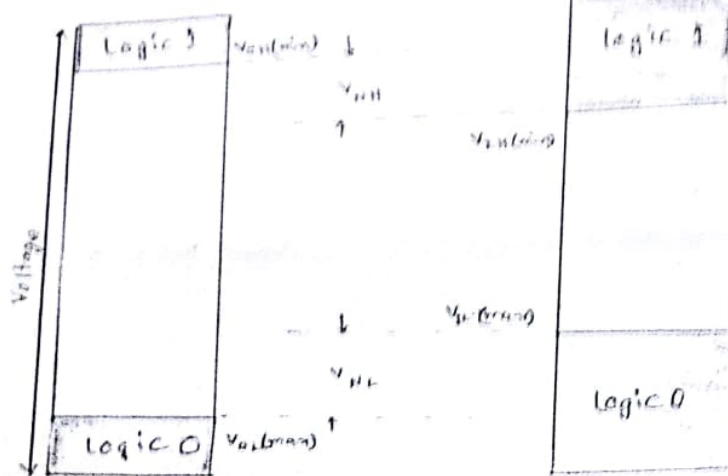


Fig. Noise margin

→ These unwanted signals are called noise and can sometimes cause the voltage at the i/p to a logic circuit to drop below $V_{IH(min)}$ (or) rise above $V_{IH(max)}$, which could produce unpredictable operation.

→ The noise immunity of a logic ckt refers to the ckt's ability to tolerate the noise without causing spurious changes in the o/p voltage.

→ To avoid this problem due to noise, voltage level $V_{IH(min)}$ is kept at a few fraction of volts below $V_{OH(min)}$ & voltage level $V_{IL(max)}$ is kept above $V_{OL(max)}$, at the design time.

$$V_{NH} = V_{OH(min)} - V_{IH(min)}$$

$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$

The noise margin allows the digital ckt to function properly if noise voltage are within the limits of V_{NH} & V_{NL} for a particular logic family.

④ Fan-in :-

The fan-in of a digital logic gate refers to the no. of inputs are connected. The fan-in provides information about the intrinsic speed of the gate itself.

→ In general, the propagation delay increases with the fan-in. This means that 2-input NAND gate is faster than the 4-input NAND if both are from same family.



⑤ Fan-out :-

When the o/p of a logic gate is connected to one (or) more i/p's of other gates, a load on the driving gate is created.

→ If there is a limit to the no. of load gate i/p's for a given can drive this limit is called fan-out of the gate.

⑥ Figure of Merit (or) Speed Power Product (SPP) :-

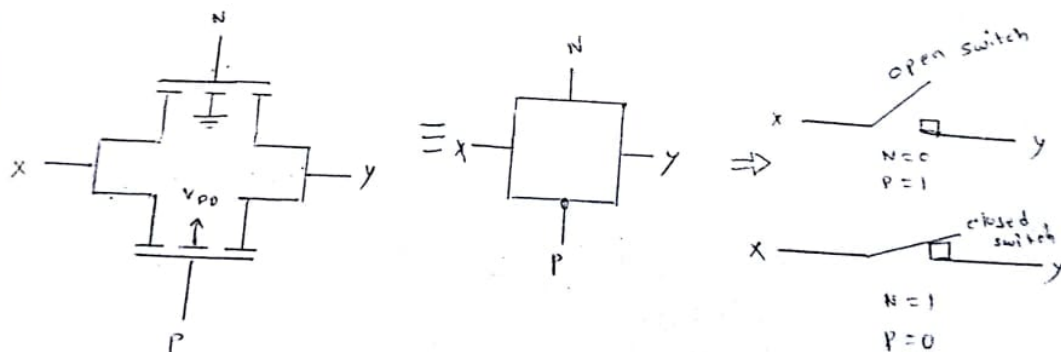
→ The SPP provides a basis for the comparison of logic ckt's, when both propagation delay and power dissipation are important. Smaller the SPP it give better performance.

$$\text{Speed Power Product} = \text{Propagation delay} \times \text{Power Dissipation}$$

units :- picojoule (pJ).

CMOS Transmission Gate:-

- Transmission gate is a special case of CMOS circuit which is not available in other digital logic families.
- The transmission gate acts as an electronic switch which is controlled by an input logic level.
- The basic structure of a transmission gate consists of one n-channel and one p-channel MOS transistor connected in parallel.
- Transmission gates are used for simplifying the construction of various digital components.



- If the n-channel substrate is connected to V_{DD} and the p-channel substrate is connected to ground, in this case the n-channel and p-channel MOS transistors are in conducting (closed switch).
- If we change i.e., by connecting p-gate to V_{DD} & n-gate to ground, two transistors will be turned into off then open switch.

(A) Comparison b/w various logic families

(B) Comparison b/w CMOS and TTL

Sl. No.	Parameter	CMOS	TTL
1	Number of transistors	MOSFET, 2	Discrete transistors
2	V_{DD} (max)	3-15V	5V
3	V_{OH} (max)	1.5V	2.8V
4	V_{OL} (min)	0.1V	0.2V
5	V_{IH} (min)	0.7V	2.0V
6	V_{IL} (max)	0.3V	0.8V
7	High level noise margin (V_{OH})	1.4V	2.0V
8	Low level noise margin (V_{OL})	1.4V	0.6V
9	Noise Immunity	Better than TTL	Less than CMOS
10	Propagation Delay	70 ns	10 ns
11	Switching Speed	Less than TTL	Faster than CMOS
12	Power dissipation/gate	0.1mW	10mW
13	Speed power Product	0.7pJ	100pJ
14	Fan-out	50	10
15	Power Supply Voltage	3-15V	Fixed 5V
16	Unconnected inputs	CMOS I/p's should never be left unconnected.	Treated as logic 1
17	Application	Portable Instrument where battery supply is used.	Laboratory Instrument

Comparison b/w RTL, DCTL, TTL, ECL, CMOS & HTL families

No. Parameter	RTL	DCTL	TTL	ECL	CMOS	HTL
1 Components Used	Resistor & Transistor	Resistor & Transistor	Resistor, diode & Transistor	Transistor	Transistor	Transistor
2 Circuit	Simple	Simplest	Complex	Simple	Simple	Simple
3 Noise Margin [Noise Immunity]	Nominal	Nominal	Very Good	Good	Good	Good
4 Fan-out	Low (4)	Low (4)	more (10)	High (20)	High (20)	High (20)
5 Power dissipation in mW/gate	12	12	10	10	10	10
6 Basic Gate	NOR	NOR	NAND	NAND	NAND	NAND
7 Propagation delay in (ns)	12	10	10	10	10	10
8 SPP	High	High	High	High	High	High
9 No. of fans	High	High	High	High	High	High
10 clock rate in Hz	5	5	5	5	5	5
11 Application	Absolute	Absolute	Absolute	Absolute	Absolute	Absolute

Note: From above table we can say that,

- ECL is the fastest logic family.
- ECL and TTL families have higher power consumption.
- CMOS family has lowest power consumption.
- CMOS family has highest fan-out.

⊗ IC Interfacing :-

Interfacing means connecting the output(s) of one circuit (or) system to the input(s) of another circuit (or) system that may have different electrical characteristics.

→ When two circuits have different electrical characteristics direct connection cannot be made.

→ In such cases driver and load circuits are connected through interface circuit.

→ Its function is to take the driver's output signal and condition it so that it is compatible with requirements of the load.

One must consider following important points while interfacing two ckt's (or) systems.

→ The driver's output must satisfy the voltage and current requirements of the load circuit.

→ The driver & load ckt may require different power supply. In such cases the output of both ckt must swing b/w specified voltage ranges.

TTL Driving CMOS :-

→ In this ckt TTL is a driver ckt and CMOS is a load ckt. The two ckt's are from different families with different electrical characteristics.

→ Therefore, we must check that the driving device can meet the current and voltage requirements of the load device.

Parameters	CMOS		TTL		
	4000B	74HC/ACT	74	74LS	74AS
$I_{IH(max)}$	1 μA	1 μA	40 μA	20 μA	200 μA
$I_{IL(max)}$	1 μA	1 μA	1.6 mA	0.4 mA	2 mA
$I_{OH(max)}$	0.4 mA	4 mA	0.4 mA	0.4 mA	2 mA
$I_{OL(max)}$	0.4 mA	4 mA	16 mA	8 mA	20 mA

Table. Input/output currents for standard devices with supply Voltage of 5V

→ Above Table indicates that the i/p current values for CMOS are extremely low compared with the o/p current capabilities of any TTL series.

→ Thus, TTL has no problem meeting the CMOS i/p current requirements.

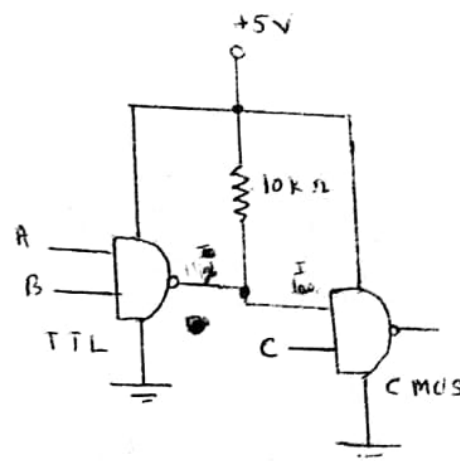


Figure: TTL driving CMOS using External Pull-up Resistor

But when we compare the TTL o/p voltages with the CMOS o/p voltage requirements we find that

V_{OH} of TTL is less than V_{OH} of CMOS for these situations.

TTL o/p must be raised to an acceptable level for CMOS.

This can be done by connecting pull-up resistor at the o/p of TTL (see circuit in the fig (a)).

The pull-up resistor causes the TTL o/p to rise to approximately V_{CC} in the High state, thereby providing an adequate CMOS o/p voltage level.

TTL Driving High voltage CMOS:-

When o/p CMOS ckt is operating with V_{DD} greater than 5V, the situation becomes more difficult. The o/p's of many TTL devices can't be operated at more than 5V. In such cases some alternative arrangement are made.

Case (i):-

When the TTL o/p cannot be pulled up to V_{DD}, one can use open collector buffer as an interface b/w totem-pole TTL o/p and CMOS operating at V_{DD} > 5V.

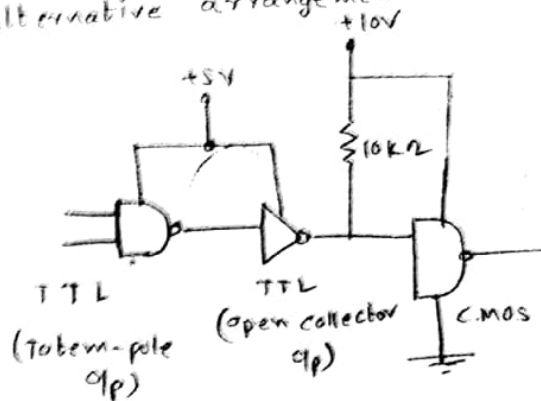


Fig (b). Open collector buffer used as interface circuit

Case (ii):- The second alternative is to use level translator ckt, such as the 40104. This is a

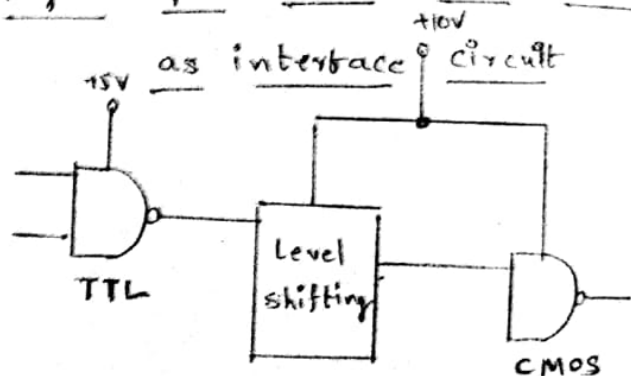


Fig (c). Level shifter used as interface ckt

CMOS chip that is designed to take a low-voltage i/p (e.g., from TTL) and translate it to high voltage o/p for CMOS.

⑧ CMOS Driving TTL :-

① In the HIGH state :-

→ Voltage parameters show that CMOS o/p's can easily supply enough voltage (V_{OH}) to satisfy the TTL i/p requirement in the HIGH state (V_{IH}).

For CMOS(4000B)	For TTL
$V_{OH(min)} = 4.95V$	$V_{IH(min)} = 2.0V$
$V_{OL(max)} = 0.05V$	$V_{IL(max)} = 0.8V$
$I_{OH(max)} = 0.4mA$	$I_{IH(max)} = 40\mu A$
$I_{OL(max)} = 0.4mA$	$I_{IL(max)} = 1.6mA$

Table. Voltage Parameters

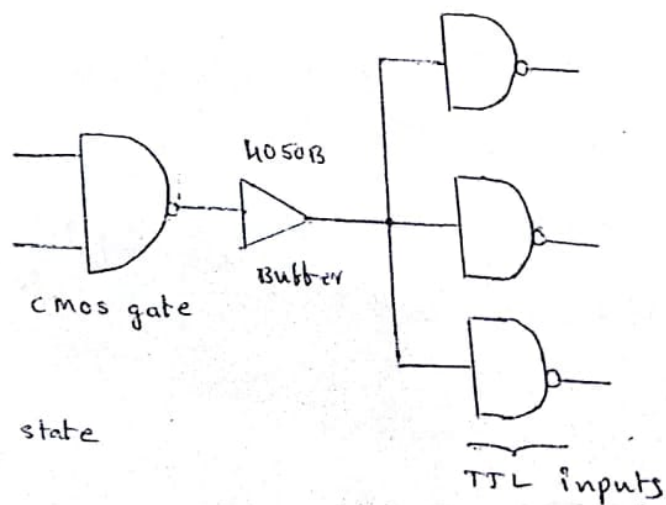
→ The parameters also show that CMOS o/p's can supply more than enough current (I_{OH}) to meet the TTL i/p current requirements (I_{IH}). Thus no special consideration is required for CMOS driving TTL in the HIGH state.

(ii) In Low state :-

→ The parameter in the Table show that CMOS o/p voltage (V_{OL}) satisfies TTL i/p requirement in the Low state (V_{IL}).

→ However, the current requirements in the Low state are not satisfied.

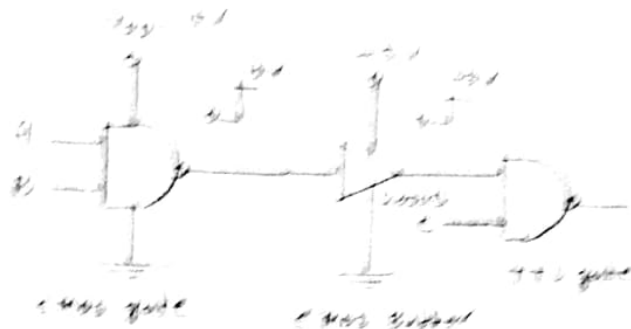
Fig. (d). CMOS driving TTL in Low state Using Buffer



- The 741 is a bipolar op-amp. It is a differential amplifier with two inputs, one inverting and one non-inverting. It has a high input impedance and a low output impedance. It is a voltage-controlled voltage source (VCVS).
- The 741 is a bipolar op-amp. It is a differential amplifier with two inputs, one inverting and one non-inverting. It has a high input impedance and a low output impedance. It is a voltage-controlled voltage source (VCVS).
- The 741 is a bipolar op-amp. It is a differential amplifier with two inputs, one inverting and one non-inverting. It has a high input impedance and a low output impedance. It is a voltage-controlled voltage source (VCVS).

4.1.5.1 Voltage level shifting - TTL

- Some of the most common logic devices are the 741 and the 7401. These devices are designed to operate at a supply voltage of 5V.

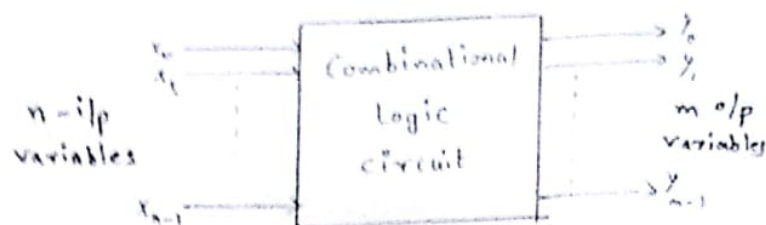


- These devices can be driven directly from a 5V supply operating at $V_{DD} = 5V$.
- However, most TTL I/O's cannot handle more than 7V and so a buffer is necessary if they are to be driven from high-voltage sources. In such situations voltage level translators are used.
- They convert the high voltage I/O to a 5V I/O that can be connected to TTL.
- Figure shows how the 4050B can be used to perform this level translation b/w 15V and 5V.

Combinational Logic I.C's

Introduction :-

When logic gates are connected together to produce a specified o/p for certain specified combinations of i/p variables, with no storage involved, the resulting ckt is called combinational logic.



Fig(a) Block diagram of a combinational circuit

⊕ Code Converters :-

There is a wide variety of Binary codes used in digital systems. Some of these codes are Binary-Coded-Decimal (BCD), Excess-3 (XS3), Gray and so on. Many times it is required to convert one code to another.

→ Let us see the Procedure to design code converters

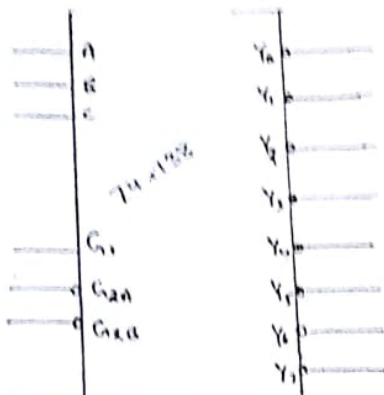
step 1 :- Write truth table showing the relationship b/w i/p code and o/p code.

step 2 :- For each o/p code bit determine the simplified Boolean expression using k-map

step 3 :- Realize the code converter Using logic gates

- | | |
|-----------------|---------------|
| ① BCD to XS3 | ③ BCD to Gray |
| ② Binary to BCD | ④ Gray to BCD |

74x138 3 to 8 Decoder



→ It accept 3 binary i/p's (A, B, C)
and when enabled, provides 8
individual active low o/p's ($\bar{Y}_0 - \bar{Y}_7$).

→ Decoder device has 3 enables:
2 active low ($\bar{G}_{2A}, \bar{G}_{2B}$) and
1 active high (G_1)

Inputs						Outputs							
$\bar{G}_{2B}$	$\bar{G}_{2A}$	G_1	C	B	A	$\bar{Y}_7$	$\bar{Y}_6$	$\bar{Y}_5$	$\bar{Y}_4$	$\bar{Y}_3$	$\bar{Y}_2$	$\bar{Y}_1$	$\bar{Y}_0$
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	0
			0	0	1	1	1	1	1	1	1	0	1
			0	1	0	1	1	1	1	1	0	1	1
			0	1	1	1	1	1	1	0	1	1	1
			1	0	0	1	1	1	0	1	1	1	1
			1	0	1	1	1	0	1	1	1	1	1
			1	1	0	1	0	1	1	1	1	1	1
			1	1	1	0	1	1	1	1	1	1	1

(X) LEI

B.

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→ H.

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D

* LED and LCD decoders with 74145 (a)

BCD to Seven Segment Decoder

→ In most practical applications, seven segment displays are used to give a visual indication of the status of digital data such as decade counters, latches etc.

→ These d/p's are usually in 4 bit BCD form, and are thus not suitable for directly driving seven segment displays.

→ Here, we are going to study LED and LCD decoder for 7 segment display.

Key seven
segment
display



Digit	segment Activated	display
0	a, b, c, d, e, f	
1	b, c	
2	a, b, d, e, g	
3	a, c, d, f, g	

→ If 7-segment display is common Anode the segment driver d/p must be active low as shown.

→ If 7-segment display is common cathode the segment driver d/p must be active high as shown.

Ex (1) for BCD to Common Cathode 7-segment display

Digit	A B C D	a	b	c	d	e	f	g
0	0 0 0 0	1	1	1	1	1	1	0
1	0 0 0 1	0	1	1	0	0	0	0
2	0 0 1 0	1	1	0	1	0	0	1
3	0 0 1 1	1	0	0	1	0	1	1
4	0 1 0 0	1	0	1	0	1	1	0
5	0 1 0 1	1	0	1	1	1	0	0
6	0 1 1 0	1	0	1	1	1	1	0
7	0 1 1 1	1	0	1	0	0	0	0

Ex (2) for BCD to Common Anode 7-segment display

Digit	A B C D	a	b	c	d	e	f	g
0	0 0 0 0	0	0	0	0	0	0	1
1	0 0 0 1	1	0	0	0	0	0	0
2	0 0 1 0	0	0	1	0	0	0	0
3	0 0 1 1	0	1	0	0	0	1	0
4	0 1 0 0	0	1	0	1	0	0	0
5	0 1 0 1	0	1	0	1	1	0	0
6	0 1 1 0	0	1	0	1	1	1	0
7	0 1 1 1	0	1	0	0	0	0	0

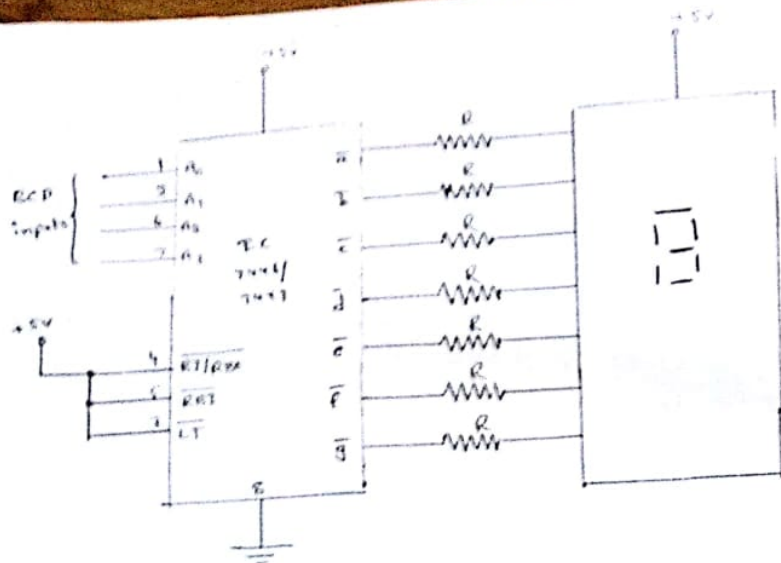


Fig. ckt for driving single seven segment display using 7446/7447

(X) Encoder :-

→ An encoder is a digital ckt that performs the inverse operation of a decoder.

→ An encoder has 2^n (or fewer) i/p lines and n o/p lines.

→ In encoder the o/p lines generate the binary code corresponding to the i/p value.

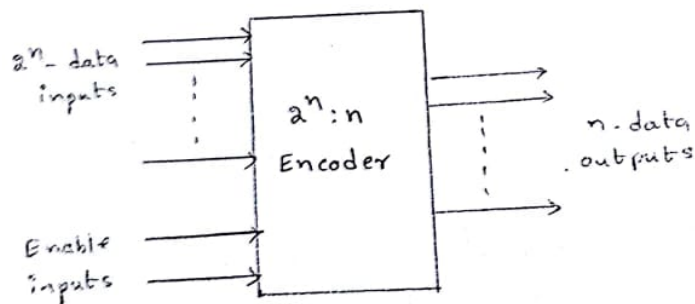


Fig. General structure of Encoder

① Priority Encoder :-

→ A priority encoder is an encoder ckt that includes the priority function.

→ In priority to 1 priority

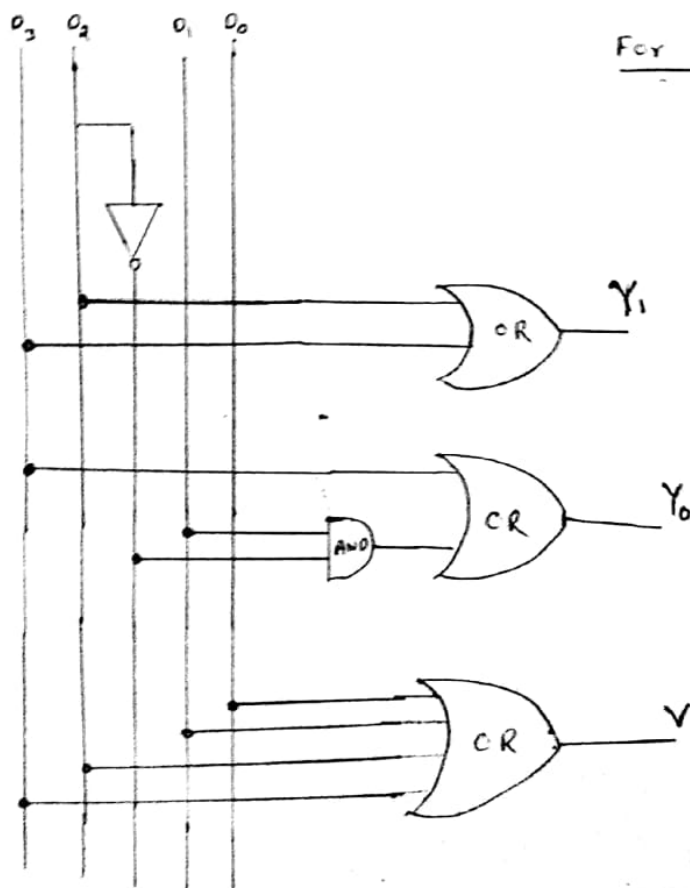
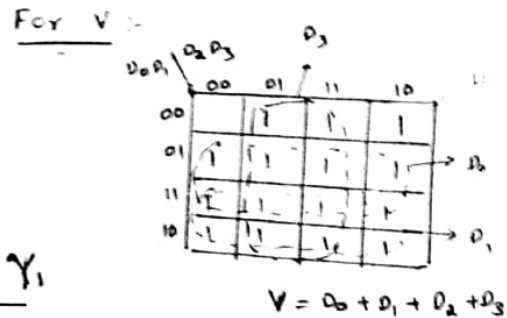
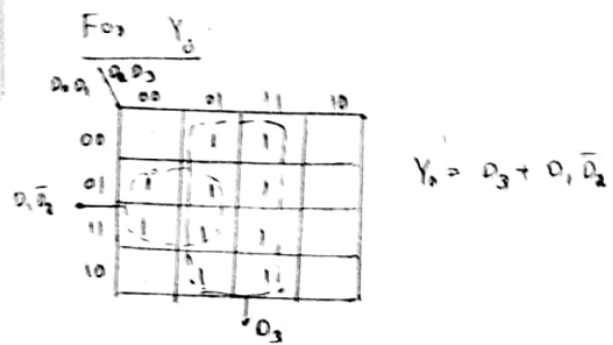
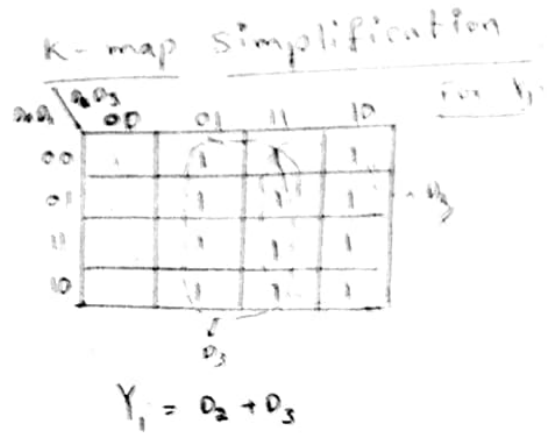
Input	
D ₀	D ₁
0	0
1	0
x	1
x	x
x	x

Table.

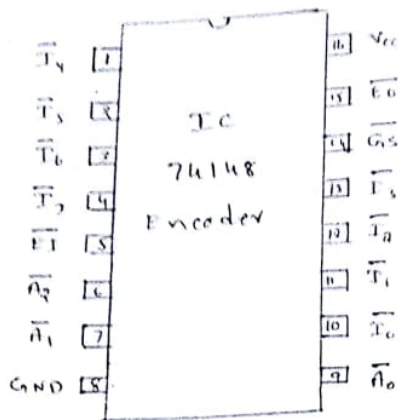
* In priority encoder, if two or more i/p's are equal to 1 at the same time, the i/p having the highest priority will take precedence.

Inputs				Outputs		
D_0	D_1	D_2	D_3	Y_1	Y_0	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Table. Truth Table of
4-bit Priority Encoder.



Priority Encoder IC (74148):



where

$\bar{I}_0 - \bar{I}_7 \rightarrow$ Active low i/p

$\bar{I}_0 \rightarrow$ Least Priority

$\bar{I}_7 \rightarrow$ highest "

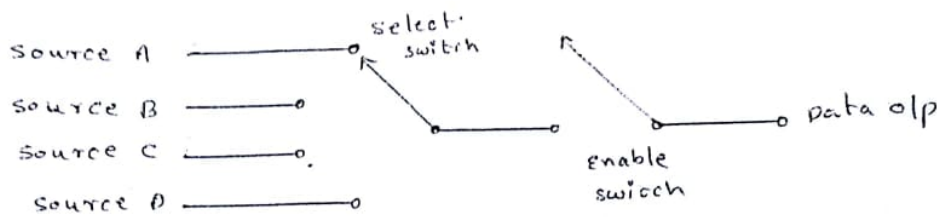
$\bar{A}_0 - \bar{A}_2 \rightarrow$ Active low o/p

$\bar{EI} \rightarrow$ active low Enable Input

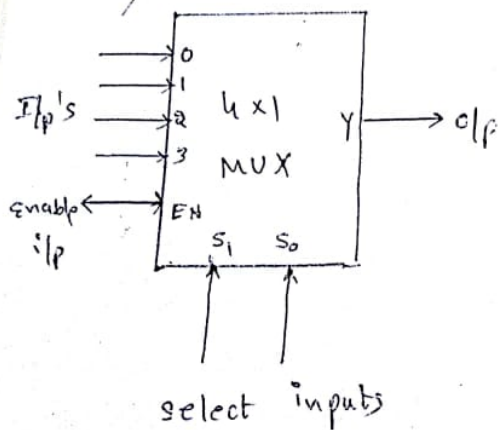
$\bar{EO} \rightarrow$ " " output

$\bar{GS} \rightarrow$ " " Ground signal

(A) Multiplexers :-



Fig(a) Analog selector Switch



select inputs

Fig(b) Logic System

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Fig(c). Function Table



Fig (11) 4-to-1 Multiplexer

It is a digital switch.
Digital combination from several sources as per
an n input output line.
multiplexer has several data input lines and
output line.

Where a particular input line is, controlled
by selection lines.

m input lines and n selection lines whose
combination determines which input is selected.

Multiplexer is "many into one" and it provides
equivalent of an analog selector switch.

1 to 1 mux

2 to 1 mux

4 to 1 mux

74157 → Quad 2-Input mux

74159 → 2-to-4 decoder

Applications of Multiplexers:-

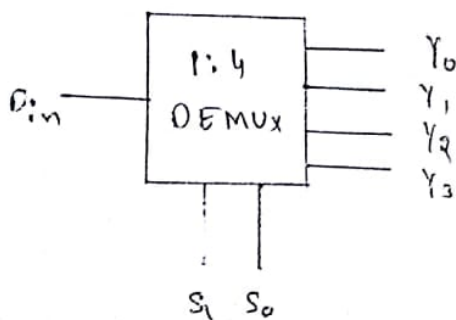
- ① They are used as a data selector to select one out of many data inputs.
- ② They can be used to implement combinational logic circuits.
- ③ They are used in time multiplexing systems.
- ④ They are used in frequency multiplexing systems.
- ⑤ They are used in A/D and D/A converter.
- ⑥ They are used in Data Acquisition systems.

(*) Demultiplexers:-

A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible o/p lines.

→ The selection of specific o/p line is controlled by the values of n selection lines.

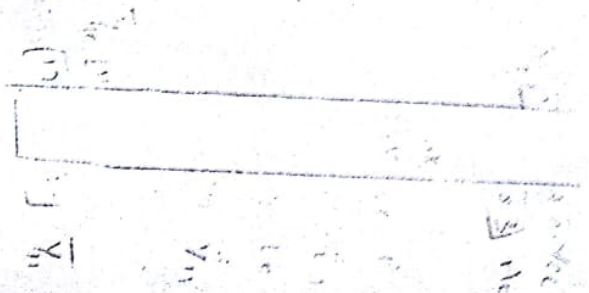
Ex:- 1:4 Demultiplexer:



Logic Symbol

Ex:-

- ① 74154 → 1:16 DEMUX
- ② 74138 → 1:8 DEMUX
- ③ 74156 → 1:4 DEMUX



(*) Priority Generators and Checkers

IC 74180: Priority Generator/Checker

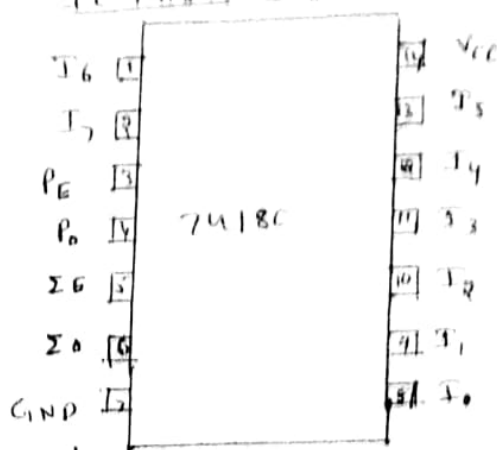
→ A parity bit is used for the purpose of detecting errors during transmission of binary information.

→ A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even.

→ The message, including the parity bit is transmitted and then checked at the receiving end for errors.

→ An error is detected if the checked parity does not correspond with the one transmitted.

→ The ckt that generates the parity bit in the transmitter is called a parity generator and the ckt that checks the parity in the receiver is called a parity checker.



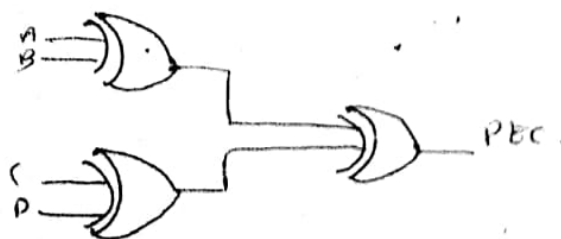
Pin Diagram

$P_E \rightarrow$ Even Parity Enable i/p

$P_0 \rightarrow$ odd " " "

→ The 74180 is a 9-bit parity generator (or) checker commonly used to detect errors in high speed data transmission (or) data retrieval systems.

→ Both even and odd parity enable i/p's and parity o/p's are available for generating (or) checking parity on 8-bits.



→ In even parity the added parity bit will make the total no. of 1's an even amount.

→ In odd parity the added parity bit will make the total no. of 1's an odd amount.

Ex:- 3 bit message with even parity and odd parity

3-bit Message			Odd Parity Bit	Even Parity Bit
A	B	C		
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

Let us Design Even Parity Generator:

A	BC			
	00	01	11	10
0		1 ₁		1 ₂
1	1 ₄		1 ₃	

$$P = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

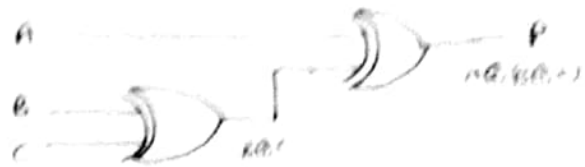
$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$

$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$

$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$

$$= A \oplus (B \oplus C)$$

$$A \oplus B \oplus C = S$$



(*) Parallel Binary Adder/Subtractor - can 4-bit binary

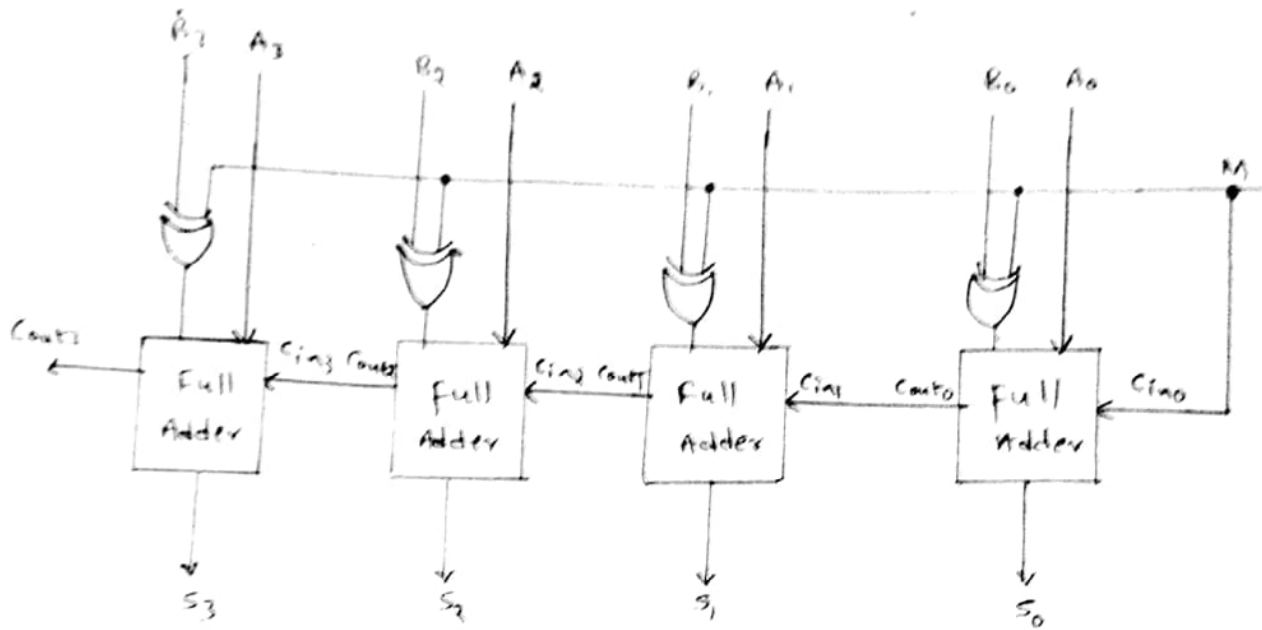


Fig. 4-bit Adder/Subtractor

→ The addition and subtraction operations can be combined into one ckt with one common binary adder. This is done by including an exclusive-OR gate with each full-adder.

→ The mode input (M) controls the operation of the ckt.

• When $M=0$, the ckt is an adder, and
 " $M=1$ " " " " subtractor

→ Each exclusive-OR gate receives i/p M and one of the i/p's of B.

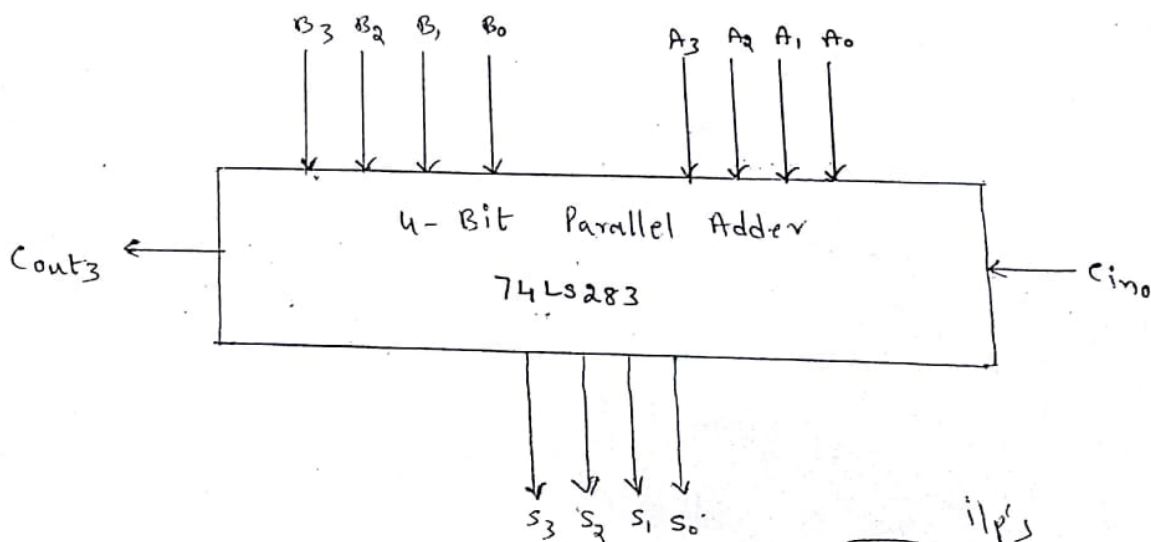
→ When $M=0$, we have $B \oplus 0 = B$.

The full-adders receive the value of B, the i/p carry is 0 and the ckt performs A plus B i.e., $A+B$.

→ When $M=1$, we have $B \oplus 1 = \bar{B}$ and $C_{in0}=1$.

The B i/p's are all complemented and a 1 is added through the i/p carry. The ckt performs the operation A plus 2's complement of B i.e., $A-B$.

IC example:- 7483/74283

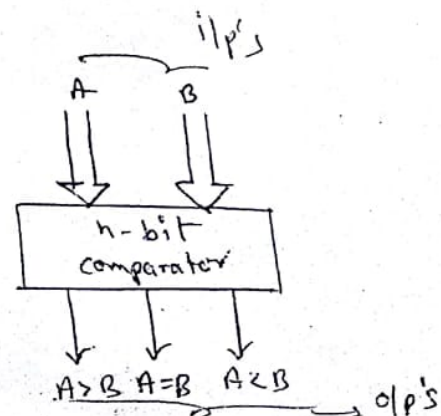


(*) Magnitude Comparator:-

IC examples:-

7485 → 4-bit comparator

74x682 → 8-bit "

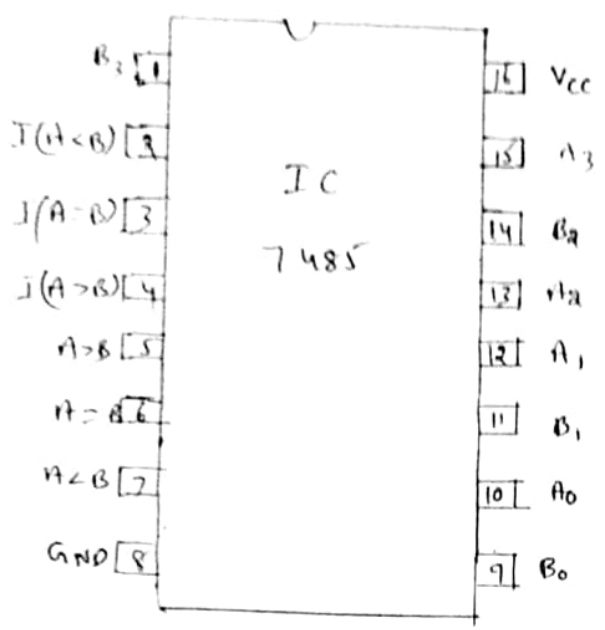


IC 74

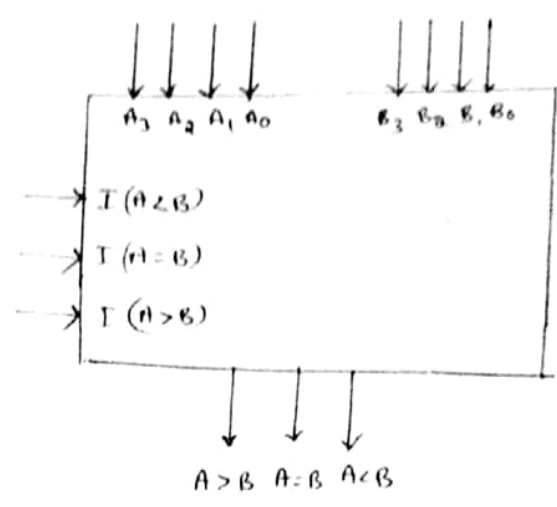
B ₃	1
I(A < B)	3
I(A = B)	3
I(A > B)	4
A > B	5
A = B	6
A < B	7
GND	5

Fig.
Cov

IC 7485 (4-bit comparator) :-



Fig(a). Pin diagram



Fig(b). Block diagram

Comparing i/p's	Cascading I/p's			Outputs		
	$I(A > B)$	$I(A = B)$	$I(A < B)$	$A > B$	$A = B$	$A < B$
$A > B$	X	X	X	1	0	0
$A = B$	1	0	0	1	0	0
	X	1	X	0	1	0
	0	0	1	0	0	1
	0	0	0	1	0	1
	1	0	1	0	0	0
$A < B$	X	X	X	0	0	1

Table. Function table for IC 7485

⊗ Specification & Application of TTL - 74xx Series IC & CMOS - 40xx series

CMOS series :- The two categories of CMOS in terms of ^{supply} DC voltage are the 5V CMOS and 3.3V CMOS.

→ The prefix 74 indicates commercial grade for General use.
" " 54 " Military grade " use.

The Basic CMOS series for 5V category

- ① 74HC & 74HCT → High speed CMOS (T indicates TTL)
- ② 74HC & 74HCT → Advanced CMOS
- ③ 74AHC & 74AHCT → Advanced High speed CMOS.

The Basic CMOS series for 3.3V category

- ① 74LV — Low voltage
- ② 74LVC — Low voltage CMOS
- ③ 74ALVC — Advanced low voltage CMOS

TTL Series :-

- ① 74 → Standard TTL
- ② 74S → Schottky TTL
- ③ 74AS → Advanced Schottky TTL
- ④ 74LS → Low power Schottky TTL
- ⑤ 74ALS → Advanced low-power Schottky TTL
- ⑥ 74F → Fast TTL

LDICA

UNIT-V

UNIT-V (Sequential logic IC's & memories)

Va

Familiarity with commonly available 74xx and CMOS 40xx

Series ICs — All types of Flip-flop

- Synchronous Counters
- Decade counters
- Shift Registers

V(b)

Memories

Rom Architecture.

Types of Rom's & Applications

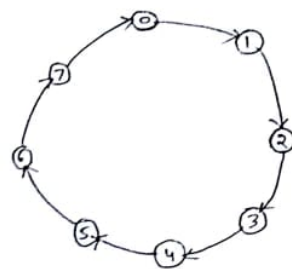
Ram Architecture

static and Dynamic RAMs

* Synchronous Counter :-

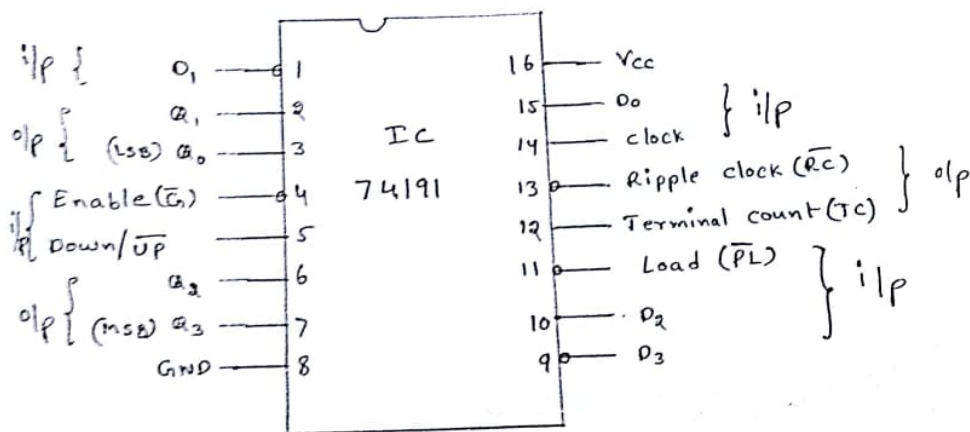
→ When counter is clocked such that each flip-flop in the counter is triggered at the same time, the counter is called "synchronous counter."

→ A 3-bit counter goes through stages : 0, 1, 2, 3, 4, 5, 6, 7 and again 0.



state diagram

Synchronous Counter (IC 74191) :-



Pin description :-

- ① Data Inputs :- D_0, D_1, D_2 and D_3 are the four data input lines with D_0 is LSB and D_3 is MSB. We can load data through these lines.
- ② $\overline{PL}$ (Parallel load) :- On activation of this signal (active low) the data available on data inputs (D_0, D_1, D_2, D_3) is loaded into the counter and it is then available on output lines. The Parallel load operation has higher priority than counting operation.

- ③ Enable ($\bar{G}$) Input :- When this signal is low, counting is enabled and count is incremented (or) decremented according to status of Down/ $\bar{U}$ P signal on each low to high transition of clock pulse applied to clock input. High on this input disables counting.
- ④ Outputs :- Q_0, Q_1, Q_2 and Q_3 are the four output lines with Q_0 is LSB and Q_3 is MSB.
- ⑤ Down/ $\bar{U}$ P :- This signal determines the direction of the counting. When this signal is high counter acts as a down counter; otherwise it acts as a up counter.
- ⑥ CP (clock) :- This is the clock input for the counter.
- ⑦ Terminal Count (TC) :- As soon as the counter reaches its maximum (1111) or minimum (0000) count this signal goes high for one clock pulse.
- ⑧ Ripple clock ($\bar{RC}$) :- This is an active low output signal. It is used as the clock input for the next higher stage.

Decade Counter :- It is also called MOD-10 counter,
(module - 10)

Here, we will not use clear input to reset the counter after state 1010.

Present state					Next state		
(A ₀)	(A ₁)	(A ₂)	(A ₃)	(A ₄)	(A ₅)	(A ₆)	(A ₇)
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

⊗ Shift Registers:-

- The group of flip-flops can be used to store a word, which is called "register".
- A flip-flop can store 1-bit information, so an n-bit register has a group of n-flip-flops and is capable of storing any binary information/number containing n-bits.
- The binary information (data) in a register can be moved from stage to stage within the register (or) into (or) out of the register upon application of clock pulses.
- This type of bit movement (or) shifting is essential for certain arithmetic and logic operations used in microprocessors.
- This gives rise to a group of registers called "shift registers".
- They are very important in applications involving the storage and transfer of data in a digital system.

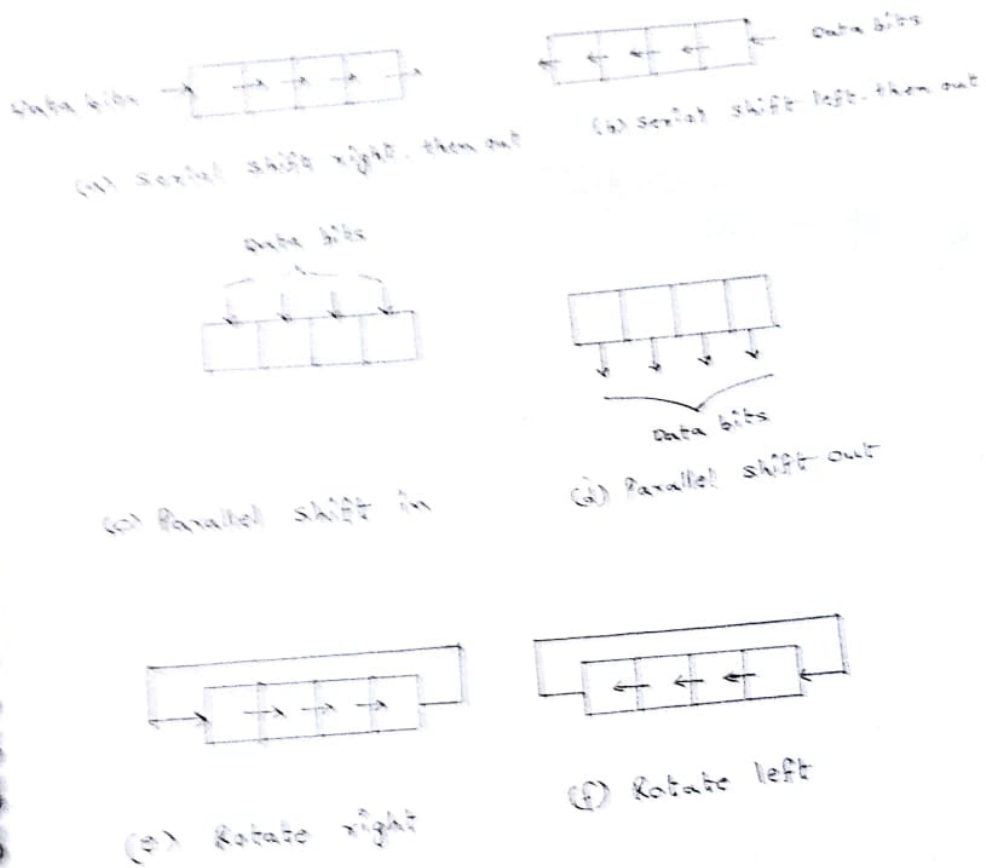
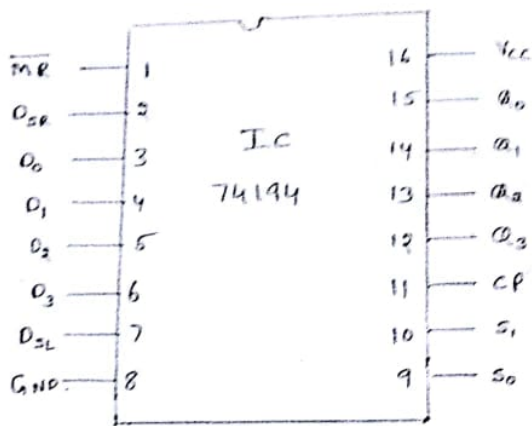


Fig. Basic data movement in registers

Modes of operation of shift registers :-

- ① Serial In serial out (SISO) shift registers
- ② Serial In parallel out (SIPO) " "
- ③ Parallel In serial out (PISO) " "
- ④ Parallel In parallel out (PIPO) " "

Universal Shift Register (IC 74194) :-



$MIO \rightarrow$ Memory (active low)
 $D_{SR} \rightarrow$ Shift Right serial I/p
 $D_{SL} \rightarrow$ " left " "
 $D_0 - D_3 \rightarrow$ 4 Parallel data lines
 $S_0 - S_1 \rightarrow$ Control inputs
 $O_0 - O_3 \rightarrow$ Outputs
 $CP \rightarrow$ clock Pulse

3) Familiarity with Commonly Available Txx and CMOS

40xx series IC - All types of Flip-Flop :-

SR - Flip-flop $\rightarrow$ $\frac{74XX}{7483}$

JK Flip-flop $\rightarrow$ 7473, 7476

Т flip-flop $\rightarrow$ 74HC74000

D flip-flop $\rightarrow$ 7479

$$\begin{array}{r} 40 \times 1 \\ \hline 4043 \end{array}$$

4027, 4095, 4096

74HC74

UNIT-V (b)

MEMORIES

Introduction :-

Memories are made up of registers. Each register in the memory is one storage location also called "memory location". Each memory location is identified by an "address".

The no. of storage locations can vary from a few in some memories to hundreds of thousand in others. Each location can accommodate one (or) more bits. Generally, the total no. of bits that a memory can store is its "capacity". Most of the types the capacity is specified in terms of bytes (group of eight bits).

Classification of Memory:-

Non-Volatile Memory		Volatile memory	
Read Only memory (ROM)	Read/Write memory (NVRAM)	Read/write memory (RWM)	
		Random Access	Non-Random Access
* Mask-Programmable ROM	* EPROM	* SRAM	* FIFO
* Programmable ROM	* EEPROM	* DRAM	* LIFO
	* FLASH		* Shift Register

ROM :- Read Only Memory

PROM :- Programmable ROM

EPROM :- Erasable PROM

EEPROM :- Electrically EPROM

RAM :- Random Access memory

SRAM :- static RAM

DRAM :- Dynamic RAM

FIFO :- First - In - First - Out

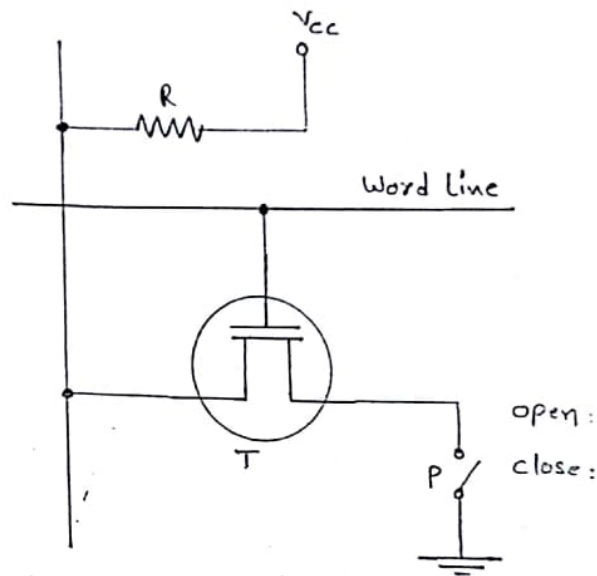
LIFO :- Last - In - First - Out

⊛ ROM Architecture :-

→ We can't write data in read only memories.

It is non-volatile memory i.e., it can hold data even if power is turned off.

→ Generally, ROM is used to store the binary codes for the sequence of instructions you want the computer to carry out and data such as look up tables. This is because this type of information does not change.



open : Data stored (logic 1)
close : Data stored (logic 0)

Fig. ROM cell

Store element one bit

→ Fig. shows the typical configuration of a ROM cell. It consist of a transistor T and switch P . The

transistor is driven by the word line. The contents of cell can be read from the cell where word line is logic 1. A logic value 0 is read if the transistor is connected to ground through switch P. If switch P is open, a logic value 1 is read. The bit line is connected through a resistor to the power supply.

⑤ Types of ROM's :- There are 3 types.

① PRoM (Programmable Read Only Memory) :-

PRoM are programmed by user. To provide the programming facility, each address select and data line intersection has its own MOSFET (or) Transistor.

② EPROM (Erasable Programmable Read Only Memory) :-

EPROMs can be programmed by the user with a special EPROM programmer. The important point is that we can erase the stored data in the EPROMs by exposing the chip to ultraviolet light through its quartz window for 15 to 20 minutes.

③ EEPROM (Electrically Erasable Programmable Read Only Memory) :-
EEPROM's also use mos circuitry very similar to that of EPROM.

The EEPROM memory also has a special chip erase mode by which entire chip can be erased in 10ms. This time is quite small as compared to time required to erase EPROM and it can be erased and reprogrammed with device right in the circuit. EEPROMs are most expensive.

* RAM Architecture:-

The memory in which the time taken to transfer information to (or) from any desired random location is always the same is called random access memory.

There are two types of RAMs: *static RAM *Dynamic RAM

Static RAM	Dynamic RAM
① Static RAM contains less memory cells per unit area.	① Dynamic RAM contains more memory cells as compared to static RAM per unit area.
② It has less access time hence faster memories.	② Its access time is greater than static RAMs.
③ Static RAM consists of no. of flip-flop. Each Flip-flop stores one bit.	③ Dynamic RAM stores the data as a charge on the capacitor. It consists of MOSFET & the capacitor for each cell.
④ Refreshing circuitry is not required.	④ Refreshing circuitry is required to maintain the charge on the capacitors after every few milliseconds. Extra h/w is required to control refreshing. This makes system design complicated.
⑤ Cost is more.	⑤ Cost is less.