# TOTE ENGINEERING OF THE WORLD THE WO

### SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Approved by AICTE, New Delhi, Affiliated to JNTUH, Hyderabad. [Formerly RVR Institute of Engineering & Technology] Sheriguda (V), Ibrahimpatnam (M), R. R. District, T.S – 501510.

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# MECHANISM TO DEAL WITH INTERNAL EXAMINATIONS RELATED GRIEVANCES IS TRANSPARENT, TIME-BOUND AND EFFICIENT.

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16X31A05E4	133BD	MATHEMATICS - IV	R16-2-1	29-NOV-21	11:45 AM TO 12:30 PM
16X31A05E4	134AK	COMPUTER ORGANIZATION	R16-2-2		11:45 AM TO 12:30 PM
16X31A05E4	136FG	INTELLECTUAL PROPERTY RIGHTS	R16-3-2	The state of the s	02:30 PM TO 03:15 PM
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16X31A05E4	136AW	CRYPTOGRAPHY AND NETWORK SECURITY	R16-3-2		02:30 PM TO 03:15 PM
16X31A05F8	137CA	DISTRIBUTED SYSTEMS	R16-4-1	The second second second second	04:30 PM TO 05:15 PM
16X31A05F8	137BQ	DATA MINING	R16-4-1	- Control Control Control	04:30 PM TO 05:15 PM
16X31A05G3	137BQ	DATA MINING	R16-4-1		04:30 PM TO 05:15 PM
16X31A05G3	137CA	DISTRIBUTED SYSTEMS	R16-4-1	The second second second	04:30 PM TO 05:15 PM
16X31A05G3	137GA	PRINCIPLES OF PROGRAMMING LANGUAGES	R16-4-1	-	04:30 PM TO 05:15 PM
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Sri Indu Institute of Engineering & Tech.
Sheriguda(V), Ibrahimpatnam(M).
R.R. Dist. Telangana 501 510.



#### JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD KUKATPALLY, HYDERABAD-500 085

III Year B. Tech-Special CBT I Semester/R09: ELECTRONICS AND COMMUNICATION ENGINEERING

HALLTICKET Original ECE

H.T.No. 12X31A04A0

Exam

Index Women's Engg. College - 02

P RAVIKUMAR

Name of the Student Father's Name

P YADAGIRI

Month and Year of Examination

Nov/Dec-2021



List of Theory Subjects Registered

SINo	Date of Exam	Subject Code	Subject Name	Session
1	21.12.2021	55009	IC APPLICATIONS	1
2	22:12:2021	55012	CONTROL SYSTEMS	- 3

SessionTimings: 1) 09:30am - 10:15am / 2f 11 45am - 12:30pm / 3) 02:30pm - 03:15pm / 4) 04:30pm - 06:15pm

Student Signature

Principal Signature NCIPAL

KirkaHoond to Controller of Examinations

1. All the students must be present in 6d 109H returning to the him of 50 the form of 50 the him of Soudents should not carry any other marginal Dear Half Ticket identity card
 Should not carry any other marginal Dear Half Ticket identity card
 Show Half Ticket and March 2019 palm computers making any

Programmative calculators paim computers mobile phones and pagers are not permitted into examination halls. They should show Hall Tricket and Identity card to the Invigrator/Coserver/Chief Superintendent whenever they are asked.

4. The University reserves the right to cancel the admission of the student at any stage when it is detected that higher admission to the examination of the college is against rules

NOTE: If there is any discrepancy in student photo or any other details, it should be brought to notice of the Controller of Examinations immediately.

COVID-19 Guidelines:

All the students must wear masks while they are on the campus.

2) Students must maintain social distancing as per Government guidelines in current scenario of COVID-19 to ensure health and safety of the Students.

Stude its must carry their own water bottles and hand sanitizers. Sharing of pens or any other stationary items among the students is snintly prohibited in the examinal.

4) Care and of the example students shall be permitted to move out in an orderly manner one candidate at a time. The students in bound not getup from their seats until advised by the invigitator.

5) Social most maintain silence while going to their alloted prain hall as well as inside the examination

E) This holi-ticket should be kept in open state beside your answer booklet whenever the room invigilator come to your place.



### JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD KUKATPALLY, HYDERABAD-500 085

IV Year B Tech-Special CBT | Semester R131-ELECTRONICS AND COMMUNICATION

HALLTICKET Original

ECE

Exam Centre

Sidevi Women's Engg. College - D2.

HT No. 14X31A04D4

- Name of the Student
- Father's Name
- Month and Year of Examination

SHIGA MANISHA SHIGA VEKATESH GOUD

Nov/Dec-2021



SINo	Date of Exam		Subject Name	
1	06 12 2021		CELLULAR AND MOBILE COMMUNICATIONS	Session
	14 12 2021			
. 0			MANAGEMENT SCIENCE	4
-0	21:12:2021	117FE	MICROVAVE ENGINEERING	4

SessionTimings: 1) 09:30am - 10:15am / 2) 11,45am - 12:30pm / 3) 02:30pm - 03:15pm / 4) 04:30pm - 05:15pm

5-Manisha

Student Signature

Principal Signature with Seal

White House has he Controller of Examinations

- All the students must be present in the contract to the commencement of examination to a skyling the share the commencement of examination to the skyling three three tracks and the skyling streams. The skyling streams will be skyling three tracks and the skyling streams.
- 1. All the students must be present in the expressibilities of the destinant. Ment of the examination and students who come after the commencement of examination by the property of the commencement of examination and students who come 2. Students should not carry any other **Shedrillings** the property of the commencement of examination halfs. They should show that Ticket and Identify card to the invigilator/Observer/Chief Superintendent whenever they are asked.
- 4. The University reserves the right to cancel the admission of the student at any stage when it is detected that his/her admission to the examination or the college is against rules.

NOTE: If there is any discrepancy in student photo or any other details, it should be brought to notice of the Controller of Examinations immediately.

#### COVID-19 Guidelines:

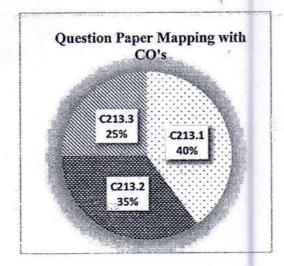
- 1) All the students must wear masks while they are on the compus.
- 2) Students must maintain social distancing as per Government guidelines in current scenario of COVID-19 to ensure health and safety of the Students
- 3) Students must carry their own water bottles and hand sanitizers. Sharing of pens or any other stationary items among the students is stream prohibited in the exam hell.
- 4) On completion of the exam, the students shall be permitted to move out in an orderly manner one candidate at a time. The students should not getup from their seats until advised by the imagrator
- Student must maintain silence while going to their alloted exam half as well as inside the exam half.
- 6) This half-licket should be kept in open state beside your answer booklet whenever the room invigilator come to your place

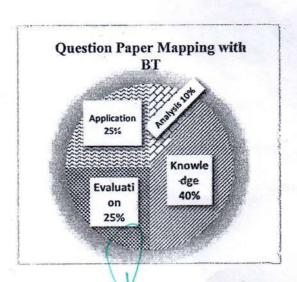
### Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 I- Mid Examinations, DEC-2020

Set-I

	r &Branch: II ECE(A ,B&C) ject: DSD	Max. Marks: 10			Date: 28/12/2020 (FN) Time: 60 mins		
Ans	wer any TWO Questions. All	Question Carry Eq	ual N	Marks	2*5=10		
mar	ks.						
1	Solve the following conversion (27.125) <sub>10</sub> = ( ) <sub>8</sub> b) $(1010100111.111001)_2$ =( c) $(237.75)_8$ = ( ) <sub>10</sub> d) $(735.5)_8$ = ( ) <sub>16</sub>		5	C213.1	(Evaluation)		
2	Apply the K-map method to Boolean function.  Y = AB+C+ACD+ABCD+C		5	C213.2	(Application)		
3		, for a given 4-bit	3	C213.1	(Knowledge)		
	B)Define the Encoder?Desig	n a 8*3 Encoder?	2	C213.2	(Knowledge)		
4	A)Define Sequential circuits types of sequential circuits?	and what are the	3	C213.3	(Knowledge)		
134	B)Differentiate Combination circuits	al and sequential	2	C213.3	(Analysis)		





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R.R. Dist. Telangana -501 510

### Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510
I- Mid Examinations, DEC-2020

Set - I

Year & Branch: II ECE A,B&C

Date:28/12/2020(FN)

Subject: DSD

Marks: 10

Time: 60 min

Answer any TWO Questions. All Question Carry Equal Marks

2\*5=10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

ANSWER KEY

$$(237.75)_{8}$$

$$= 7\times 8^{9} + 3\times 8^{9} + 2\times 8^{2} + 7\times 8^{9} + 5\times 8^{2}$$

$$= 7\times 1 + 24 + 2\times 64 + \frac{7}{8} + \frac{5}{64}$$

(Page 7 of 333) 10

d) 
$$(735.5)_8 = ()_{16}$$
  
 $735.5$   
111 011 101.101  
 $000111011101.1010$   
 $1 D D A$   
 $(1DD.A)_{16}$ 

2. Apply the k-map method to simplify the boolean function

Y= AB+C + ACD+ ABCD +CD

AB+C+ACD+ABCD+CD

[3M]

= AB(C+T) +C (A+A) +(B+B). (D+D) + ACD(B+B)+ABCD + CD(A+A)+(B+B)

= ABCD+ ABCD + ABCD+ ABCD + ABCD + ABCD + ABED.

= m15 + m14+m12+m13+m1+m3+m3+m10+m6+m2 ≤m (2,3,6,7,10,11, 12,13,14,15)

7 1	\$	
15	14	
13	AP AR	3
Φ 1	2	
	7 1 15 1	15 1 14 AC

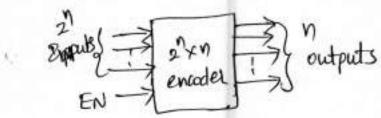
$$y = AB + C$$
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39) 7-bit hamming code for aginen 4-bit data 1110 [3M]

$$m = 1110$$
 $A = 1110$ 
 $A = 1100$ 
 $A =$ 

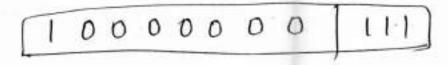
7Hoit hamming code is (1111000)

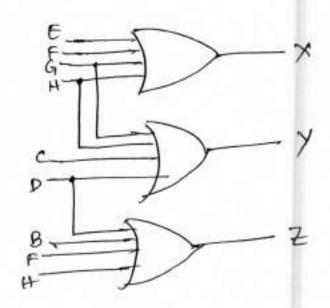
3b. Encoder: - encoder is a digital circuit It has 2<sup>n</sup> inputs and n outputs when enable signal is high only the operation is performed.



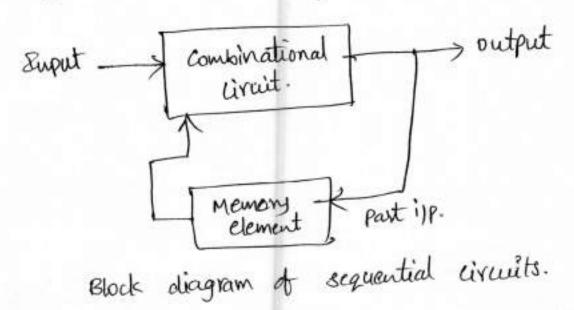
8X3 Encoderi- It how 8 inputs 3 outputs.

_	0	0	0 (	0 0	) (	0	1	0	0	0
0	0	0	0	0 1	0	1	O	0	0	)
0	0	0	0	0	1	0	0	0	١	0
0	0	0	0	1	0	0	0	0	1	
0	0	0	1	0	0	0	0	1	0	(
0	0	1	0	0	0	0	0	1	0	
0	1	0	0	0	0	age	9 of	33 (	1	1





49 sequential circuits: — It is a digital circuit. He output is depends on present inputs and past inputs. The past input data is stored in memory element.



Types of sequential circuits:

- . It is depends on their timming of their signals. They are two types.
- 1) synchronous sequential circuits
- 2, Asychronous sequential circuits.
- -> synchronous sequential circuits, are the signal can effect the memory elements at discrease instant of time.
- > Asynchronous sequential circuits the input of signal can effect the memory element at any instant of time.

# 46. Combinational circuits

1, En combinational circuits, the opp is depends on the present input variables.

- 2) Memory element is not required.
- 3, Easy to design

4) It is very faster than sequential circuits due to delay of variables.

ext parallel adder.

# sequential circuits.

- 1) In sequential, the output is depends on its present and past input variables.
- 2) Memory element is required to store input variables
- 8, comparatively harder to design.
- 4) It is slower than combinational circuits. ex: serial adder.

St Indu Institute of Engineering and St. 1510

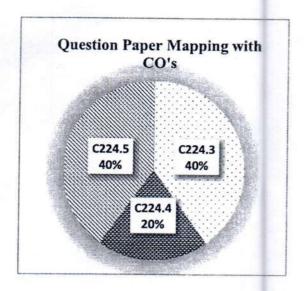
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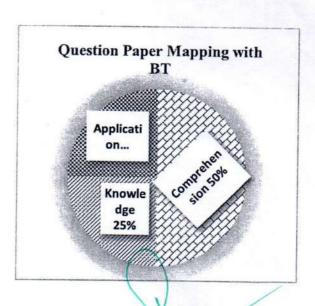
## Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510
II - Mid Examinations, JULY -2021

Set -I

	ar & Branch: II –ECE(A,B&C) bject:LINEAR IC APPLICATIONS	Max. Marks: 10		ate: 23/07/21(AN) me: 60 mins
	Answer any TWO Questions. All Questi	on Carry Equal Ma	irks	2*5=10 marks
1.	Draw the basic circuit of RC-Phase Shift Oscillator and explain its operation. Also derive the expression for frequency of oscillations.		(C224.3)	(Application)
2	Describe the working Operation of IC55. Timer PLL and in detail?	5 5	(C224.4)	(Knowledge)
3	Explain the working of R-2R ladder DAO neat circuit diagram	C with 5	(C224.5)	(Comprehension)
4	Explain the working of dual slope ADC neat circuit diagram	with 5	(C224.5)	(Comprehension)





PRINCIPAL

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## Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 II- Mid Examinations, JULY-2021

Set - I

Year & Branch: II ECE (A, B&C)

Date: 23/07/21 (AN)

Subject: LICA

Marks: 10

Time: 60 min

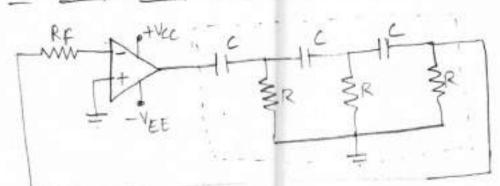
Answer any TWO Questions. All Question Carry Equal Marks

2\*5=10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

### ANSWER KEY

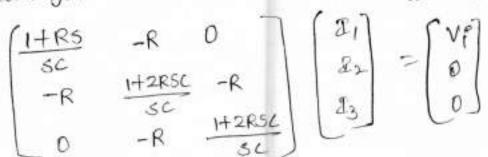
1. RC Phase shift oscillator:-



Samil

RC phase shift oscillator using op-amp in investing amp mode. thus, it produces the phase shift of 180° between if p & olp. The feedback now consist of three RC sections each producing 60' phase shift.

Apply EVL at the circuit; we can get the matrix format.



$$\Delta = \frac{1 + 6R^2 s^2 c^2 + 5Rsc + R^3 s^3 c^3}{s^3 c^3}$$
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1M

$$D_{3} = V_{1}^{2} R^{2}$$

$$I_{3} = \frac{\Delta_{3}}{\Delta} = \frac{ViR^{2}s^{3}c^{3}}{1+5Rsc+6R^{2}s^{2}c^{2}+s^{3}R^{3}c^{3}}$$

$$V_{0} = V_{f} = I_{3} \cdot R$$

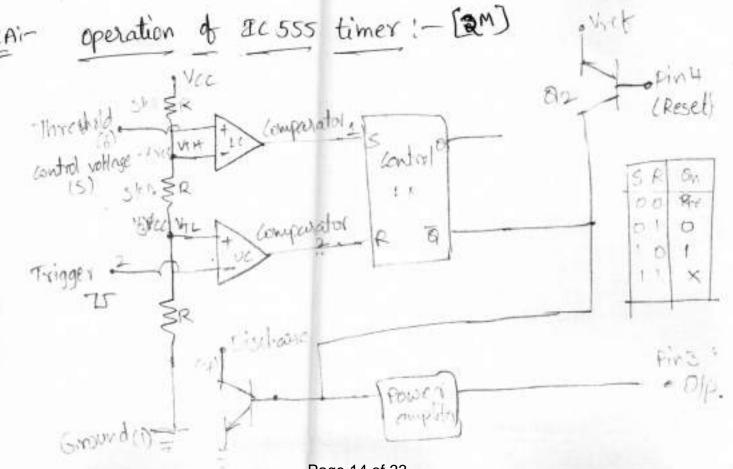
$$= \frac{1}{(1-s\lambda^{2})-j\lambda(6-\lambda^{2})}$$

$$= \frac{1}{(1-s\lambda^{2})-j\lambda(6-\lambda^{2})}$$

equate imaginary part & real parts equal to zero.

$$-j\chi(6-\chi^{2})=0$$
  
 $6-\chi^{2}=6$   
 $\chi^{2}=6$   
 $j=6$   
 $j=6$   

$$(1-5a^{2})=0$$
 [2M]  
 $1-5(6)=0$   
 $1-30$   
 $A = 29$   
 $1B) = 1A1$   
 $B = \frac{1}{29}$ 



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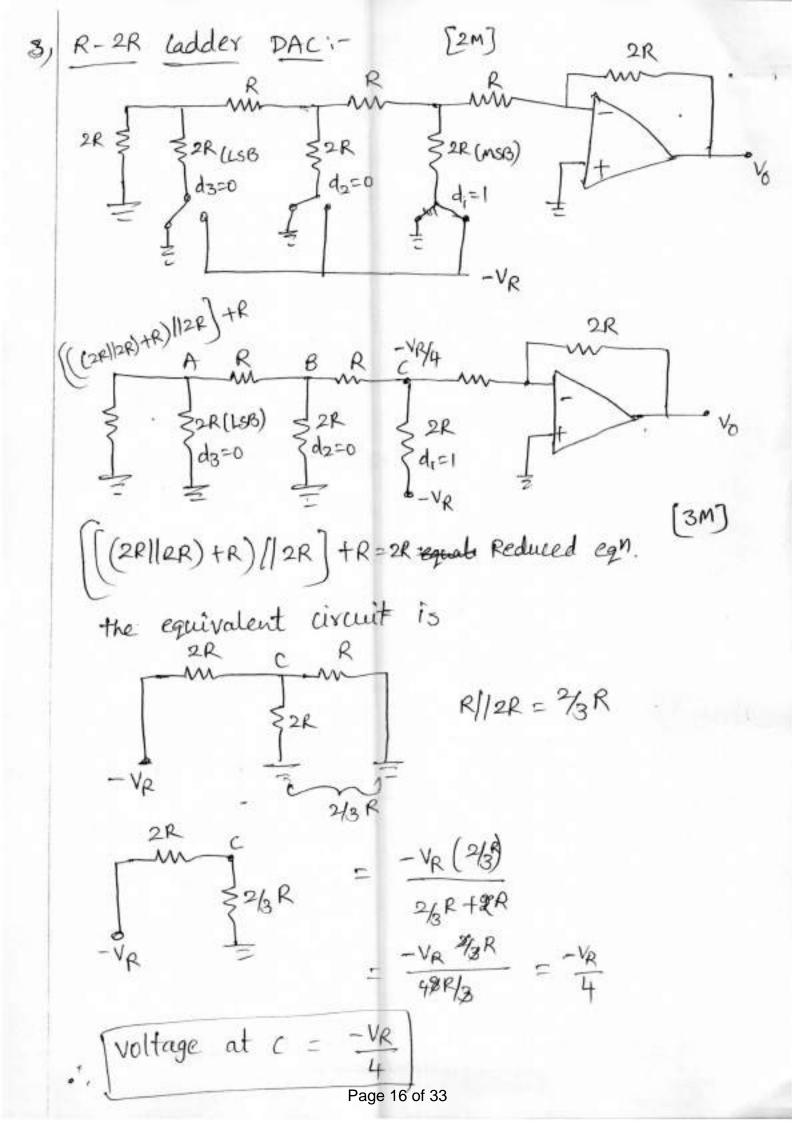
Pin1 (Ground): All the voltages are measured with [3M] respect to this terminal

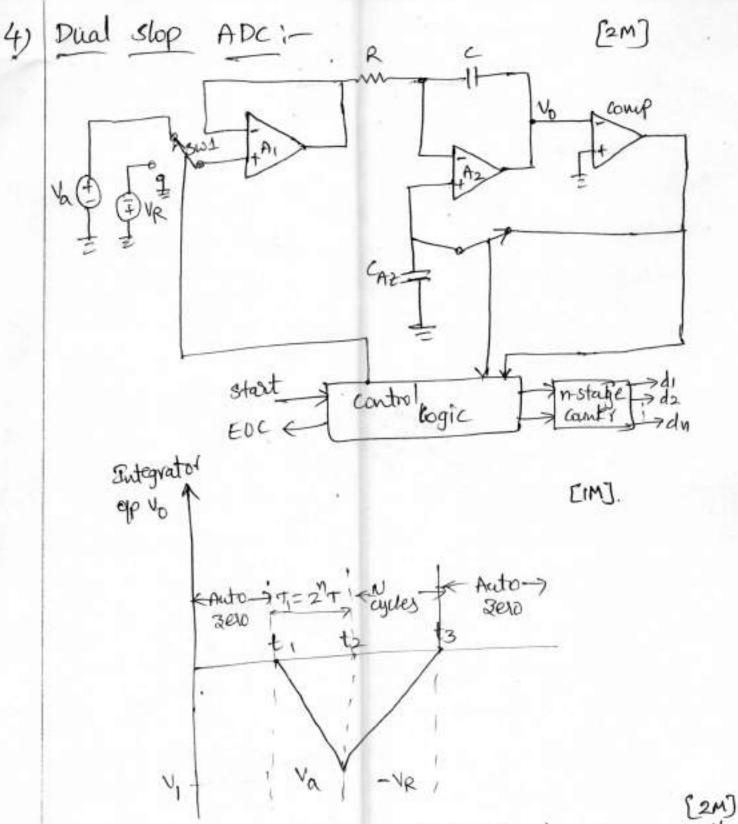
Pin2 (trigger): - The 8c 555 uses two comparators. the voltage divides consist of 3 equal resistances due to voltage divider. The inverting i/P of compartor-2 which is compared with vc/3. trigger i/P is slightly leasthan vcc/3. The comparator o/P goes high. The o/P is given to set i/P of the FF. so high o/P of comparator-2 resets the flipflop.

The non-inverting ip of comparator - 1. which is compared with 23 Vcc. The threshold voltage is greater than the 23 Vcc the comparator of goes how the of the Hiptop will be set state.

Pin 3 (Reset): - The complementary signal OIP (a) of the FF goes to pin3 which is the OIP. The load can be connected in two ways one bln pin3 to GNO. @pin3 to Ke connected in two ways one bln pin3 to GNO. @pin3 to Ke connected in two ways one bln pin3 to GNO. @pin3 to Ke connected in two ways one bln pin3 to GNO. @pin3 to Ke connected in two ways one bln pin3 to GNO pin3 to Ke timming driven pin4 (Reset): - This is an interpet to the timming driven when pin4 is connected to ground. It stopps the working of device and makes it off. The pin4 provides on (or) OFF.

An 7 (Dicharge): This pin is connected to collectors of the discharge transistor &1. when the old is high the B is low. The transistor &1 is OFF. It acts as open als to the external capacitor 'c' connected according to the external capacitor 'c'





The circuit consists at high i/p impedance butter A) & integrator A2 and comparator. The converter first integrates the analog i/p signal Va tor a fixed duration of 2" clock periods then it integrates reference voltage VR of opposite polarity until the integrator of is sero. The no. N of clock cycles page 17 of 33

propotional to the value of Va.

and sw2 is closed. Any obset voltage present in the A1, A2, comparator loop after integration, appears across the capacitances CAZ till the threshold of comparator is achieved.

PRINCIPAL PROPERTY IS 10.

# SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

SHERIGUDA (V), IBRAHIMPATNAM (M), RANGA REDDY DIST. - 501 510



Diploma / B. Tech

# CERTIFICATE

This is to Certify that Mr. / Ms S. Shivani'
Diploma / B. Tech Cle chronics Communication Engineering Branch, bearing the
H.T. No. 20x3540423 has satisfactorily completed 12 Experiments
in the TC Applications Lab laboratory as prescribed
Jawaharlal Nehru Technological University, State Board of Technical Education
and Training Hyderabad. During the Academic year 201 - 201
Lab-In-Charge
Head of the Department Lab-In-Charge

Practical date held on

12-08-2021

Signature of Internal Examiner

Signature of External Examiner

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SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Approved by AICTE, New Delhi. Affiliated to JNTUH, Hyderabad.
SHERIGUDA (V), IBRAHIMPATNAM (M), RANGA REDDY DIST. – 501 510

Department of Plectronics & Communication. Engineering INDEX

Espl. No.	Name of the Experiment	Date	Page No.	Remarks / Signature
1.	Introduction	26 0721	1-2	50H 28H 2LA
2.	Adder & Subtractor using TC741	jelfolac	and the same of the same of	श्रिच क्षिम्म वि
3.	IC 741 op-amp as a Inverting	26/07/21	6-8	क्रीनाय कि
4.		26/07/21	9-10	2012/9/12/ AT
	Integrator circuit using Ictul op-am	BRIDGE STREET, THE OWNER, THE	10 THE R. P. LEWIS CO., LANSING, MICH.	श्रिपेट्वीभीय (A+
6	Differentiator using retul op-amp			श्रिस्ट्याम् Aन
4.	Design of Active filters - UPF, HPF			श्रिक्त की मार्थ (AT
	wave form generation using ICTY! Operational Amplifier			क्रिसंज्ञामाथ वि
9.	Monostable Multivibrator using PC55	29/07/21	21-22	क्रिने डामिय मि
	Astable Multivibrator using 12555		23-24	204317721 AT
-11-	Schmitt Prigger Circuit using IC741	29/07/21	25-36	20 317121 AT
	Ic 565 - phase locked loop  Applications.	वनीवनीवा	27-30	18 21 AT
_13·	Voltage Regulator using 20723	39/04/21	31-35	845 8121 AT
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	Page 20 c	of 33		

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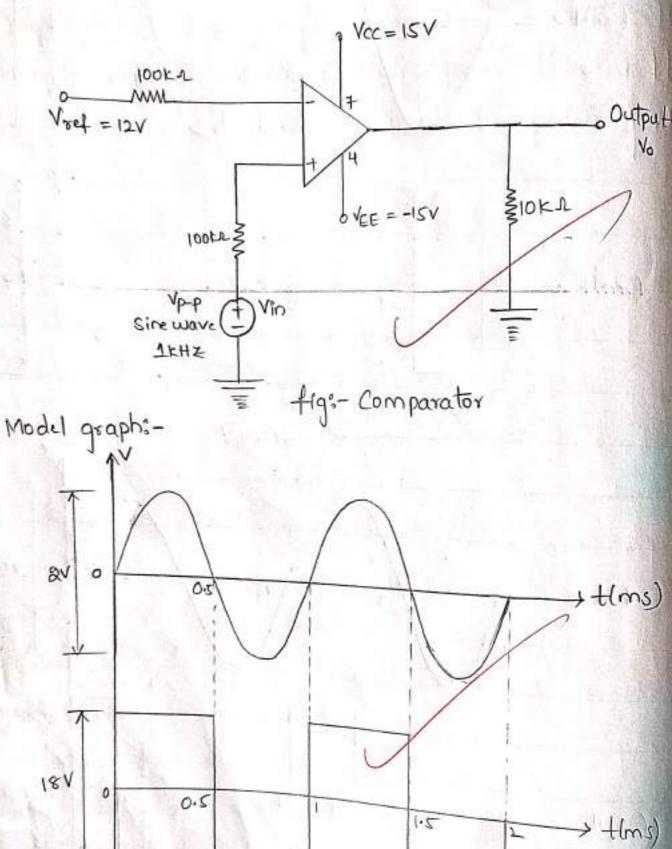
SI. No.	Date	No. of Periods	Brief Note of topic dealt	Signature of Head / Principal
1	21/4/204	3	manual worting	
2	2/4/204	1.3.	Amplitude modulation & Demodul.	groo)
3	104/2021	3	Frequency modulation & Demodul	green -
4	elstron	(2,1)	DEBISC modulator 2 Defector	· ·
5	SIGIROU	3	SSB-SC modulator & Detector.	
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9	2616	reason.	& pemultiplining	1 1
1	26/6/204	3	pulse Amplitude modulation & per	nadulation
8	3/7/2021	3	nulsewidth modulations permodulation	p p
9	10/7/24	3	rule position modulations permodulation	1 11
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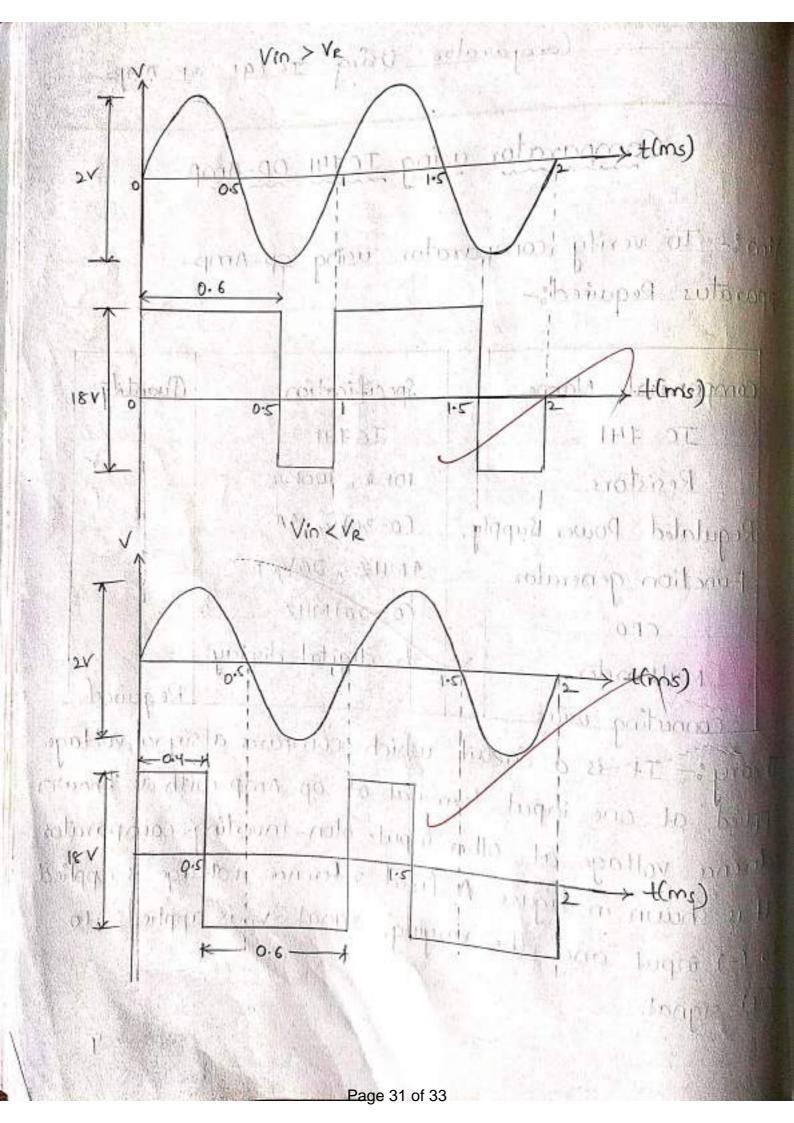
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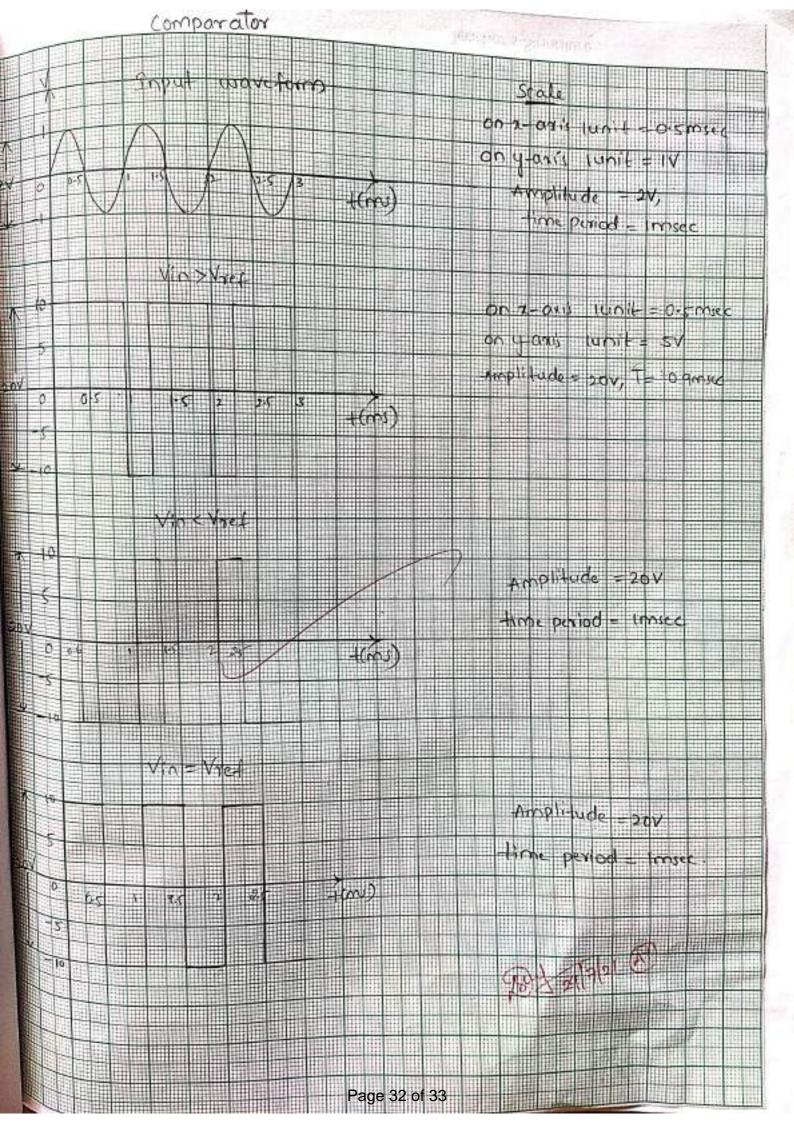
SI. No.	Date	No. of Periods	Brief Note of topic dealt	Signature ( Head / Principal
1	23/03/204	38	momental withthe - Holler	* j
2	2012/204	3//	Amplifude modulation & permodulation	
3	6/4/204	3 12	Frequency modulation & Demodulation	1/ 2
4	2714/104	243 1	DSB-SC modulator & petertor 1001	1. P
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			Page 28 of 33	
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Circuit diagram :-



Name of the Experiment:	108 USing TC 741	OP-AMP
2. 10. 10. 10. 10. 10. 10. 10. 10. 10. 10	using ICHHI OP-Am	Ρ
Component Name	Specification 20	Quantily
TC 741  Resistors	TC 741	1 1
Regulated Power Supply	(0-39) v, 4A	2
Function generator	1MHZ, 20Vp=p	i
Multimeter >	3/2 digital display	1
connecting wires		Required
heory: - It is a circuit	which compares a	signal voltag
explied at one input terrence voltage at other this shown in figure. A	input. Non-invertion	q comparate
(-) input and the vo	arying signal v, is	applied to
(+) signal.		Page No.: 9







The autput voltage is at -Vsat for vi < Vret and no
goes to tVsat for the VirVref. The output wave form
for a line input applied to (+) input as shown.
procedure:-
1. connect the circuit as per circuit diagram.
2. Apply supply voltage of 15v to pin 7 and 15v to pin 4
of IC741 respectively.
3 Apply input V1 as sine wave of 10Vp-p and note down
the output at pin 6 of IC+HI
4. Note down the square wove output amplitude.
precautions:
1. check the conductions before giving power supply
2. Readings should be taken carefully.
Results-
Hence using op-amp comparator circuit is verified.
and 20121 (At)