6.5.2 The institution reviews its teaching learning process, structures & methodologies of operations and learning outcomes at periodic intervals through IQAC set up as per norms and recorded the incremental improvement in various activities for first cycle incremental improvements made for the preceding five years with regard to quality.

S.No.	Two examples of institutional reviews	Page No.
1	Course file	1-69
2	Evaluation process	70-104

PRINCIPAL
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Sri Indu Institute of Engineering and Technology

Department of Computer Science and Engineering

COURSE FILE

PREPARED BY: Dr.K.S.SADA SIVA RAO

DEPARTMENT: COMPUTER SCIENCE AND ENGINEERING

ACADEMIC YEAR : 2018-2019

SUBJECT :CS304ES-DIGITAL LOGIC DESIGN(C214)

CLASS : II YEAR / I SEM – CSE – B – SECTION.

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DEPARTMENT VISION

To become prominent knowledge hub for learners, strive for educational excellence with innovative and industrial techniques so as to meet the software industry needs.

DEPARTMENT MISSION

DM1 To Provide educational ambience that enhances innovations, problem solving skills, leadership qualities, decision making, team-spirit and ethical responsibilities.

DM2 Imparting quality education with professional and personal ethics, so as to attain with challenging technological needs of industry and society.

DM3 To provide academic infrastructure and develop linkage with the world class organizations to strengthen industry-academia relationships for learners.

DM4 Provide platform to strengthen novel research in thrust area of Computer Science and Engineering to serve the needs of Government and Society.

Head of The Department

Head of the Department
Computer Science & Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH.
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

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Sri Indu Institute of Engineering & Tech
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R.R. Dist. Telangana -501 510

PROGRAM EDUCATIONAL OBJECTIVES(PEO's)

PEO1 Graduates with strong academic and technical skills of modern computer science and engineering.

PEO2 Graduate with leadership qualities and ability to solve real time problems using current techniques & tools in interdisciplinary environment.

PEO3 Graduates with attitude towards lifelong learning through continuing education and professional development.

PROGRAM SPECIFIC OUTCOMES(PSO's)

PSO1 **Professional Skills:** The ability to implement computer programs of varying complexity in the areas related to web design, cloud computing and networking.

PSO2 **Problem-Solving Skills**: The ability to develop quality products using open ended programming environment

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Head of the Department
Computer Science & Engg. Dept.
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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

PROGRAMME OUTCOMES (POs)

PO1 **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 **Problem analysis:** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3 **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4 **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO6 **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7 **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8 **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9 **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10 **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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Computer Science & Engg. Dept.
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Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

CS304ES: DIGITAL LOGIC DESIGN

B.Tech. II Year I Sem.

L	T	P	C
3	0	0	3

Course Objectives:

- To understand basic number systems, codes and logical gates.
- To understand the concepts of Boolean algebra.
- To understand the use of minimization logic to solve the Boolean logic expressions.
- To understand the design of combinational and sequential circuits.
- To understand the state reduction methods for Sequential circuits.
- To understand the basics of various types of memories.

Course Outcomes:

- Able to understand number systems and codes.
- Able to solve Boolean expressions using Minimization methods.
- Able to design the sequential and combinational circuits.
- Able to apply state reduction methods to solve sequential circuits.

UNIT - I

Digital Systems, Binary Numbers, Number base conversions, Octal, Hexadecimal and other base numbers, complements, signed binary numbers, Floating point number representation,binary codes, Error detection and correction, binary storage and registers, binary logic,Boolean algebra and logic gates , Basic theorems and properties of Boolean Algebra,Boolean functions, canonical and standard forms, Digital Logic Gates.

UNIT - II

Gate–Level Minimization, The K-Map Method, Three-Variable Map, Four-Variable Map,Five-Variable Map , sum of products , product of sums simplification, Don't care conditions ,NAND and NOR implementation and other two level implementations, Exclusive-ORfunction.

UNIT - III

Combinational Circuits (CC), Analysis procedure, Design Procedure, Combinational circuitfor different code converters and other problems, Binary Adder-Subtractor, Decimal Adder,Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers, Demultiplexers.

UNIT - IV

Synchronous Sequential Circuits, Latches, Flip-flops, analysis of clocked sequential circuits, Registers, Shift registers, Ripple counters, Synchronous counters, other counters.
Asynchronous Sequential Circuits -Introduction, Analysis procedure, Circuits with latches, Design procedure, Reduction of state and follow tables, Race- free state assignment, Hazards.

UNIT - V

Memory: Introduction, Random-Access memory, Memory decoding, ROM, Programmable Logic Array, Programmable Array Logic, Sequential programmable devices.
Register Transfer and Microoperations - Register Transfer Language, Register Transfer, Bus and Memory Transfers,Arithmetic Microoperations, Logic Microoperations, Shift Microoperations, Arithmetic LogicShift Unit.

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TEXT BOOKS:

1. Digital Design, M. Morris Mano, M.D.Ciletti, 5th edition, Pearson.(Units I, II, III, IV, Part of Unit V)
2. Computer System Architecture, M.Morris Mano, 3rd edition, Pearson.(Part of Unit V)

REFERENCE BOOKS:

1. Switching and Finite Automata Theory, Z. Kohavi, Tata McGraw Hill.
2. Fundamentals of Logic Design, C. H. Roth, L. L. Kinney, 7th edition, Cengage Learning.
3. Fundamentals of Digital Logic & Micro Computer Design, 5TH Edition, M. Rafiquzzaman, John Wiley.

Faculty Signature

Dr.K.S.Sada Siva Rao

(Professor/CSE, SIIET)

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SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Computer Science and Engineering
2018-19; 1st Semester

Course:DIGITAL LOGIC DESIGN (C214) **Class: II – I SEM – B- Section**

COURSE OUTCOMES (CO):

After completing this course the student will be able to:

C214.1 Apply the number conversion systems and codes.(Application)

C214.2 Solve Boolean expressions using Minimization methods.(Evaluation)

C214.3 Design the sequential and combinational circuits.(Synthesis)

C214.4 Analyze state reduction methods to solve sequential circuits. (Analysis)

C214.5 Describe about memory organizations, PAL, PLA and memory hierarchy concepts.(Knowledge)

C214.6 Designreduction of state and follow tables, role free conditions. (Synthesis).

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO/CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C214.1	3	1	-	-	-	-	-	-	-	-	-	-	2	-
C214.2	2	3	1	-	-	-	-	-	-	-	-	-	1	-
C214.3	1	-	3	-	-	-	-	-	-	-	-	1	-	-
C214.4	1	3	2	-	-	-	-	-	-	-	-	-	1	1
C214.5	3	-	-	-	-	-	-	-	-	-	-	2	-	-
C214.6	2	1	3	-	-	-	-	-	-	-	-	1	-	-
C214	2	2	2.5	-	-	-	-	-	-	-	-	1.3	1.3	1

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CO-PO Mapping Justification

C214.1 Apply the number conversion systems and codes.(Application)

	Justification
PO1	Able to understand the basic concept of number systems and codes(level 3)
PO2	Solve problems on number systems(level 1)

C214.2 SolveBoolean expressions using Minimization methods. (Analysis)

	Justification
PO1	Solve Boolean expressions using Minimization methods.(level 2)
PO2	Solve Identify, formulate and analyze complex Boolean expressions(level 3)
PO3	Student can able to designing minimization methods(level 1)

C214.3 Design the sequential and combinational circuits.(Synthesis)

	Justification
PO1	Able to understand thesequential and combinational circuits(level 1)
PO3	Student can design the combinational circuits(level 3)

C214.4 Analyze state reduction methods to solve sequential circuits. (Analysis)

	Justification
PO1	Understanddifferent types of latches and flip-flops. (level 1)
PO2	Student can anlyze the state tables(level 3)
PO3	Understand about reduction of state and follow tables, role free conditions. (level 2)

C214.5 Analyze memory organizations, PAL, PLA and memory hierarchy concepts(Analysis)

	Justification
PO1	Understand the basics of various types of memories. (level 3)

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C214.6 Design reduction of state and follow tables, role free conditions. (Synthesis)

	Justification
PO1	Understan different types of latches and flip-flops (level 2)
PO2	Understand about Asynchronous Sequential Circuits: reduction of state and follow tables, role free conditions (level 1)
PO3	Ability to design in Sequential Circuits(level 3)

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
ACADEMIC CALENDAR (2018-19)
FOR NON-AUTONOMOUS CONSTITUENT& AFFILIATED COLLEGES
B. TECH. II, III &IV YEARS I & II SEMESTERS

I SEM

S. No	EVENT	DATE	Duration
1.	Commencement of Instruction	9th July 2018	--
2.	First Mid Term Examinations	4th to 6th Sept. 2018	--
3.	Submission of First Mid Term Exam Marks to University on or before	15th Sept. 2018	--
4.	Parent-Teacher Meeting	13th Oct. 2018	--
5.	Dussehra recess	15th to 20th Oct. 2018	1 week
6.	Last date of Instruction	10th Nov. 2018	16 weeks
7.	Second Mid Term Examinations	12th to 14th Nov. 2018	--
8.	Preparation Holidays and Practical Examinations	15th to 24th Nov. 2018	1 week
9.	Submission of Second Mid Term Exam Marks to University on or before	24th Nov. 2018	--
10.	End Semester / Supplementary Examinations	26th Nov. to 8th Dec. 2018	2 weeks
11.	Semester Break	10th to 15th Dec. 2018	1 week

II SEM

S. No	EVENT	DATE	Duration
1.	Commencement of Instruction	17th Dec. 2018	--
2.	First Mid Term Examinations	11th to 13th Feb. 2019	--
3.	Submission of First Mid Term Exam Marks to University on or before	20th Feb. 2019	--
4.	Parent-Teacher Meeting	9th March. 2019	--
5.	Last date of Instruction	13th April 2019	16 weeks
6.	Second Mid Term Examinations	15th to 17th April 2019	--
7.	Preparation Holidays and Practical Examinations	18th to 27th April 2019	1 week
8.	Submission of Second Mid Term Exam Marks to University on or before	25th April 2019	--
9.	End Semester / Supplementary Examinations	29th April to 11th May 2019	2 weeks
10.	Summer Vacation	13th May to 6th July 2019	8 weeks

DIRECTOR
ACADEMIC & PLANNING, JNTUH

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SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY
COMPUTER SCIENCE AND ENGINEERING DEPARTMENT
TIME TABLE FOR AY-2018-19

Class: II-B.Tech CSE-B **Semester: 1** **LH. NO: A- 307** **W.E.F. 09-07-2018**

Period/ Day	1	2	3	4	1:00 - 1:30	5	6	7
	9:40-10:30	10:30-11:20	11:20-12:10	12:10-1:00		1:30-2:20	2:20-3:10	3:10-4:00
Monday	MFCS	DSTC++/MFCS(T)	DSTC++	M-IV	L	EST	JAVA	REM / COUN
Tuesday	MFCS	DLD	M-IV	SPORTS	U	DSTC++ LAB(BATCH-I)/ JAVA LAB(BATCH-II)		
Wednesday	JAVA	M-IV(T)	JAVA	DSTC++	N	DSTC++/MFCS(T)	DLD	MFCS
Thursday	DLD/JAVA(T)	JAVA LAB (BATCH-I)/ ITWS LAB(BATCH-II)			C	M-IV	CO - C/ SS/ DAA	
Friday	M-IV	EST	MFCS	LIB	H	DSTC++	DLD	INT
Saturday	EST	ITWS LAB (BATCH-I)/ DSTC++ LAB (BATCH-II)				DLD/JAVA(T)	DSTC++	JAVA

(T) – Tutorial (concern faculty)

Subject Code	Subject Name	Name of the Faculty	Subject Code	Subject Name	Name of the Faculty
DLD	Digital Logic Design	Dr.K.S.Sada siva Rao	JAVA LAB	Object Oriented Programming through Java Lab	Mrs. A.Padma
M - IV	Mathematics - IV	Mrs.T. Revathamma	ITWS LAB	IT Workshop Lab	Mr. P. Manoj Kumar
MFCS	Mathematical Foundation of Computer Science	Mrs.G. Swapna	INT	Internet	Mrs. J. Pujitha
DSTC++	Data Structures through C++	Mr. M. Sagar	CO - C/ SS/ DAA	Co-Curriculum/Soft Skills/Department Association Activities	Dr. T. Parameswaran
JAVA	Object Oriented Programming through Java	Mrs. A.Padma	LIB	Library	Mrs. G. Hemalatha
EST	Environmental Science and Technology	Mrs. V.Swapna	SPORTS	Sports	Mr. R. Karunakar Rao
DSTC++ LAB	Data Structures through C++ Lab	Mrs. P. H. Swarna Rekha	REM/COUN	Remedial/ Counseling	Concerned Faculty

Class In-Charge

Nasavi
Time Table Coordinator

HOD, CSE Department

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SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY
Department of Computer Science and Engineering

2018-19; 1st Semester

Course Title	DIGITAL LOGIC DESIGN
Course Code	CS304ES
Programme	B.Tech
Year & Semester	II-year I-semester
Regulation	R16
Course Faculty	Dr.K.S.Sada Siva Rao, Professor , CSE

LESSON PLAN

S.NO	Unit	TOPIC	Number of Sessions Planned	Teaching method/Aids	REFERENCE
1.	1	Digital Systems	1	Black Board	T1
2.		Binary Numbers	1	Black Board	T1
3.		Number base conversions	1	Black Board	T1
4.		Octal, Hexadecimal	1	Black Board	T1
5.		Other base numbers	1	Black Board	T1
6.		Complements	1	Black Board	T1
7.		Signed binary numbers	1	Black Board	T1
8.		Floating point number representation	1	Black Board	T1
9.		Binary codes	1	Black Board	T1
10		Error detection and correction	1	Black Board	T1
11		Binary storage and registers	1	Black BoarD	T1
12		Binary logic	1	Black Board	T1
13		Boolean algebra and logic gates	1	Black Board	T1
14		Basic theorems and properties of Boolean Algebra	1	Black Board	T1
15		Boolean functions	1	Black Board	T1
16		Canonical and standard forms	1	Black Board	T1
17		Digital Logic Gates	1	Black Board	T1
18		Hamming Code			
19	2	Gate-Level Minimization	1	Black Board	T1
20		The K-Map Method, Three-Variable Map	1	Black Board	T1
21		Four-Variable Map	1	Black Board	T1
22		Five -Variable Map	1	Black Board	T1
23		sum of products , product of sums simplification	1	Black Board	T1

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24	2	Don't care conditions	1	Black Board	T1
25		NAND and NOR implementation	1	Black Board	T1
26		other two level implementations, Exclusive-OR function	1	Black Board	T1
27	3	Combinational Circuits (CC)	1	Black Board	T1
28		Analysis procedure	1	Black Board	T1
29		Design Procedure	1	Black Board	T1
30		Combinational circuit	1	Black Board	T1
31		for different code converters and other problems	1	Black Board	T1
32		Binary Adder-Subtractor	1	Black Board	T1
33		Decimal Adder	1	Black Board	T1
34		Binary Multiplier	1	Black Board	T1
35		Magnitude Comparator	1	Black Board	T1
36	4	Decoders, Encoders, Multiplexers, Demultiplexers	1	PPT	T1
37		Synchronous Sequential Circuits, Latches	1	PPT	T1
38		Flip-flops, analysis of clocked sequential circuits	1	PPT	T1
39		Registers, Shift registers, Ripple counters	1	PPT	T1
40		Synchronous counters, other counters	1	PPT	T1
41		Asynchronous Sequential Circuits -Introduction	1	PPT	T1
42		Analysis procedure	1	PPT	T1
43		Design procedure	1	PPT	T1
44		Circuits with latches		PPT	
45		Reduction of state and follow tables	1	PPT	T1
46		Race- free state assignment	1	PPT	T1
47		Hazards	1	PPT	T1
48		Memory: Introduction	1	Black Board	T2

49		Random-Access memory	1	Black Board	T2
50		Memory decoding, ROM	1	Black Board	T2
51	5	Read only Memory	1	Black Board	T2
52		Programmable Logic Array	1	Black Board	T2
53		Programmable Array Logic	1	Black Board	T2
54		Sequential programmable devices	1	Black Board	T2
55		Register Transfer	1	Black Board	T2
56		Microoperations	1	Black Board	T2
57		Register Transfer Language, Register Transfer	1	Black Board	T2
58		Bus and Memory Transfers	1	Black Board	T2
59		Arithmetic Microoperations	1	Black Board	T2
60		Logic Microoperations	1	Black Board	T2
61		Shift Microoperations	1	Black Board	T2
62		Arithmetic Logic Shift Unit	1	Black Board	T2

TEXT BOOKS:

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3. Fundamentals of Digital Logic & Micro Computer Design, 5TH Edition, M. Rafiquzzaman, John Wiley.

WEB REFERENCES

W1 : https://www.logicdesign.co.uk/

W2:https://www.wiziq.com/tutorials/digital-logic-design

W3:www.nptel.iitm.ac.in

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W2:https://www.wiziq.com/tutorials/digital-logic-design

W3:www.nptel.iitm.ac.in

Faculty Signature

(Dr.K.S.Sada Siva Rao)

(Professor/CSE, SIIET)

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Code No: 133AJ **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, April/May - 2018
DIGITAL LOGIC DESIGN
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Convert $(67A9)_{16}$ into decimal. [2]
b) Add (+80) and (-70) using 2's complement. [3]
c) Write the truth table of Ex-OR Gate. [2]
d) Implement OR gate using NAND gates only. [3]
e) Write the truth table of half adder. [2]
f) Design half sub tractor circuit. [3]
g) Differentiate between Latch and flip flop. [2]
h) Draw the circuit diagram of Ring counter. [3]
i) Differentiate between RAM and ROM. [2]
j) Name any 3 logic micro operations. [3]

PART-B

(50 Marks)

2.a) i) Convert $(657)_8$ into decimal.
(C214.1)
ii) Convert $(2348)_{10}$ into hexa decimal.
(C214.1)
b) Represent the decimal number 46.5 as a floating point number with 16 bit mantissa and 8 bit exponent. [5+5]

OR

3.a) i) Convert 110001.1010010 into hexadecimal.
ii) Convert $(423.25)_{10}$ into Hex.
b) i) Simplify A(B+C)+AB+ABC
ii) Write the truth table and symbols of AND and OR gates. [5+5]

4. Obtain the simplified expression in sum of products for the following Boolean function.
a) $F(A,B,C,D) = \Sigma(2,3,12,13,14,15)$
b) $BDE+B'C'D+CDE+A'B'CE+A'B'C+B'C'D'E'$ [5+5]

OR

5. Obtain the simplified expression in product of sums.
a) $F(A,B,C,D) = \pi(0,1,2,3,4,10,11)$
b) $F(A,B,C,D) = \pi(1,3,5,7,13,15)$ [5+5]

16

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6.a) Design half adder using only NAND gates.
b) Design a combinational circuit which converts BCD to Excess-3 code. [5+5]

OR

7.a) Design a 2 bit magnitude comparator.
b) Implement 4*16 decoder using two 3*8 decoders. [5+5]

8.a) Explain a right shift register.
b) Design a 3 bit Ripple counter. [5+5]

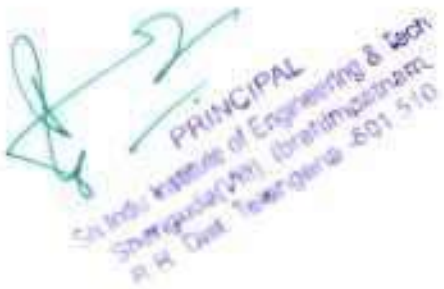
OR

9.a) What is a hazard? How do you eliminate hazards?
b) Design and explain Johnson counter. [5+5]

10.a) Explain different types ROMs.
b) Implement the following Boolean functions using PLA with 3 AND gates.
$F_1(ABC) = \Sigma(3,5,7)$, $F_2 = \Sigma(4,5,7)$. [5+5]

OR

11.a) Explain the applications of Logic micro operations.
b) Explain shift Right and Left with examples.



Code No: 133AJ **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, November/December - 2017
DIGITAL LOGIC DESIGN
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Subtract the following using 1's and 2's complement $(101)_2 - (10110)_2$. [2]
b) Distinguish between canonical and standard forms by giving an example. [3]
c) Derive the sum of minterms for the function f(a,b,c)=a'b+b'c' [2]
d) Implement the following function using only NAND Gates F=a.(b'+ c') + (b. c). [3]
e) Differentiate multiplexer and de-multiplexer. [2]
f) Draw the diagram of 4-Bit Parallel adder cum parallel subtractor. [3]
g) Show the excitation table and truth table of JK flip flop. [2]
h) Differentiate critical and non-critical race. [3]
i) Define Register Transfer Language. [2]
j) Differentiate PLA and PAL. [3]

PART-B

(50 Marks)

2.a) What are the various logic gates, give the representation along with the truth table.
b) What is the use of complements? Perform subtraction using 7's complement for the given Base-7 numbers (565)-(666). [5+5]

OR

3.a) Convert the following to the corresponding bases
i) $(9BCD)_{16} = (\ )_8$
ii) $(323)_4 = (\ )_5$
b) Given the 8 bit data word 11011011, generate the 12 bit composite word for the Hamming code that corrects and detects single errors. [5+5]

4.a) Derive the product of maxterms for f(a,b,c,d)=a.b.c+ b'.d+c.d'. **(C214.2)**
b) Derive and Implement Exclusive OR function involving three variables using only NAND function. [5+5]

OR

5.a) Obtain the simplified expression in SOP form of F(a,b,c,d,e)=Σ(1,2,4,7,12,14,15,24,27,29,30,31)using K-maps. [5+5]
b) Implement the function f(a,b,c)=π(0,1,3,4) using NAND-NAND two level gate structure.

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6.a) Implement and odd parity generator for 3-bit using a decoder.
b) Design a circuit for 2-bit binary multiplier. [5+5]

OR

7.a) Define a multiplexer? Draw a 4:1 multiplexer for the function
f(a,b,c,d)=Σ(0, 4,5,10,11,12,15)
b) Design a full binary adder with two half adders and a OR gate. [5+5]

8.a) Explain about a NOR Latch in detail, with a neat diagram.
b) Design a 3-bit counter using T flip flops. [5+5]

OR

9. Define essential hazard? Implement SR Latch by avoiding Hazard Neatly draw the diagram of SR latch before hazard and after Hazard elimination. [10]

10. Explain about RAM in detail. [10]

OR

11. What is a micro operation? List and explain its categories with relevant examples. [10]

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I- Mid Examinations, SEP-2018

Set - 1

Year &Branch: II CSE Date:

Subject:DIGITAL LOGIC DESIGN Marks: 10 Time: 60 min

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5 =10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

1.	Solve for X i)$(367)_8 = (X)_2$	(1)	(C214.1)	(Evaluation)	
	ii)$(378.93)_{10} = (X)_8$	(1)			
	iii)$(160)_{10} = (X)_2$	(1)	(C214.1)		
	iv)$(B9F.AE)_{16} = (X)_8$	(1)			
	V)$(11111110011)_2 = (X)_{16}$	(1)			
2.	(a) Define universal gates ? Realise AND, OR, NOT gates using universal gates?	(3)	(C214.2)	(Knowledge)	
	(b)Express the Canonical SOP form of the following functions (i)Y (A, B) = A + B (ii) Y(A, B, C, D) = AB + CD	(2)	(C214.1)	(Knowledge)	
3.	Solve the Boolean function i) $F(A,B,C,D) = \sum(2,3,10,11,12,13,14,15)$	(3)	(C214.2)	(Evaluation)	
	(ii) $F(A,B,C,D) = \pi(0,1,4,5,6,7,8,9)$	(2)	(C214.2)		
4.	Draw the following Boolean function with NAND gates $F(w, x, y, z) = \sum(1,3,10)$ and $d(w,x,y,z) = \sum(0,2,8,12)$	(5)	(C214.2)	(Knowledge)	

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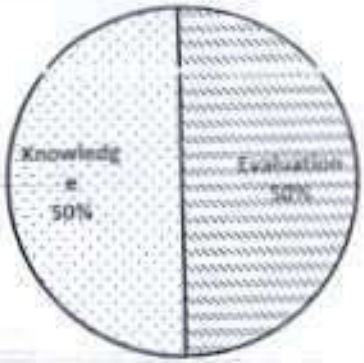
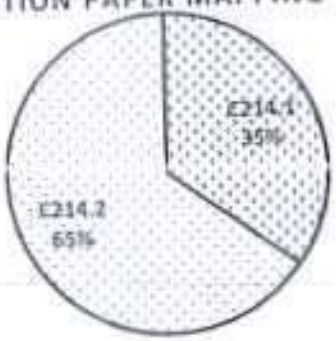
20

QUESTION PAPER MAPPING WITH BT'S



QUESTION PAPER MAPPING WITH CO'S



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I- Mid Examinations, SEP-2018

Set – II

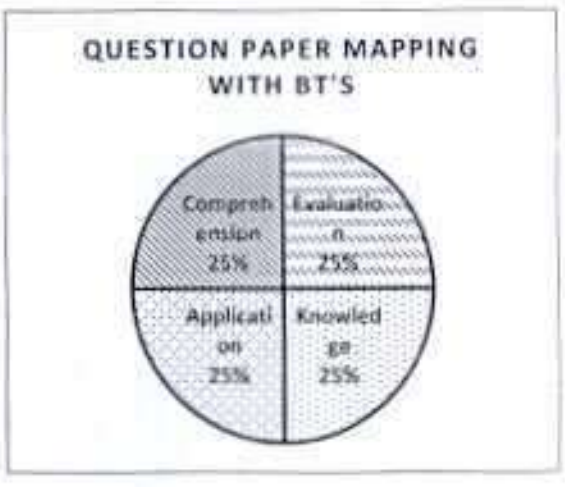
Year & Branch: II CSE Date:

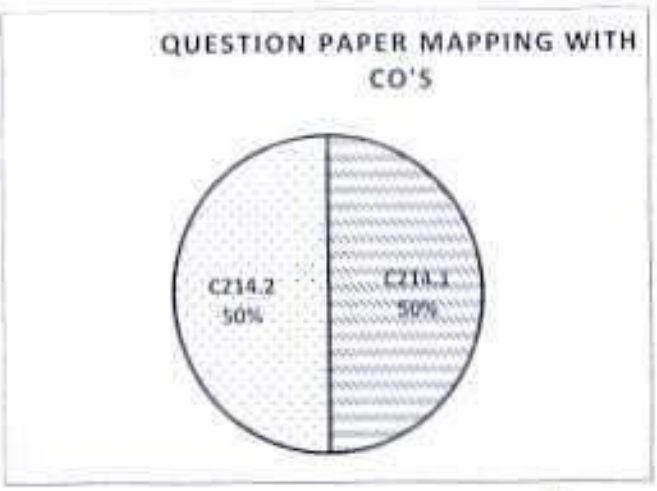
Subject:DIGITAL LOGIC DESIGN Marks: 10 Time: 60 min

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

1.	a) Perform 15_{10} - 28_{10} using 6 bit 2's complement representation.	(C214.1)	$2_{1/2}$	Evaluation
	b) Perform $46_{10} - 22_{10}$ in BCD using 10's complement.	(C214.1)	$2_{1/2}$	
2.	a) Define Excess 3 and Grey code numbers ?	(C214.1)	3	Knowledge
	b) Convert the binary (101011001) into excess-3 and grey code number.	(C214.1)	2	
3.	a) Simplify the Boolean function $F(w,x,y,z) = \sum (1,3,7,11,15)$ which has the don't care conditions $d(w,x,y,z) = \sum (0,2,5)$.	(C214.2)	3	Application
	b) Express F=A+B'C as sum of minterms.		2	
4.	Discuss about two graphic symbols for NOR gate and NAND gate (Demorgans laws). a) (A+B) (C+D) E b) A(B+CD)+BC'	(C214.2)	3+2	Comprehension





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I- Mid Examinations, SEP-2018

Set – I

Year & Branch: II CSE (A)

Date:

Subject: DLD

Marks: 10

Time: 60 min

All Question Carry Equal Marks

(This question paper is prepared with Course Outcome and BT's mapping)

ANSWER KEY

1. Solve for X i) $(367)_8 = (X)_2$

3	6	7
011	110	111

1/2

$(111110111)_2$ 1/2

ii) $(378.93)_{10} = (X)_8$

8 | 378

8 | 47 -2

5 - 7

$(572)_8$ 1/2

$.93 \times 8 = 7.44$

$0.44 \times 8 = 3.52$

$0.52 \times 8 = 4.16$

$0.16 \times 8 = 1.28$

7
3
4
1

1/2

$(572.7341)_8 = (378.93)_{10}$

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iii) $(160)_{10} = (X)_2$

2	160
2	80 – 0
2	40 – 0
2	20 – 0
2	10 – 0
2	5 – 0
2	2 – 1
	1 – 0

½

$(160)_{10} = (10100000)_2$ ½

iv) $(B9F \cdot AE)_{16} = (X)_8$

B 9 F . A E

1011 1001 1111 . 1010 1110

101	110	011	111	.	101	011	10
5	6	3	7	.	5	3	4

½

½

$((5637) \cdot (534))_8$

$(B9F.AE)_{16} = (5637.534)_8$

v) $(111\ 1111\ 0011)_2 = (X)_{16}$ ½

24

0111	1111	0011

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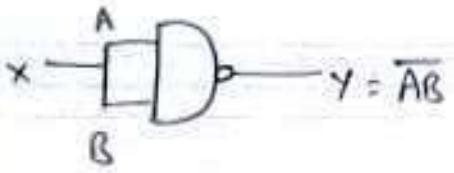
2.a) Define universal gates ? Realise AND, OR, NOT gates using universal gates.

The NAND and NOR gates are known as universal gates, since any logic function can be implemented using NAND (or) NOR gates. (1)

NOT fun using NAND gates:



A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

(1)

fig: NOT function using NAND gate.

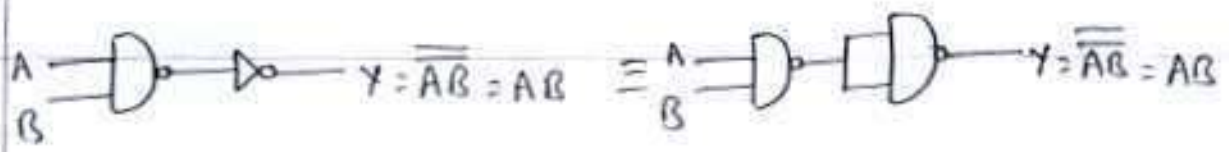
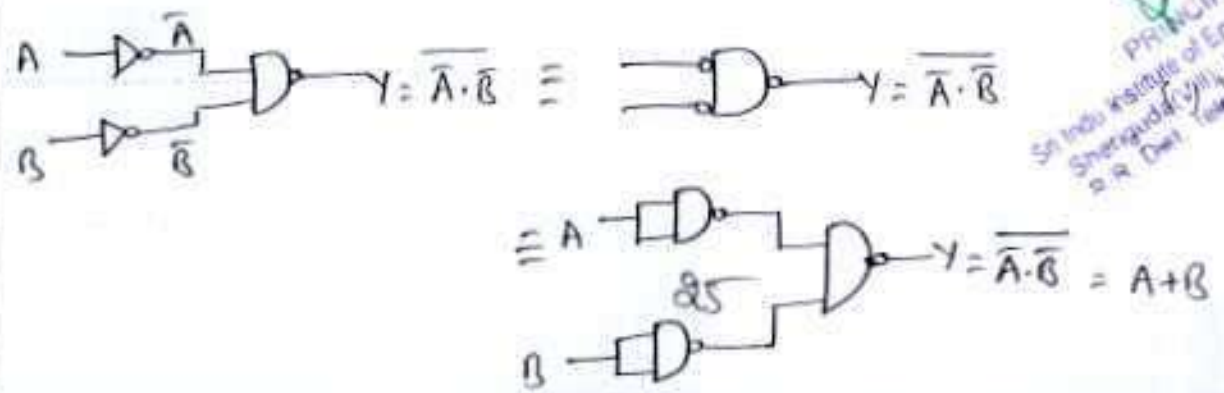


fig: AND function using NAND gates.



iii) $(160)_{10} = (X)_2$

2	160
2	80 – 0
2	40 – 0
2	20 – 0
2	10 – 0
2	5 – 0
2	2 – 1
	1 – 0

½

$(160)_{10} = (10100000)_2$ ½

iv) $(B9F \cdot AE)_{16} = (X)_8$

B 9 F . A E

1011 1001 1111 . 1010 1110

101	110	011	111	.	101	011	10
5	6	3	7	.	5	3	4

½

½

$((5637) \cdot (534))_8$

$(B9F.AE)_{16} = (5637.534)_8$

v) $(111\ 1111\ 0011)_2 = (X)_{16}$ ½

0111	1111	0011
7	F	3

26

½

$(7F3)_{16}$

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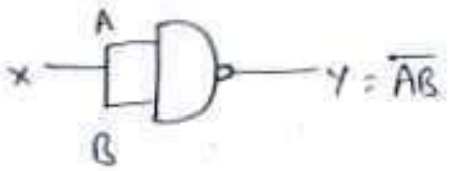
2.a) Define universal gates ? Realise AND, OR, NOT gates using universal gates.

The NAND and NOR gates are known as universal gates, since any logic function can be implemented using NAND (or) NOR gates.

NOT fun using NAND gate:



A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

fig: NOT function using NAND gate.

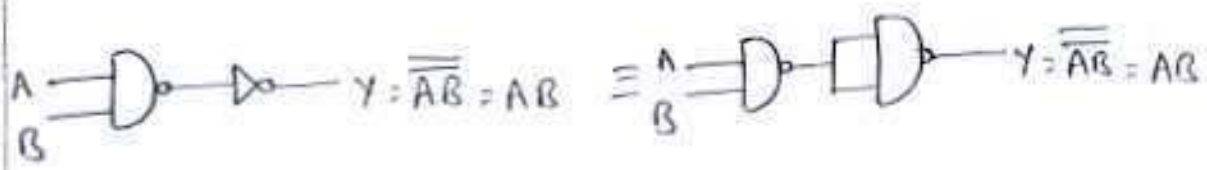


fig: AND function using NAND gates.

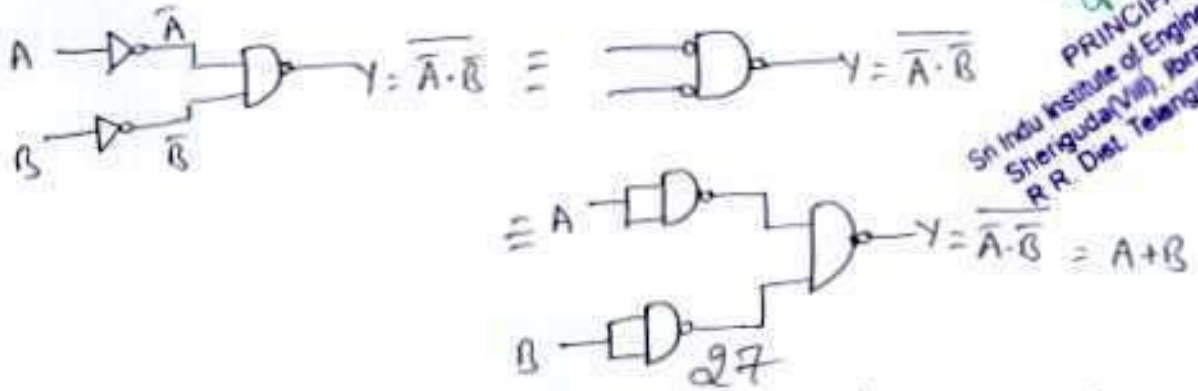
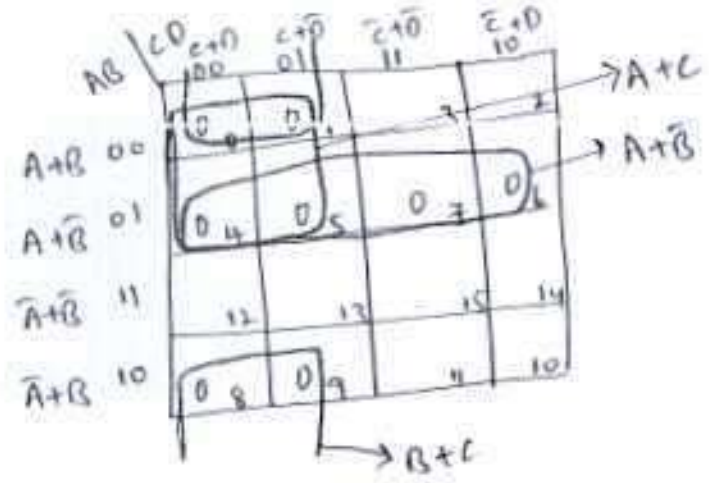


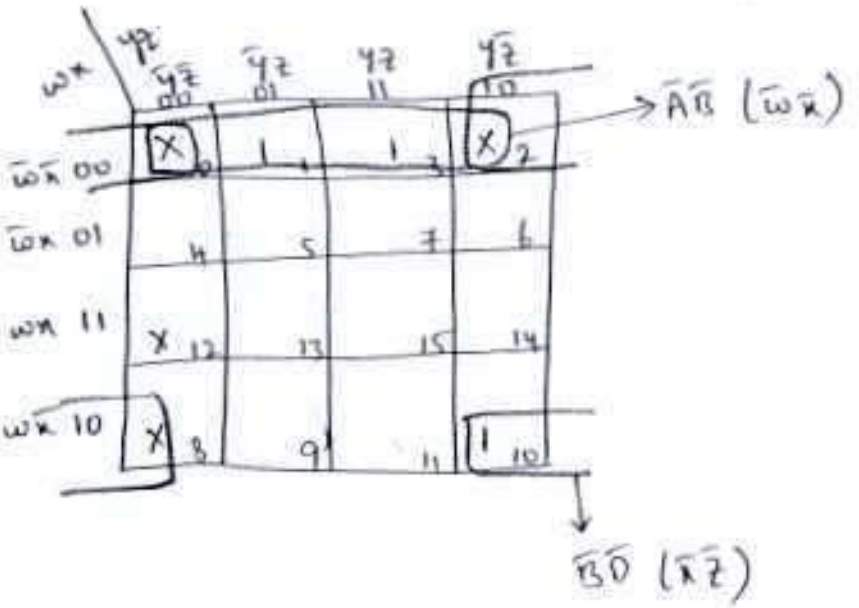
fig: OR function using only NAND gates.

3ii) $F(A,B,C,D) = \pi(0,1,4,5,6,7,8,9)$



4 Draw the following Boolean function with NAND gates

$F(w,x,y,z) = \Sigma(1,3,10)$ and $d(w,x,y,z) = \Sigma(0,2,8,12)$



$\therefore (\bar{w}\bar{x} + \bar{x}\bar{z})$

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b) Express the canonical SOP form of the following functions : i) $Y(A,B) = A+B$ ii) $Y(A,B,C,D) = AB+ACD$

i) $Y(A,B) = A+B$

$= A(B+B') + B(A+A')$

$= AB + AB' + AB + A'B$

$= AB + AB' + A'B$

ii) $Y(A,B,C,D) = AB+ACD$

$= AB(C+C')(D+D') + ACD(B+B')$

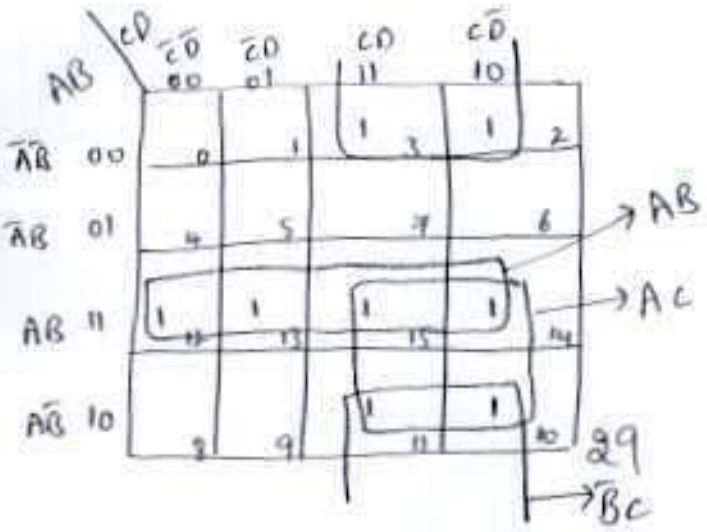
$= (ABC + ABC')(D+D') + ABCD + AB'CD$

$= ABCD + ABCD' + ABC'D + ABC'D' + ABCD + AB'CD$

$= ABCD + ABCD' + ABC'D + ABC'D' + AB'CD$

3) Solve the Boolean function

i) $F(A,B,C,D) = \Sigma(2,3,10,11,12,13,14,15)$



$AB + AC + \bar{B}C$

29

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II- Mid Examinations, NOV -2018

Set – I

Year & Branch: II- CSE-A,B&C Date:

Subject: **DLD** Max. Marks:10 Time: 60mins.

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

1.a)Distinguish between a decoder and encoder,with aid of block diagram clearly. (Comprehension)(C214.3)(3M)

b)Define half adder and full adder (Knowledge) (C214.3) (2M)

2.a)Comparison between combinational and sequentional circuits. (Evaluation) (C214.4) (2M)

b)Explain the working of master-slave JK-Flipflop. (Comprehension) (C214.4) (3M)

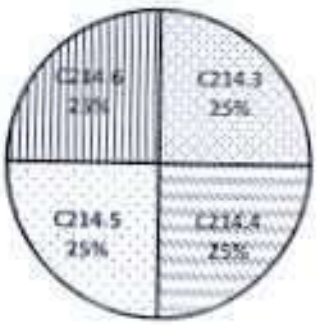
3.a)Design steps of asynchronous counters (Synthesis) (C214.6) (2M)

b)Draw and explain the working of 3-bit synchronous counters. (Knowledge) (C214.6) (3M)

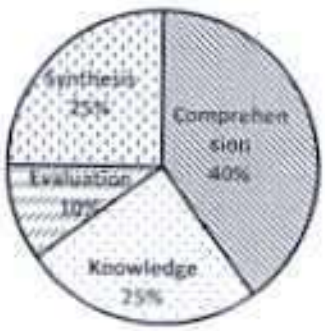
4.a)Explain the block diagram of memory unit. (Comprehension)(C214.5)(2M)

b) Design a combinational circuit is defined by the functions.F1=∑m(3,5,7), F2=∑m(4,5,7) implement that circuit with a PLA having 3 inputs,3 product terms & 2 outputs. (Synthesis) (C214.5) (3M)

QUESTION PAPER MAPPING WITH CO'S



QUESTION PAPER MAPPING WITH BT'S



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II- Mid Examinations, NOV -2018

Set – II

Year & Branch: II- CSE-A,B&C Date:

Subject: **DLD** Max. Marks:10 Time: 60mins

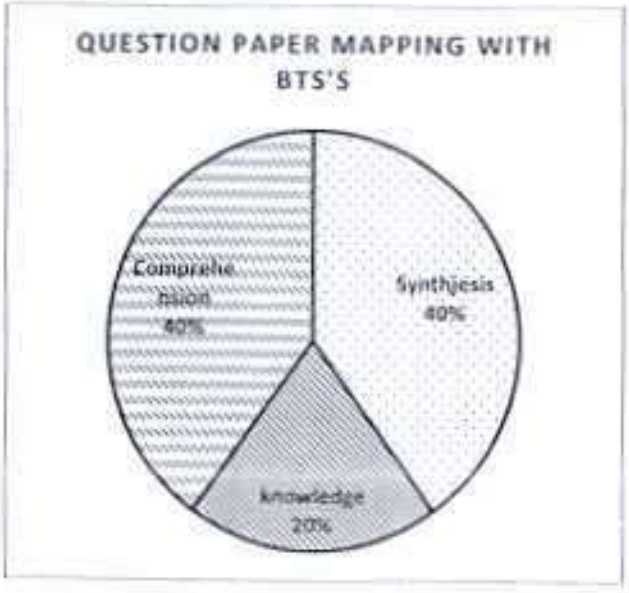
Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

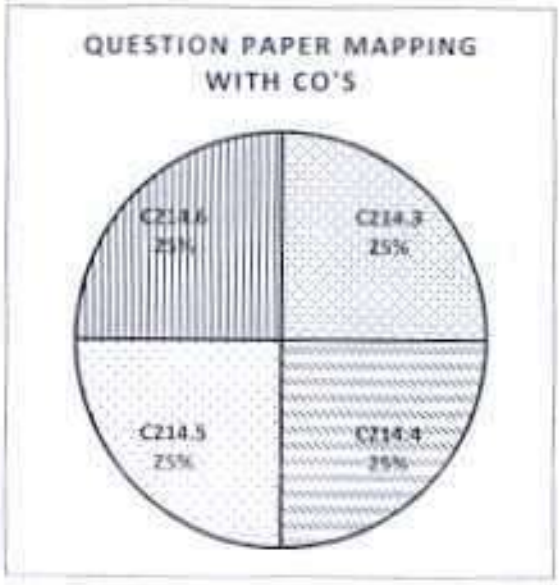
1.a)Design 3-to-8 line Decoder. (Synthesis)(C214.3)(3M)
b)Design 4-t01 line Multiplexer. (Synthesis) (C214.3)(2M)

2.a)Define buffer register. (Knowledge) (C214.6) (2M)
b)Explain the operation of SIPO and PISO shift registers. (Comprehension) (C214.6) (3M)

3.a)Design a mod-6 synchronous counter using JK-Flipflop. (Synthesis) (C214.4) (3M)
b)Draw andexplain the operation of 2's complement adder-subtractor.(Knowledge) (C214.4)(2M)

4.a)Explain in detail about RAM. (Comprehension)(C214.5) (2M)
b)Explain briefly about PAL,draw its structure. (Comprehension) (C214.5) (3M)





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II- Mid Examinations, NOV-2018

Set – I

Year & Branch: II CSE (A) Date:

Subject: DLD Marks: 10 Time: 60 min

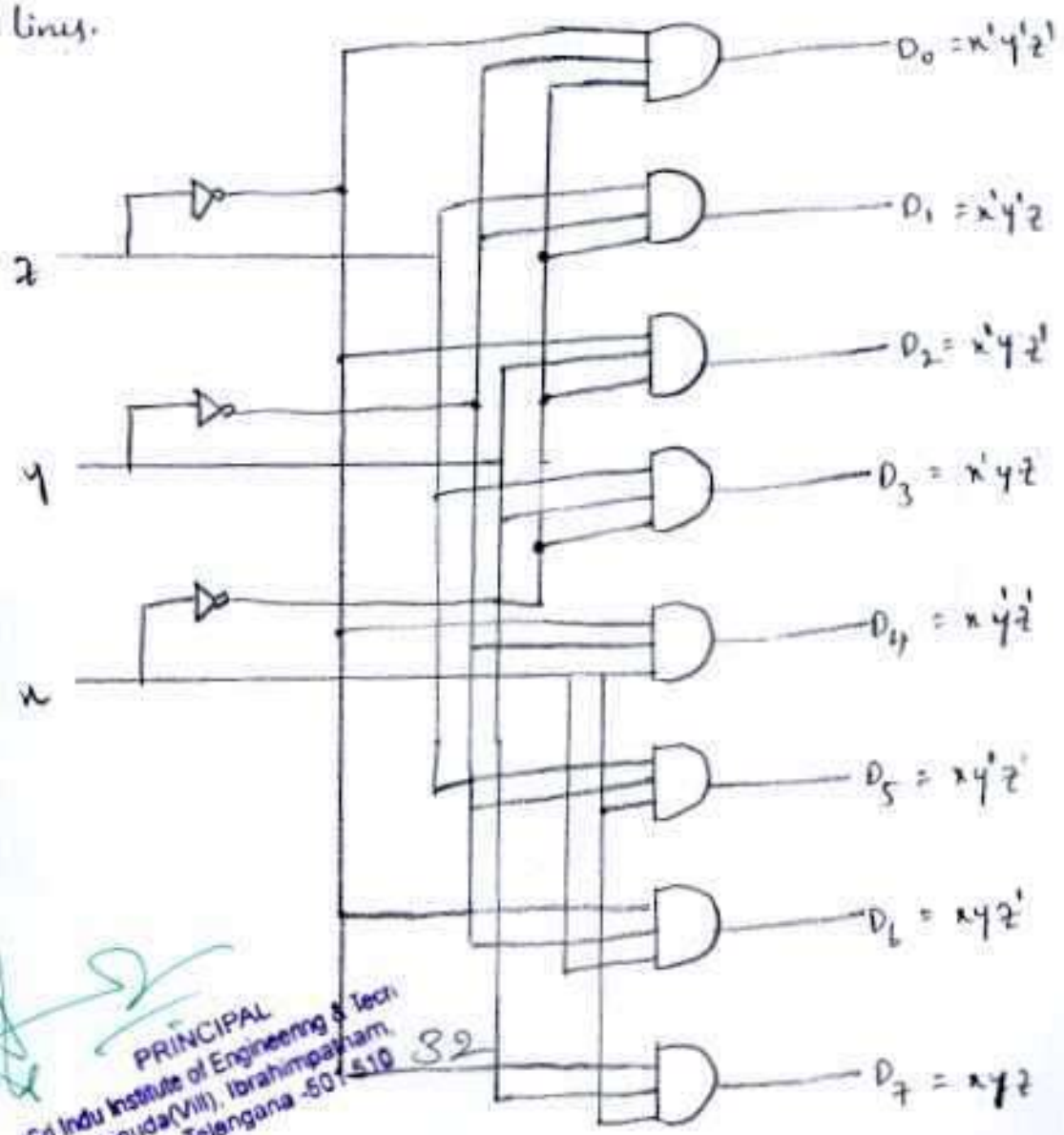
Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

ANSWER KEY

1) a) Design 3-to-8 line Decoder

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.



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1 b) Design 4 to 1 line Multiplexer.

A multiplexer is a combinational circuit that selects binary information from one of many i/p lines and directs it to a single output line.

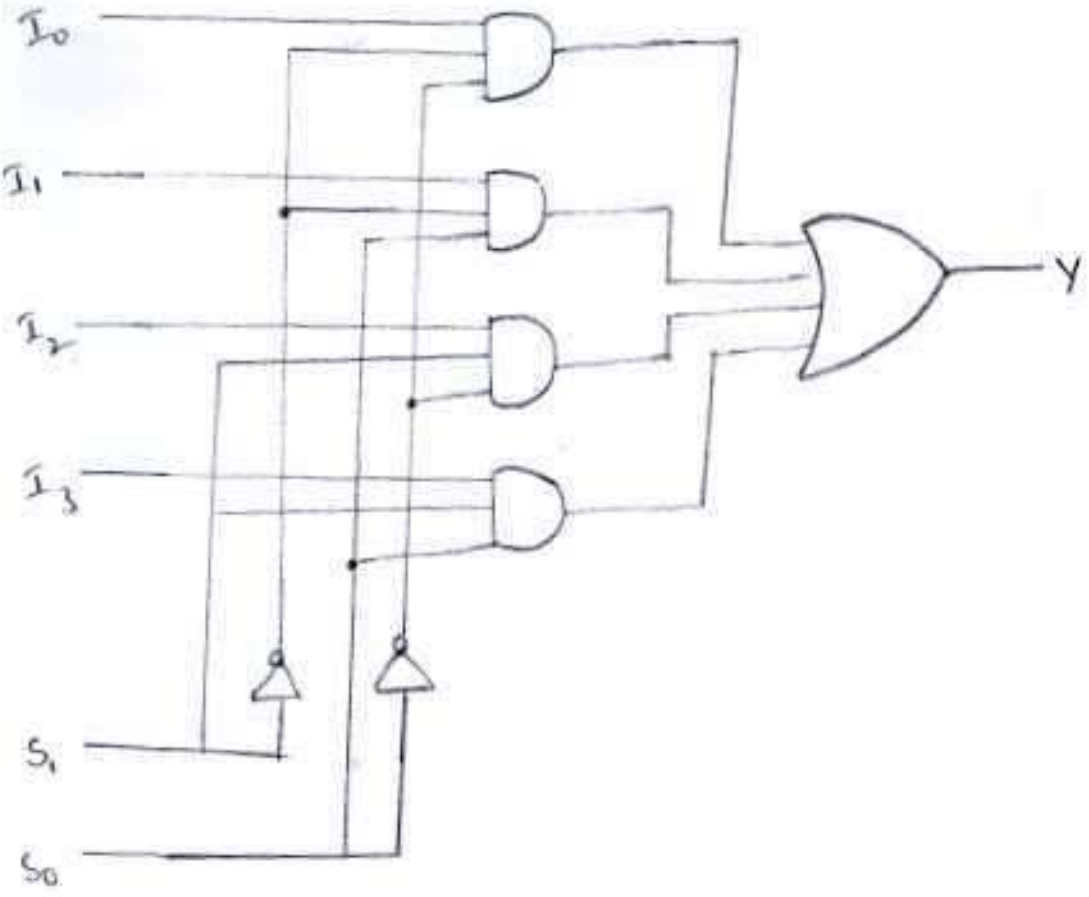
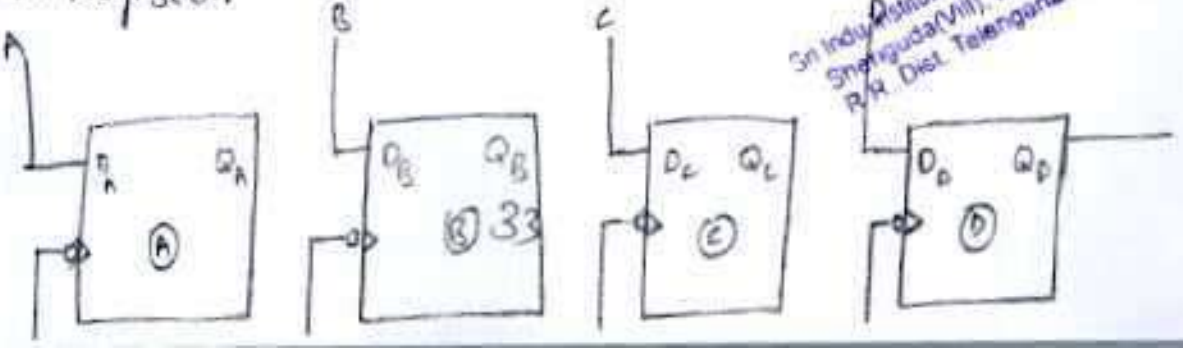


fig: 4 to-1 line multiplexer.

2)a) Define Buffer Register.

Buffer Register:-



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The simplest register constructed with four D-flip flops. this register is called buffer register. Each D-flip flop is triggered with a common negative edge clock time pulse.

b) Explain the operation of SIPO and PISO shift registers.

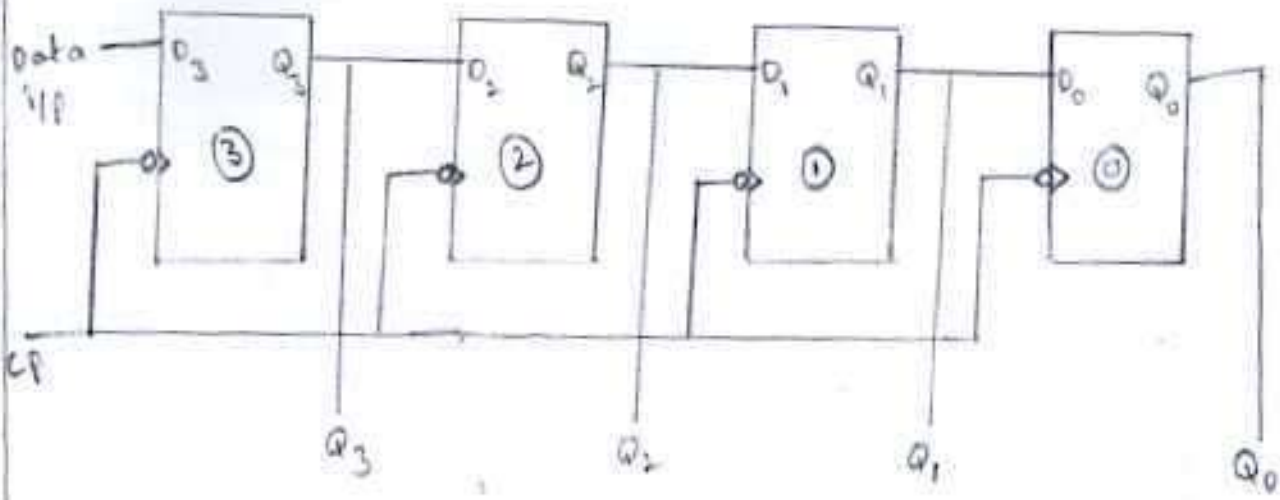

fig: Serial In Parallel out (SIPO) shift register.

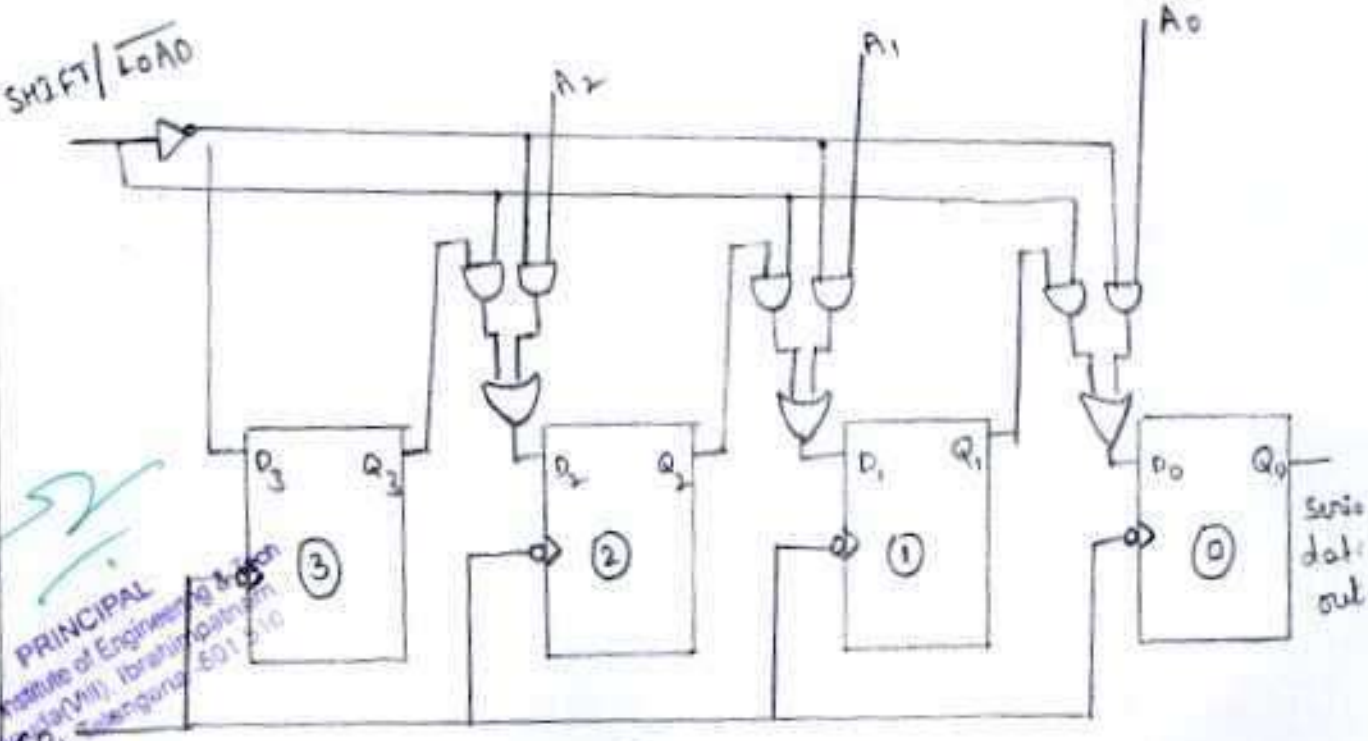

fig: Parallel In Serial out (PISO) shift Register.

3.a) Design a mod-6 synchronous counter using JK-flip flop.

The counter with n-flip flops has maximum mod number 2^n.

For ex 3-bit binary counter is a mod 8 counter. Let us design mod-6 counter using clocked JK-flip-flops.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

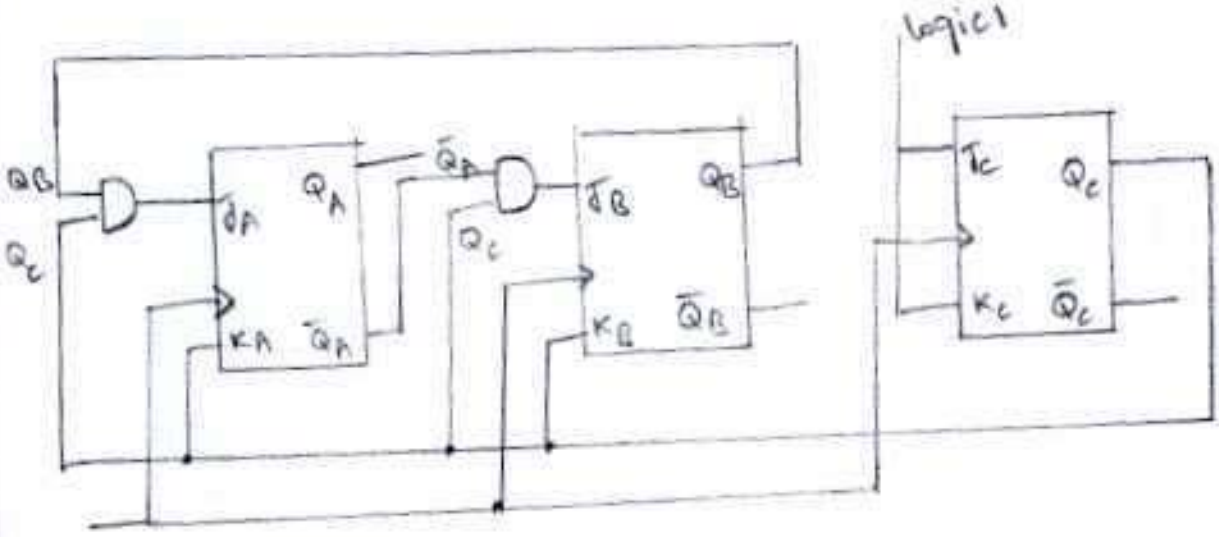

fig: Implementation of mod-6 synchronous counter.

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3.b) Draw and explain the operation of 2's complement adder-subtractor.

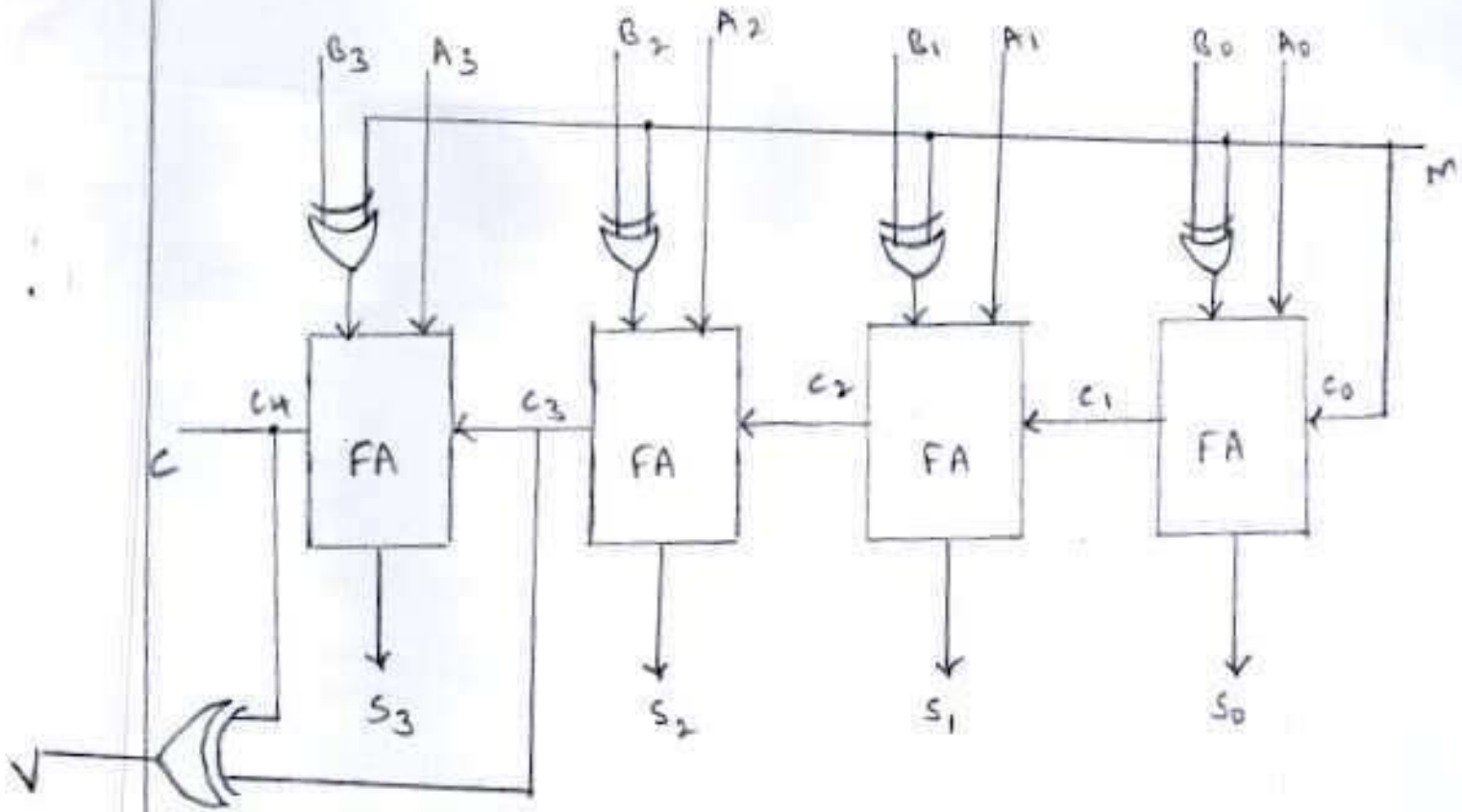

fig: 4-bit Adder Subtractor.

the mode input M controls the operation. When M=0, the circuit is adder, when M=1 the circuit becomes a subtractor.

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Receiving

0 0 1 0 0 1

$P_1 = 01 + 10 = 1$

$P_2 = 1 + 1 + 1 = 0$

$P_3 = 1 + 0 + 1 = 1$

$(101) = 5$

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Assignment Questions-I

(Assignment Questions are mapped with CO's, BT)

1.a) **Solve** 2's complement perform $(42)_{10} - (68)_{10}$. (Evaluation)(C214.1)
b) Implement the following Boolean function with NOR-NOR logic
$F(A,B,C) = \pi M\,(0,2,4,5,6)$.
c) **Convert** following hexadecimal number to decimal. (Evaluation)(C214.1)
i) $(F28)_{16}$ ii) $(BC2)_{16}$.

2.a) What is the specialty of unit-distance code? State where they are used.
b) Solve the Boolean expressions used for following gates (Evaluation)(C214.2)
i) AND ii) NOR iii) EX-OR iv) OR v) EX-NOR

3.**Analyze** the following functions using K-map techniques. (Analysis) (C214.2)
a) $f(A, B, C, D, E) = \Sigma m\,(1, 4, 8, 10, 11, 20, 22, 24, 25, 26) + d\,(0, 12, 16, 17)$
b) $f(A, B, C, D) = \pi M\,(4, 5, 6, 7, 8, 12, 13) + d\,(1, 15)$.

4.a) Using K-map obtain the minimal sum of products and the minimal product of sums from of the function $f(a,b,c,d) = \Sigma m\,(1, 2, 3, 5, 6, 7, 8, 13)$.
b) **Explain** about essential prime implicants. (Comprehension)(C214.1)

5.a) **Analyze** the following function Y = A + BCD using NAND gates only.(Analysis) (C214.2)
b) What is a Hamming code and encode data bits 0101 into a 7-bit even parity Hamming code. (Synthesis) (C214.1)

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II CSE-B

1) Solve the below problems

a) $(42)_{10} - (68)_{10}$ using 2's Compliment method

Sol) 42 – 101010 →
-68 – 1000100
-26

1000100
0111011
+1
0111100

0101010
0111100
1101 10

↓

0011001
1
-0011010

Procedure:

1) 2's Compliment the subtrahend (1000100 → 0111011)
2) Add it to the minute (0111011+1)
3) If there is no end around carry, again 2's Compliment the result & add negative sign
(0111100 ⇒ 0101010 – 0111100 = 1100110+1 = -0011010)

Result: -0011010 = -26.

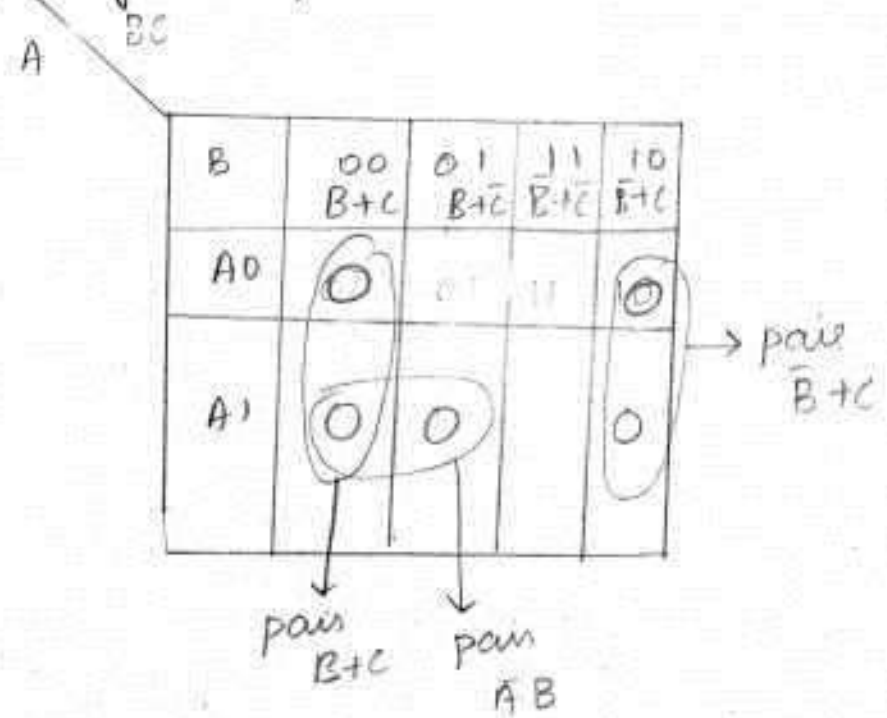
2) Implement the following boolean function with NOR-NOR logic $F(A,B,C) = \pi M(0,2,4,5,6)$

Sol

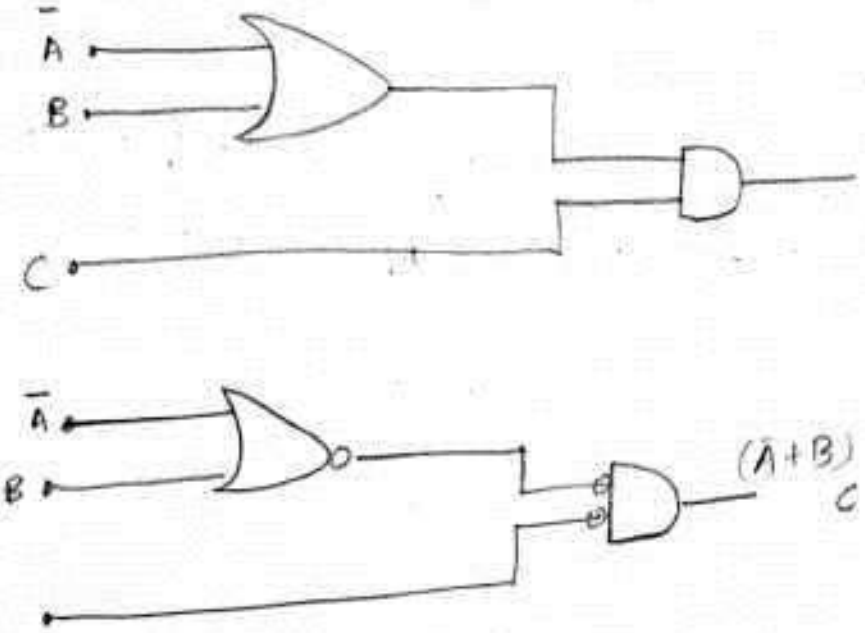
A	B	C		Y	
0	0	0	–	0	→ (A+B+C)
0	0	1	–	1	
0	1	1	–	0	→ $(A+\bar{B}+\bar{C})$
1	1	1	–	1	
1	1	0	–	0	→ $(\bar{A}+\bar{B}+C)$
1	0	0	–	0	→ $(\bar{A}+B+C)$
1	0	1	–	0	→ $(\bar{A}+B+\bar{C})$
0	1	0	–	1	

$Y=(A+B+C)(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+C)(\bar{A}+B+C)(\bar{A}+B+\bar{C})$

By using K-map.



$Y=C(\bar{A}+B)$



c) Convert the following Hexa-decimal number, to decimal number

i) $F28_{(16)}$ ii) $BC2_{(16)}$

i) $F28_{(16)}$

Sol) F28

$\rightarrow 16^0 \times 8 = 8$

$\rightarrow 16^1 \times 2 = 32$

$\rightarrow 15 \times 16^2 = 3840$

$F28 = 8 + 32 + 3840$

$= 3880$

ii) $BC21_{(18)}$

BC21

$\rightarrow 18^0 \times 1 = 1$

$\rightarrow 18^1 \times 2 = 36$

$\rightarrow 18^2 \times C = 18^2 \times 12 = 3888$

$\rightarrow 18^3 \times B = 18^3 \times 11 = 64152$

$BC21 = 1 + 36 + 3888 + 64152$

$= 68077$

$BC21_{(18)} = 68077_{(10)}$

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2a) What is the speciality of unit distance Code? Write. Why they are used.

Ans The Gray Code is a single-step code (i.e a unit distance code). It's often used in analog/digital Conversion devices. Adjacent code patterns of Gray

Code differs in just only one bit to avoid ambiguity.

→ It is non-weighted code. Each increased count in a gray code is accomplished by only bit change in its state. The change of the single bit of any binary code group is useful to increment the characteristics, which is important in some of digital electronics.

Rules for writing Gray code:

1. The left most bit of the gray code is same as binary code.
2. Add the MB to bit on its immediate right and record the sum below the gray code line by neglecting if any carry.
3. Continue the addition process for each bit with its right bit until LSB is reached.
4. The no. of bits in gray code will always be same as in the binary code

Eg:

Bin :- 1 0 1 1 0 0 1

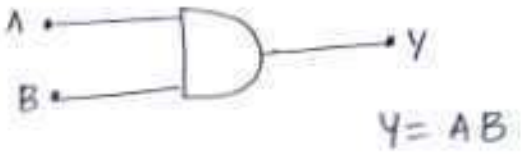
Gray 1 1 1 1 1 1 1 0 1

Bin :- 1 0 1 0 1 1 0 0 1

b. Solve the bodean expression used for following gates
i) AND ii) NOR iii) EX-OR iv) OR v) EX-NOR.

i) AND Gate.

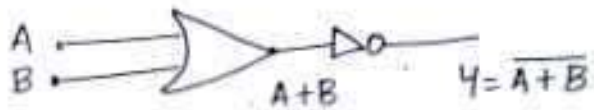
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



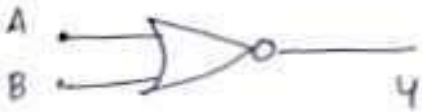
$Y = AB$

ii) NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



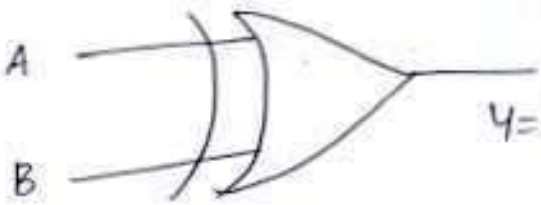
$Y = \overline{A+B}$



$Y = \overline{A+B}$

iii) EX-OR

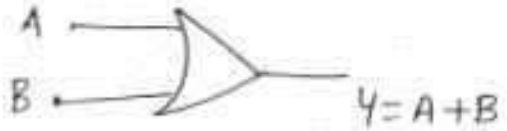
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



$Y = \bar{A}B + A\bar{B}$

iv) OR - gate

A	B	Y
0	0	0
0	1	1
1	1	1
1	0	1



v) EX-NOR gate

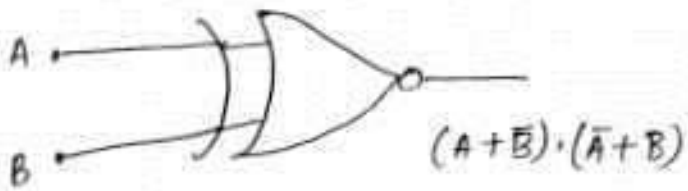
A	B	$Y = A\bar{B} + \bar{A}B$	$Y = \overline{\bar{A}B + A\bar{B}}$
0	1	1	0
0	0	0	1
1	0	1	0
1	1	0	1

$$Y = \overline{\bar{A}B + A\bar{B}}$$

$$Y = \overline{\bar{A}B} \cdot \overline{A\bar{B}}$$

$$= \bar{A} + \bar{B} \cdot \bar{A} + \bar{B}$$

$$= (A + \bar{B}) \cdot (\bar{A} + B)$$



3a) Analyse the following functions using K'map techique

$f(A,B,C,D,E) = \Sigma m(1,4,8,10,11,20,22,24,25,26) - d(0,12,16,17)$

b) $f(A,B,C,D,E) = \Sigma m(6,4,5,18,7,12,13) - d(1,15)$

a) $f(A,B,C,D,E) = \Sigma m(1,4,8,10,11,20,22,24,25,26) - d(0,12,16,17)$

A	B	C	D	E	Y	
0	0	0	0	0	x	$\bar{A}\bar{B}C\bar{D}\bar{E}$
1	0	0	0	1	1	$A\bar{B}C\bar{D}E$
0	0	0	1	0	0	
0	0	0	1	1	0	
0	0	1	0	0	1	$\bar{A}\bar{B}C\bar{D}\bar{E}$
0	0	1	0	1	0	
0	0	1	1	0	0	
0	0	1	1	1	0	
0	1	0	0	0	1	$\bar{A}B\bar{C}\bar{D}\bar{E}$
0	1	0	0	1	0	
0	1	0	1	1	1	$\bar{A}B\bar{C}D\bar{E}$
0	1	0	1	1	x	$\bar{A}B\bar{C}DE$
0	1	1	0	0		
0	1	1	0	1	0	$\bar{A}BCD\bar{E}$
0	1	1	1	0	0	
0	1	1	1	1	0	
1	0	0	0	0	x	$A\bar{B}C\bar{D}\bar{E}$
1	0	0	0	1	x	$A\bar{B}\bar{C}DE$
1	0	0	1	0	0	
1	0	0	1	1	0	
1	0	1	0	0	1	$A\bar{B}C\bar{D}\bar{E}$
1	0	1	0	1	0	
1	0	1	1	0	1	

1	0	1	1	1	0	
1	1	0	0	0	1	$A\bar{B}C\bar{D}\bar{E}$
1	1	0	0	1	1	$A\bar{B}C\bar{D}E$
1	1	0	1	1	0	$A\bar{B}CD\bar{E}$
1	1	1	0	0	0	
1	1	1	0	1	0	
1	1	1	1	0	0	
1	1	1	1	1	0	

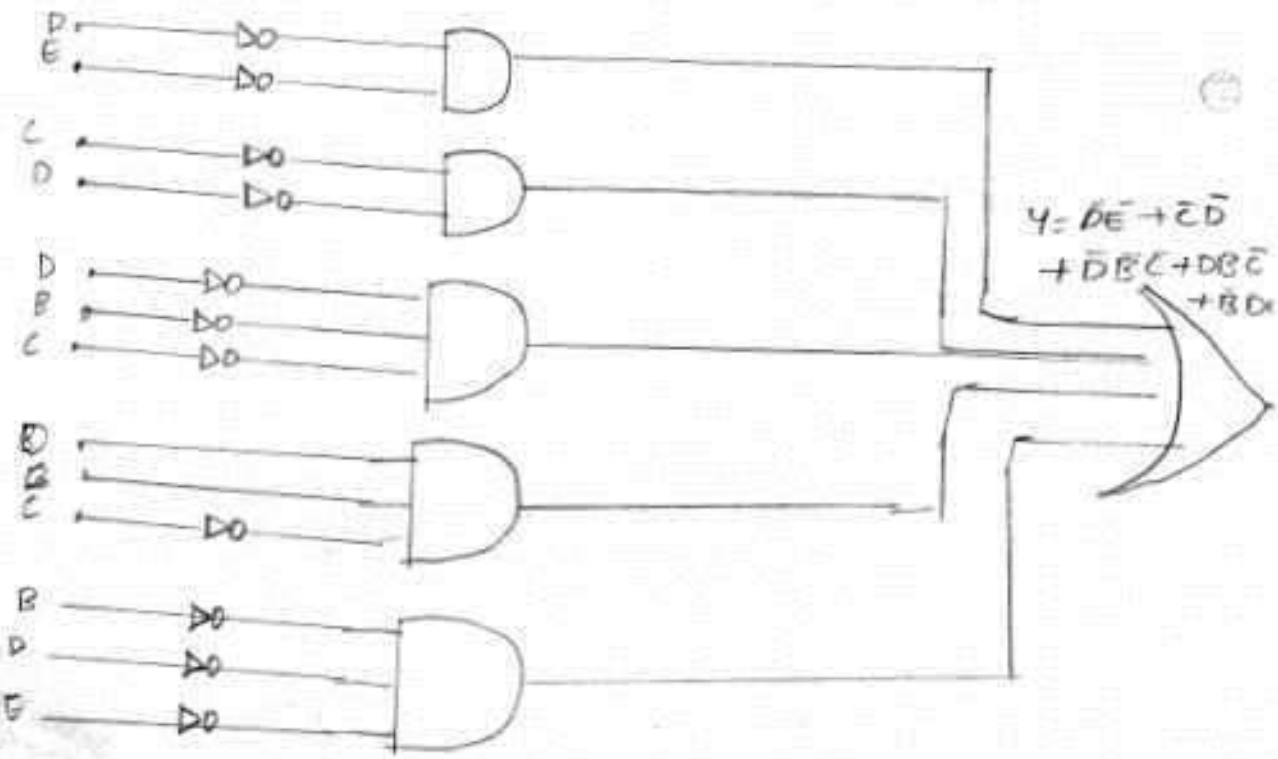
A=0

BC \ DE	00 $\bar{D}\bar{E}$	01 $\bar{D}E$	11 DE	10 $D\bar{E}$	
00 $B\bar{C}$	X	1	0	0	→ pair $=\bar{B}\bar{C}$
01 $B\bar{C}$	1	0	0	0	
11 BC	X	0	0	0	
10 $B\bar{C}$	X	0	1	1	

A=1

BC \ DE	00 $\bar{D}\bar{E}$	01 $\bar{D}E$	11 DE	10 $D\bar{E}$	
00 $B\bar{C}$	X	X	0	0	
01 $B\bar{C}$	1	0	0	1	
11 BC	0	0	0	0	pair $B\bar{D}E$
10 $B\bar{C}$	1	1	0	1	

$Y = \bar{D}\bar{E} + \bar{C}\bar{D} + B\bar{D}\bar{C} + D\bar{B}\bar{C} + \bar{B}D\bar{E}$ ↓ quadr: $\bar{C}\bar{D}$



b) $f(A,B,C,D) = \sum m(6,4,5,7,8,12,13) - d(1,15)$

	A	B	C	D	Y	
0	0	0	0	0	X	— $A+B+C+D$
1	0	0	0	1	1	
2	0	0	1	0	1	
3	0	0	1	1	1	
4	0	1	0	0	0	— $A+\bar{B}+C+D$
5	0	1	0	1	0	— $A+\bar{B}+C+\bar{D}$
6	0	1	1	0	0	— $A+\bar{B}+\bar{C}+D$
7	1	1	1	1	0	— $A+\bar{B}+\bar{C}+\bar{D}$
8	1	0	0	0	0	— $\bar{A}+B+C+D$
9	1	0	0	1	1	
10	1	0	1	0	1	
11	1	0	1	1	1	
12	1	1	0	0	0	— $\bar{A}+\bar{B}+C+D$
13	1	1	0	1	0	— $\bar{A}+\bar{B}+C+\bar{D}$
14	0	ϕ	1	0	1	
15	0	ϕ	1	1	X	— $\bar{A}+\bar{B}+\bar{C}+\bar{D}$

$Y = (A+B+C+D)(A+\bar{B}+C+D)(A+\bar{B}+C+\bar{D})(A+\bar{B}+\bar{C}+D)$
$(A+\bar{B}+\bar{C}+\bar{D})(\bar{A}+B+C+D)(\bar{A}+\bar{B}+C+D)(\bar{A}+\bar{B}+C+\bar{D})(\bar{A}+\bar{B}+\bar{C}+\bar{D})$

AB \ CD	$C+D$ 00	$C+\bar{D}$ 01	$\bar{C}+\bar{D}$ 11	$\bar{C}+D$ 10	
$A+B$ 00	1	X	1	1	
$A+\bar{B}$ 01	0	0	0	0	— $A+\bar{B}$
$\bar{A}+\bar{B}$ 11	0	0	X	1	
$\bar{A}+B$ 10	0	1	1	1	

$\bar{A}+C+D$, $B+C$

$Y = (\bar{A}+C+D)(A+\bar{B})(B+C)$

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4a) Using K'map obtain the minimal sum of product and minimal product of sum from the function $f(A,B,C,D) = \Sigma(1,2,3,5,6,7,8,13)$

Sol) Sum of product technique

A	B	C	D	Y	
0	0	0	0	0	
0	0	0	1	1	$\rightarrow (\bar{A}\bar{B}\bar{C}D)$
0	0	1	1	1	$\rightarrow (\bar{A}\bar{B}CD)$
0	1	1	1	0	$\rightarrow (\bar{A}BCD)$
1	1	1	1	0	
1	1	1	0	0	$\rightarrow (\bar{A}BC\bar{D})$
1	1	0	0	1	$\rightarrow (AB\bar{C}\bar{D})$
1	0	0	0	1	$\rightarrow (A\bar{B}\bar{C}\bar{D})$
1	0	0	1	1	$\rightarrow (A\bar{B}\bar{C}D)$
1	0	1	1	0	
0	1	1	0	1	
0	1	0	0	1	
1	1	0	0	1	
0	0	1	1	1	$\rightarrow (\bar{A}\bar{B}CD)$
0	1	0	1	1	

AB \ CD

	$\bar{C}\bar{D}$ (00)	$\bar{C}D$ (01)	CD (11)	$C\bar{D}$ (10)
$\bar{A}\bar{B}$ (00)	0	1	1	0
$\bar{A}B$ (01)	0	0	1	0
AB (11)	1	0	0	1
$A\bar{B}$ (10)	1	1	0	0

$(\bar{A}\bar{B}\bar{C}D) + (\bar{A}\bar{B}CD) + (\bar{A}BCD) + (AB\bar{C}\bar{D}) + (AB\bar{C}\bar{D}) + (A\bar{B}C\bar{D}) + (A\bar{B}\bar{C}D) + (\bar{A}\bar{B}CD)$

$\Rightarrow \bar{A}\bar{B}D(\bar{C}+C) + AB\bar{D}(C+\bar{C}) + \bar{B}D(A\bar{C}+\bar{A}C) + \bar{A}BCD + A\bar{B}\bar{C}\bar{D}$

$\Rightarrow \bar{A}\bar{B}D + AB\bar{D} + \bar{B}D + \bar{A}BCD + A\bar{B}\bar{C}\bar{D}$

Product of sum.

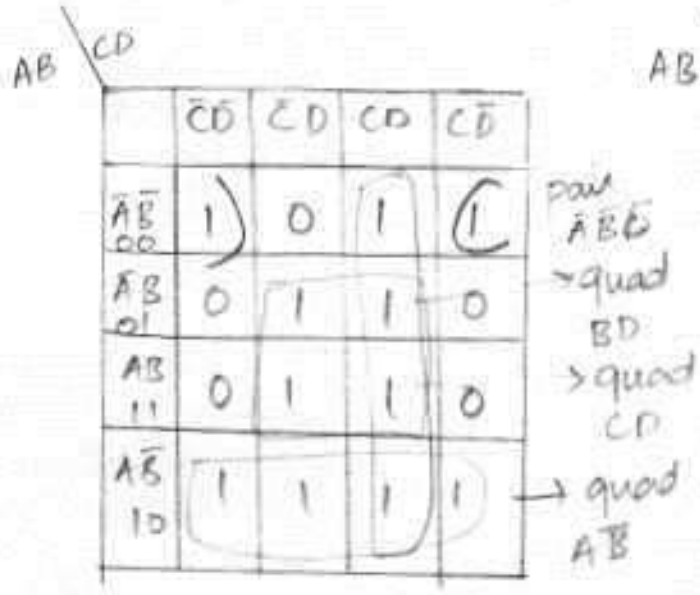
	00 $\bar{C}\bar{D}$	01 $\bar{C}D$	11 $C\bar{D}$	10 CD
00 $\bar{A}\bar{B}$	0	1	1	0
01 $A\bar{B}$	0	0	1	0
11 $\bar{A}\bar{B}$	1	0	0	1
10 $A\bar{B}$	1	1	0	0

$Y = \bar{A} + \bar{B} + D$

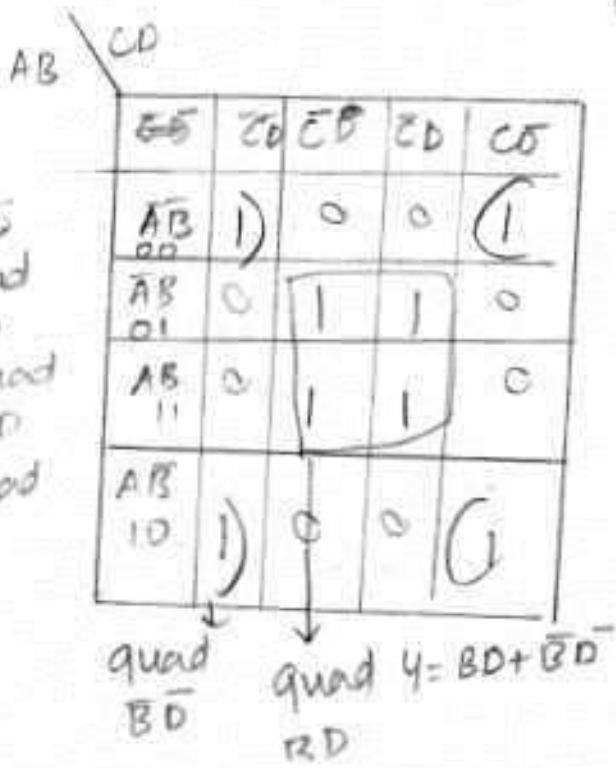
b) Explain about essential prime implicants.

A prime implicant is a product term obtained by combining the maximum possible numbers of adjacent squares in the map. If a minterm in a square is covered by only one prime implicant, that prime implicant is said to be "Essential prime implicant".

Ex: $F(A,B,C,D) = \Sigma(0,2,3,5,7,8,9,10,11,13,15)$



$Y = \bar{A}\bar{B}\bar{D} + BD + CD + A\bar{B}$



$Y = BD + \bar{B}\bar{D}$

5] a) Analyse the following $Y = A + BCD$ using NAND gate only.

$Y = A + BCD$

$Y = A(B+\bar{B})(C+\bar{C})(D+\bar{D}) + BCD(A+\bar{A})$

$Y = (ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C})(D+\bar{D}) + BCD(A+\bar{A})$

$Y = ABCD + AB\bar{C}D + A\bar{B}CD + A\bar{B}\bar{C}D + ABC\bar{D} + AB\bar{C}\bar{D} +$

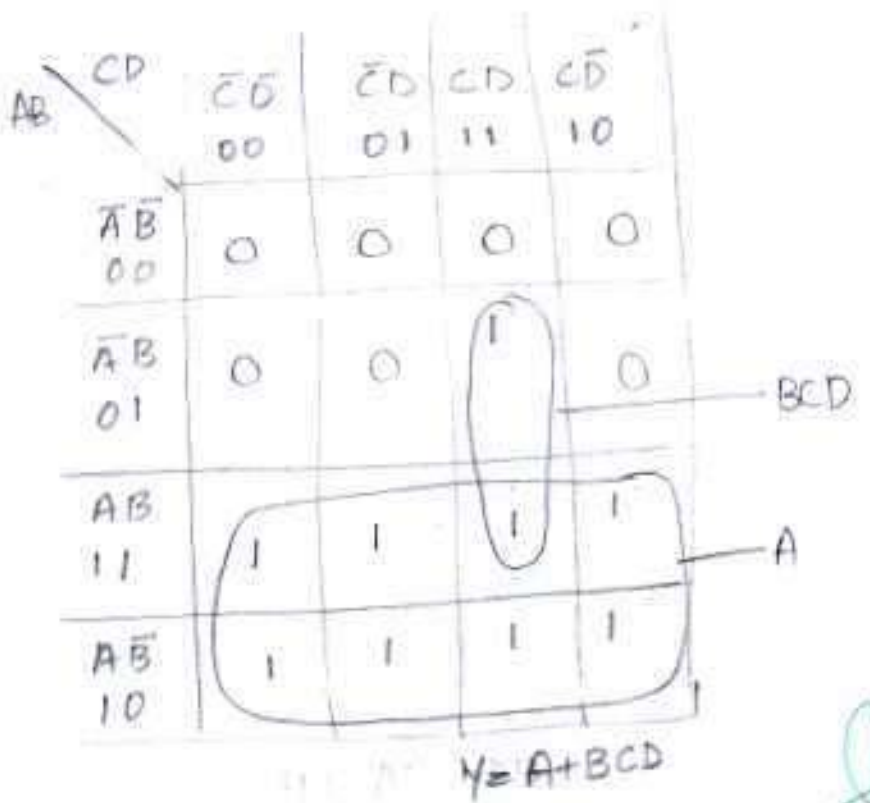
$A\bar{B}C\bar{D} + A\bar{B}C\bar{D} + ABCD + \bar{A}BCD$

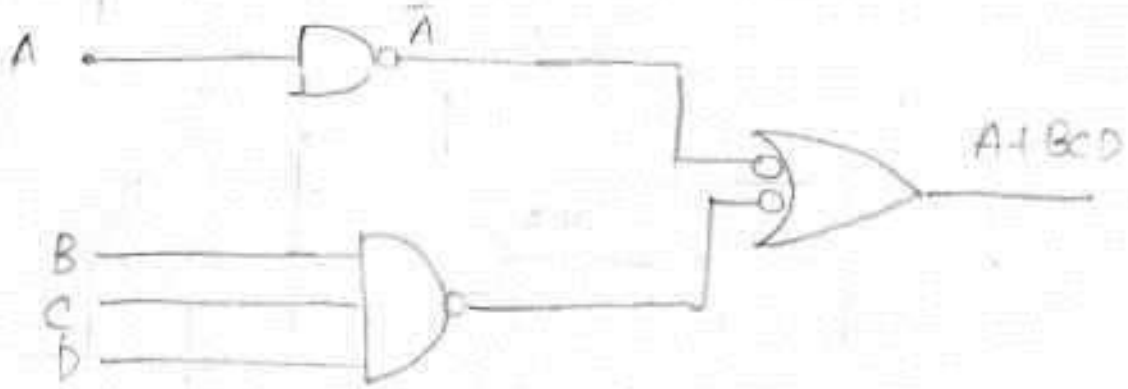
$Y = ABCD + AB\bar{C}D + A\bar{B}CD + A\bar{B}\bar{C}D + ABC\bar{D} + AB\bar{C}\bar{D} + \bar{A}BCD$

$+ A\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D}$

$= 15+13+11+9+14+12+7+10+8$

$= \Sigma m(7,8,9,10,11,12,13,14,15)$





b) What is hamming code and encode data bits 0101 into a 7 bit even parity hamming code.

Sol Hamming code not only provides the detection of bit errors, but also identifies which is in error so, that it can be corrected.

Thus, Hamming code called error detecting and correcting code.

Example: 0101

$2^P \geq m+P+1$

$2^3 \geq 4+2+1$

$4 \geq 7$

6	5	4	3	2	1
110	101	100	011	010	001
0	1	P_3	0	P_2	P_1

$P_1 = \{1,3,5\} = P_1+0+1=1$

$P_2 = \{2,3,6\} = P_2+0+01=0$

$P_3 = \{4,5,6\} = P_3+1+0=1$

Hamming code:-

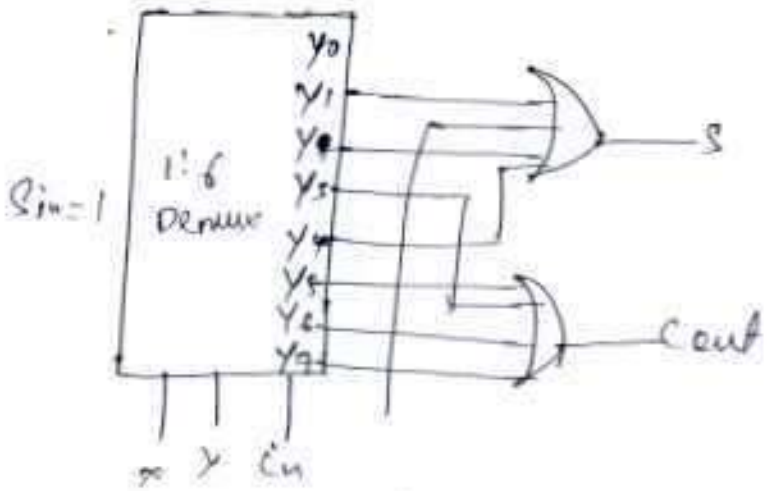
011001

For full adder, the expression for Sum (S) and Carry out (Cout) can be written from above table as

$$S = \sum m(1,2,4,7)$$

$$Cout = \sum m(3,5,6,7)$$

The above full adder expressions are implemented using 1:8 demultiplexer as shown in the figure. In the figure, Sin=1 will be sent to the respective output of demultiplexer, depending on the values of x, y and Cin then after the corresponding outputs are ored together to obtain required outputs.



) write a short note on priority encoder:

The truth table of 4-input priority encoder is shown in table.

inputs				outputs		
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

Truth table of 4-input priority encoder

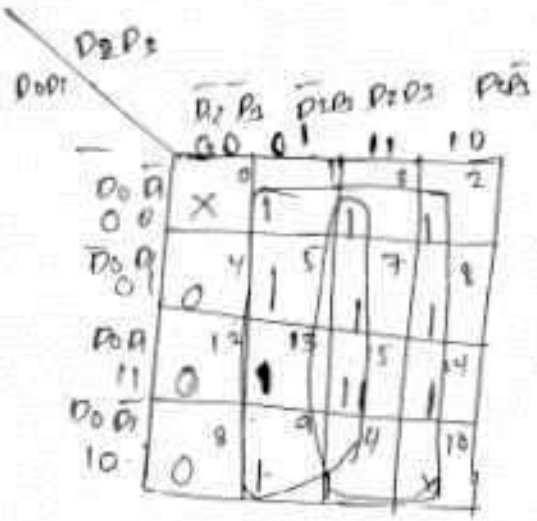
47

From the above table, the input D_3 has the highest priority where as, the input D_0 has lowest priority.

The output 'V' represents the 'valid bit indicator' It goes HIGH (i.e. 1) when one or more input goes High (i.e. 1)

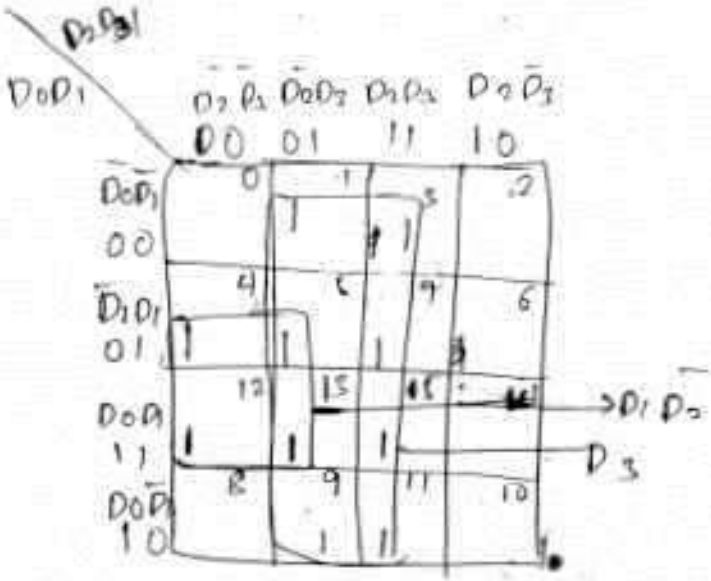
The expressional for the corresponding and output variables can be obtained by employing K-map method as

K-map for x



$\therefore x = D_2 + D_3$

K-map for y.



$\therefore y = D_3 + D_1\bar{D}_2$

Therefore, the output expressions are

$x = D_2 + D_3$, $y = D_3 + D_1\bar{D}_2$

and $V = D_0 + D_1 + D_2 + D_3$ (i.e. $V = 1$, when any of the i/p is 1)

Assignment Questions-II

(Assignment Questions are mapped with CO's, BT)

1.a)Explain in detail lok ahead carry generator. (Comprehension)(C214.3)

b)What is decoder. (Synthesis) (C214.3)

2.a)Design the full adder circuit using decoder and demultiplexer. (Synthesis) (C214.3)

b)Write a short note a priority encoder. (Knowledge) (C214.3)

3.a)Compare combinational and sequentional circuits. (Analysis) (C214.4)

b)Explain the clocked JK-flipflop with truth table. (Comprehension)(C214.4)

4.a)What is counter?Give the different between synchronous and asynchronous counters. (Synthesis) (C214.4)

b)Draw the circuit diagram of 4-bit ring counter using D-flipflops and explain its operation with the help of bit pattern. (Knowledge)(C214.4)

5.a)what is buffer registers. (Synthesis) (C214.6)

b)Explain the operations SIPO,PISO,SISO,PISO shift registers. (Comprehension) (C214.6)

6.a)Explain in detail about RAM. (Comprehension) (C214.5)

b)Draw and explain the block diagram of PLA.. (Knowledge)(C214.5)

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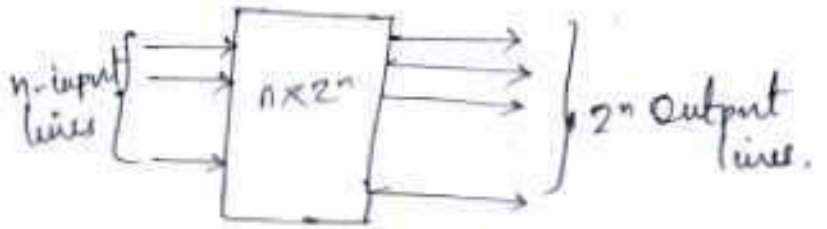
Assignment

1) What's decoder?

Decoder: A decoder is a combinational circuit which has 'n' number of input lines and 2^n number of output lines. It converts an n-bit binary input code into a 2^n unique output lines. The logic symbol of a decoder is as shown:



2a) Design the full adder circuit using decoder and demultiplexer.

Full Adder circuit using decoder.

A full adder circuit of three inputs A, B, C and two outputs So and Co. The truth table of a full adder is as shown in the table.

Inputs			Outputs	
A	B	C	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1

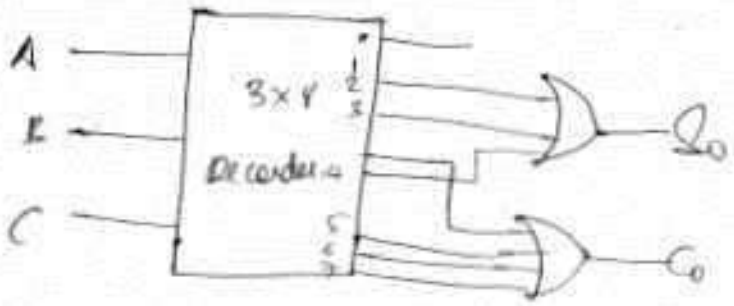
Truth table of full-adder.

The outputs S_0 and C_0 can be expressed in Boolean functions as:

$S_0(A,B,C) = \Sigma[(0,0,1),(0,1,0),(1,0,0),(1,1,1)] = \Sigma(1,2,4,7)$

$C_0(A,B,C) = \Sigma[(0,1,1),(1,0,1),(1,1,0),(1,1,1)] = \Sigma(3,5,6,7)$

The above functions are realized using a 3×8 decoder and two OR gates as shown in figure (2).



Fig(2): Realization of a Full Adder using a decoder and two OR Gates.

Design Full Adder Circuit using Demultiplexer.

The full adder circuit using Demultiplexer. This is implemented by using a 1×8 demultiplexer and OR gates

Consider the truth table of full adder as shown in below table.

X	Y	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4a) Explain in detail about RAM.

A memory unit is a collection of storage cells together with associated circuits needed to transfer information in and out of the device. The name random-access memory abbreviated RAM.

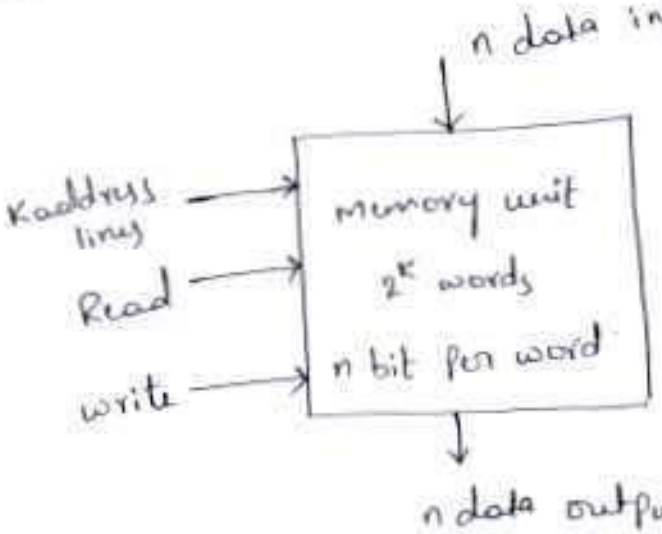


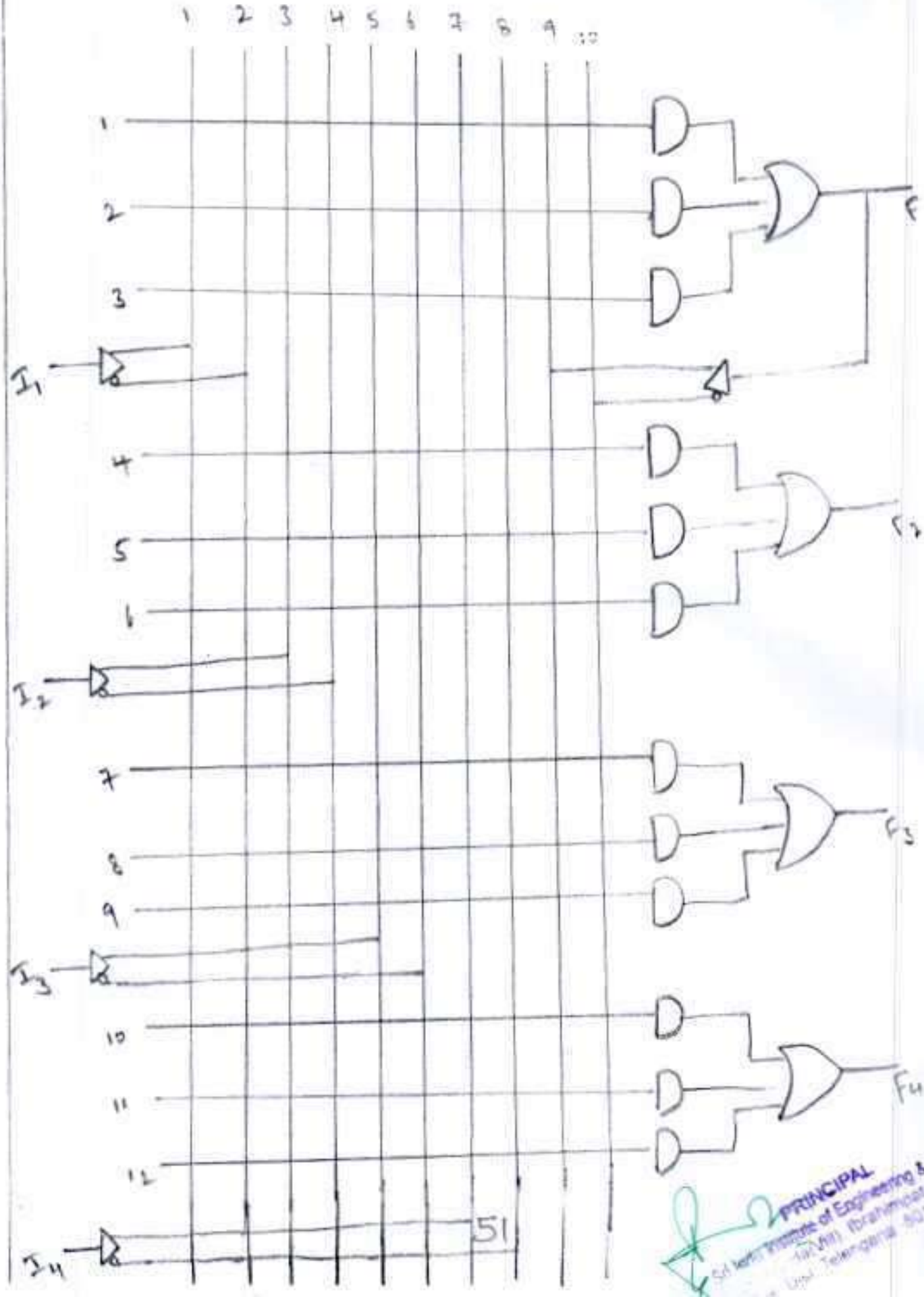
fig: Block diagram of memory unit.

The two operations that a RAM can perform are the write and read operations.

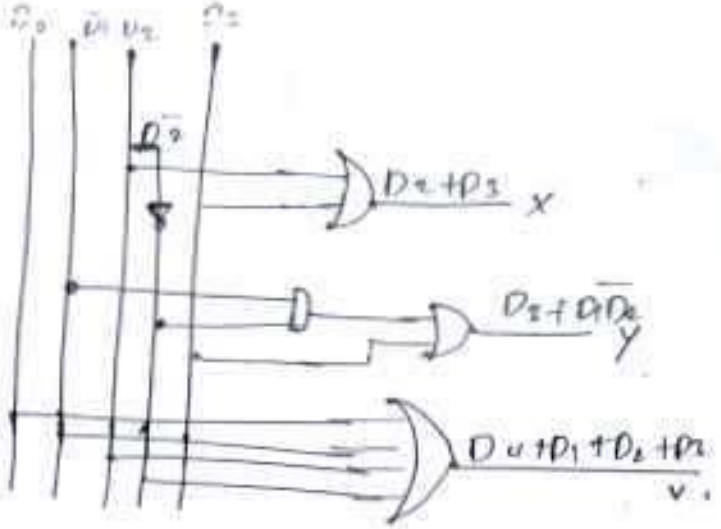
The steps that must be taken for the purpose of transferring a new word to be stored into memory as follows:

1. Apply the binary address of the desired word to the address lines.
2. Activate the write input.

4.b) Explain briefly about PAL draw its structure.



The logic diagram of a 4-input priority encoder is obtained by using gate ①, ② & ③ as shown in figure.



9.

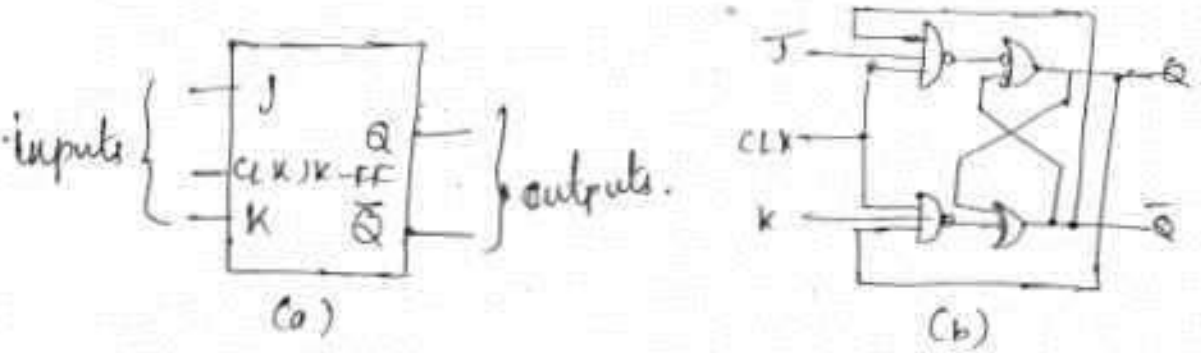
a) Compare combinational & sequential circuit

The comparision between sequential and combinational circuits is mentioned below.

Combinational logic circuits	Sequential logic circuits
1. output depends only on the present input.	1. output depends on the present input and past output also.
2. Easier to design.	2. Comparatively harder to design.
3. Speed of operation is high.	3. Speed of operation is comparitively low.
4. Memory unit is not required.	4. Memory unit is required to store past outputs.
5. Example: Parallel Adder.	Ex: Serial adder.

b) Explain the clocked JK flip-flop with truth table.

JK Flip-flop: The logic symbol and circuit diagram of JK-flipflop is as shown in the figure(1).



where - J, K - data inputs

CLK: Clock input

Q: Normal output

$\bar{Q}$: Complementary output.

The truth table of JK-flipflop is as shown in the table.

	Inputs				Outputs	
Operating Mode	CLK	J	K	Q	Q	Effect on output Q.
Hold	⊓	0	0	No change	No change	No change / Disable
Reset	⊓	0	1	0	0	Reset (i.e. cleared to 0)
Set	⊓	1	0	1	1	Set to 1
Toggle	⊓	1	1	Toggle	Toggle	Changes to opposite state (i.e. from 0 to 1 (or) 1 to 0).

working:

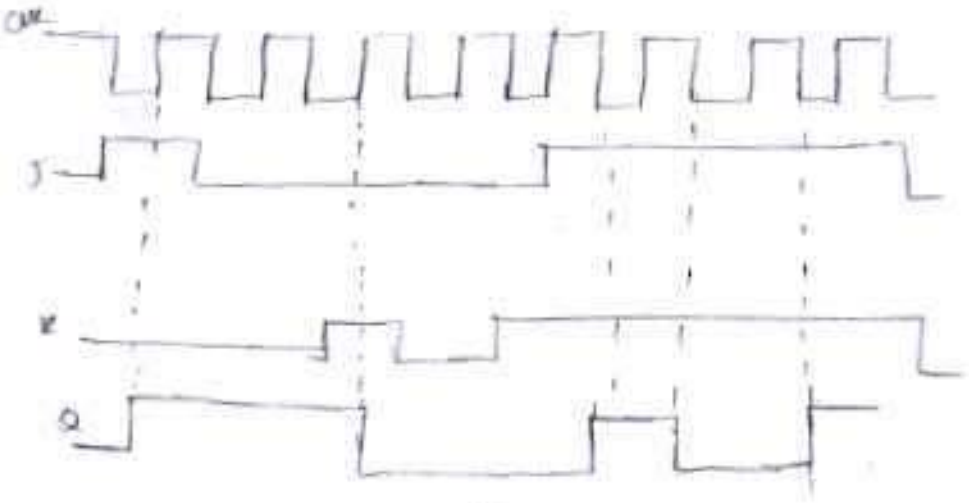
Case i: If both the inputs JK-flip-flop are '0' (i.e., J=K=0), then the flip flop enters into hold mode. In this mode, output remains same as that at the previous state (i.e., no change in the output.)

Case ii: If J=0, K=1. then the flipflop enters into reset mode. In the reset mode, the data inputs reset the output 'Q'. Thus the outputs are Q=0, $\bar{Q}$=1.

Case iii: If J=1, K=0, then the flip flop are '1' (i.e., J=K=1) then the flip flop enters into toggle mode, in which, output continuously shift between logic '0' and logic '1' for complete clock pulse. Thus certain output is obtained.

Timing diagram:

The timing diagram of JK-flip-flop is as shown in figure (2)



Elimination of race around condition.

In JK – flip flop, the condition in which output circuit more than once between 0 & 1 during a single clock pulse is referred to as "race around condition". (or problem) To understand it consider a JK flip flop as shown in the figure (1).

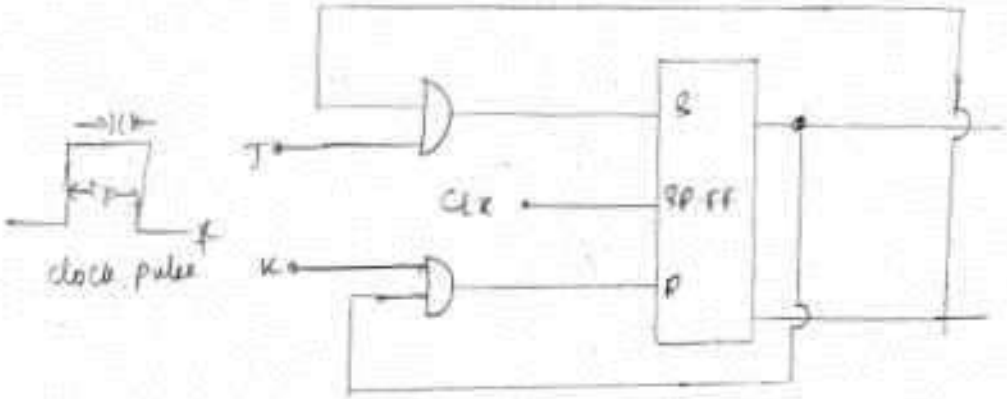
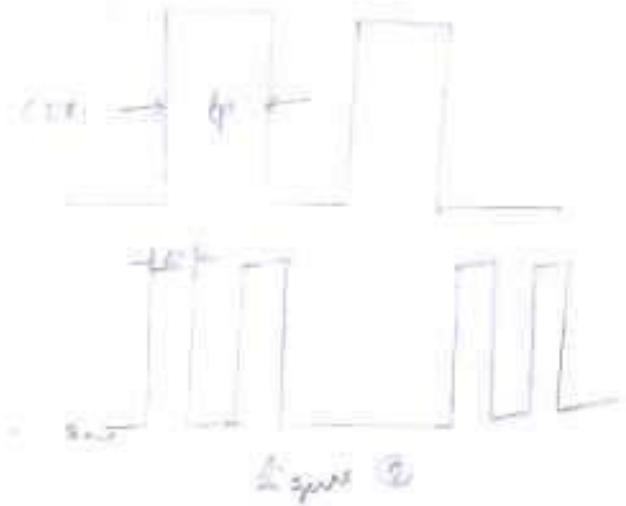


figure (1)

In the above figure, consider that the initial output for input J=K=1 is '0' (i.e, Q=0) when a clock signal of pulse width 'tp' is applied to flip flop, after a time duration of Δt output of the circuit changes to '1' (i.e, Q=1). This interval of Δt specifies the propagation delay due to the logic gate. If tp > Δt, then the output changes again from '1' to '0' after another Δt as shown in fig (2). This process continue till the end of the clock pulse, which results in an uncertain value at the output. This situation of changing output value is known as race around condition (i.e. output varies from '0' to 1 and 1 to '0'). This condition can be overcome by



4) What is a counter? Give the difference between Synchronous and asynchronous.

Counter: A Sequential circuit which counts the no of clock pulses is known as 'Counter'.

Classification of Counters:

Counters are classified into 2 types. they're:

1. Synchronous Counter
2. Asynchronous Counter (Ripple Counter)

The Comparision between Synchronous and asynchronous Sequential circuits is mentioned below:

Asynchronous Sequential circuits	Synchronous Sequential circuits
1. In asynchronous Sequential circuits, input signals affect memory elements at any instant of time.	1. In Synchronous Sequential circuits input signals can affect memory elements at discrete instances of time.

Asynchronous Sequential circuits	Synchronous Sequential circuits
2. These circuits are complex to design.	2. These circuits are simple to design.
3. In this circuit, clock is not required.	3. Here clock is required as one of the input.
4. In this circuit, the speed of operation is high.	4. In this circuit, the speed of operation is limited by the time delays involved.
5. Ex: unclocked flipflops	5. clocked flipflops.

b. Draw the circuit diagram of a 4-bit ring counter using flip-flops and explain its operation with the help of bit pattern.

Ring counter: A ring counter is also known as circular shift register. It is used to control the sequence of operation of digital system by using timing signals. In this counter, output of each stage is connected to the input of the succeeding stage. The output of the last flip flop is connected as data input to the first flip flop. The circuit diagram of a ring counter is shown in fig (a).

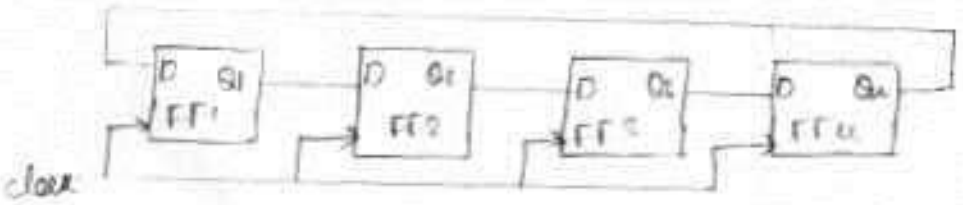


Fig (a)

In the above figure, clock pulse is applied to all the flip flops simultaneously.

working:

Initially, at any given point of time, only one flip flop is set and the remaining flip flops are cleared. i.e, is set and the remaining flipflops are 0001. After the first clock pulse, 1 in LSB is shifted to second flipflop i.e., FF2 and the counter output is 0010. After this counting continues till the counter counts 1000 at 4th clock pulse. The counting sequence of the ring counter is shown in table.

Clock	Counter			Sequence
	Q_4	Q_3	Q_2	Q_1
0	0	0	0	1
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	1	0	0	0

table

The timing diagram of a ring counter is shown in fig (2).

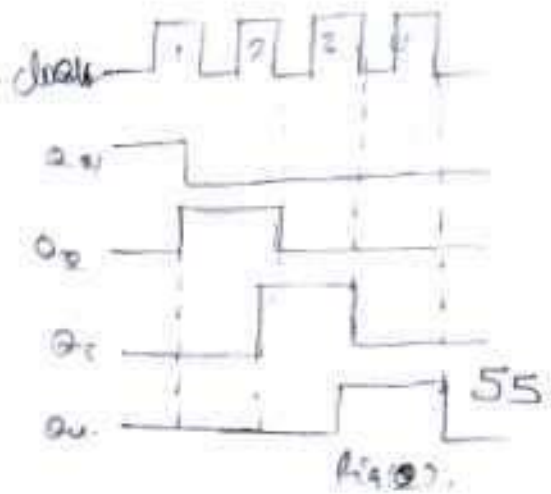


Fig (2).

5a) what's a buffer register?

Buffer registers are a type of register used to store a binary word. these can be constructed using a series of flipflops as each flip flop can store a single bit. This means that in order to store an n-bit binary word one should design an array of n flip flops binary word figure 1 shows a 4 bit synchronous buffer register formed by cascading four positive edge triggered D flip-flops. Here the entire input data word $B_3 B_2 B_1 B_0$ is loaded into the register at a single clock tick This means that at every leading edge of the clock tick this means that at every leading edge of the clock the value of flipflop outputs follow their input bits i.e $Q_1 = B_1$, $Q_2 = B_2$, $Q_3 = B_3$ & $Q_4 = B_0$.

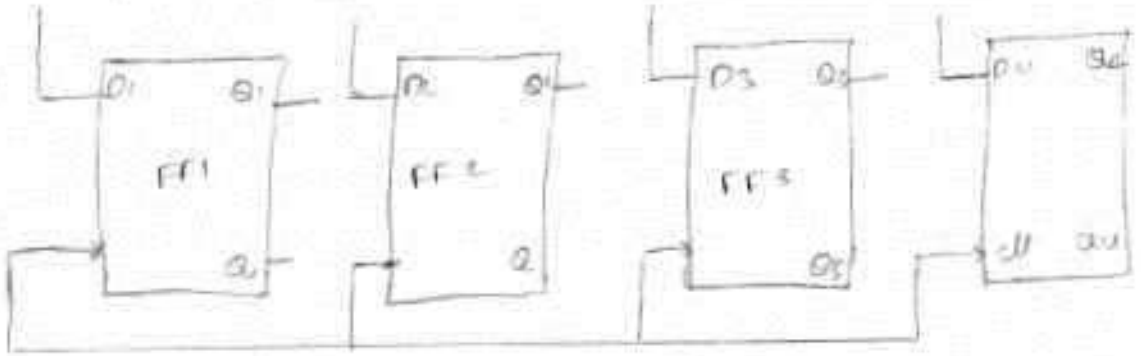


Fig 1 4-bit Buffer register

b) Explain the operation of SIPO and CLEOO, PISO, PIPO shift registers.

1. Serial-in out (SISO) shift Register.

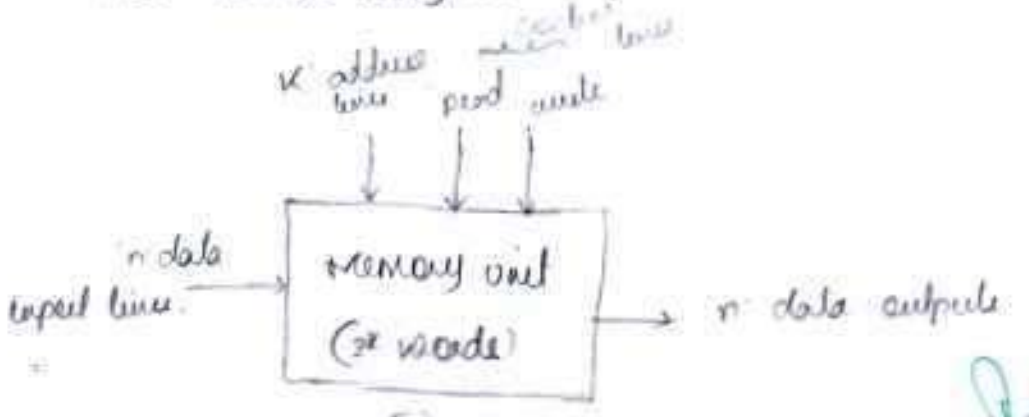
6a) Explain in detail about RAM.

RAM is an acronym for random access memory. This type of memories can be used to perform both read & write operations.

It is possible to access all the memory locations in the RAM at the same speed to perform both read and write operations. RAM is a volatile memory, hence it stores data temporarily. It stores data related to program instructions and intermediate result of the program that are used temporarily.

The data stored in the RAM can be read as many numbers of times as possible. A new data, which is written in the any of RAM locations, over writes the existing data present in those locations.

The block diagram of a RAM is as shown in figure.



Figure

A random access memory unit contains in put lines, address lines, selection lines and control lines as shown in the figure.

The 'n' data input lines are used to write the binary information to be stored in the memory, when the control line is active.

The 'n' data output lines are used to read (write) the information stored in the memory, when the condition, read is active.

The 'k' address lines are used to select a specific word location (among the 2^k words of memory) to which information has to be written or from where information has to be read.

Salient Features of RAM:

1. Ram is a volatile memory (i.e., it looses the stored information on power cut)

2. A RAM basically performs two operations. They are:

1) Read: The process in which stored information is transferred outside the memory is called read operations.

2) write: The process in which new information is stored in the memory is known as write operation.

3. Based on the mode of operation. RAMs are classified as:

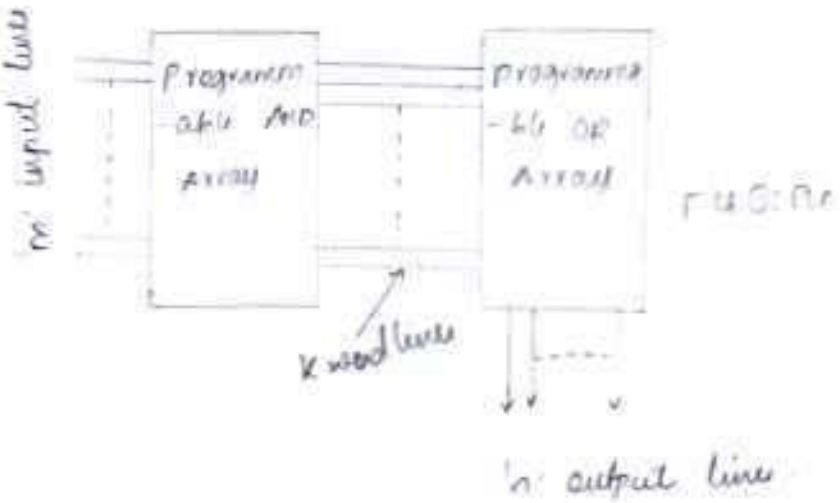
i) Static RAM (SRAM): The RAM in which stored information is valid only when Power is available is static RAM. It is made of internal latch

iii) Dynamic RAM (DRAM): The RAM in which binary information is stored as electric charge on capacitors is known as dynamic ram. The discharge capacitor with time leads to the discharge of stored information. By recharging the capacitor the stored information can be retrieved.

b) Draw and explain the block diagram of PLA.

The Programmable Logic Array (PLA) is a combinational logic device, containing a two level programmable 'AND' and programmable 'OR' array logic.

The block diagram of PLA with 'm' inputs and 'n' outputs is as shown in the figure (1).



The PLAs are programmed in order to achieve sum of product logic expressions.

In PLA, an array of 'AND' gates produce the product term of the applied inputs, and an array of 'OR' gates produce the "sum of products" logical expression.

i.e., $f_1 = PQ + PR$

$f_2 = Q'R + P'R'$

$f_3 = PQ + PR'$

$f_4 = PR$

Then, the corresponding PLA programing table is shown in the table.

product term	Inputs			Outputs			
	P	Q	R	f_1	f_2	f_3	f_4
PQ	1	1	-	1	0	1	0
Q'R	-	0	1	0	1	0	0
PR	1	-	1	1	0	0	1
PR'	1	-	0	0	1	1	0

Table: PLA programmable table.

The internal gate level structure of PLA for three inputs and four outputs boolean expression is as shown in fig ⑤.

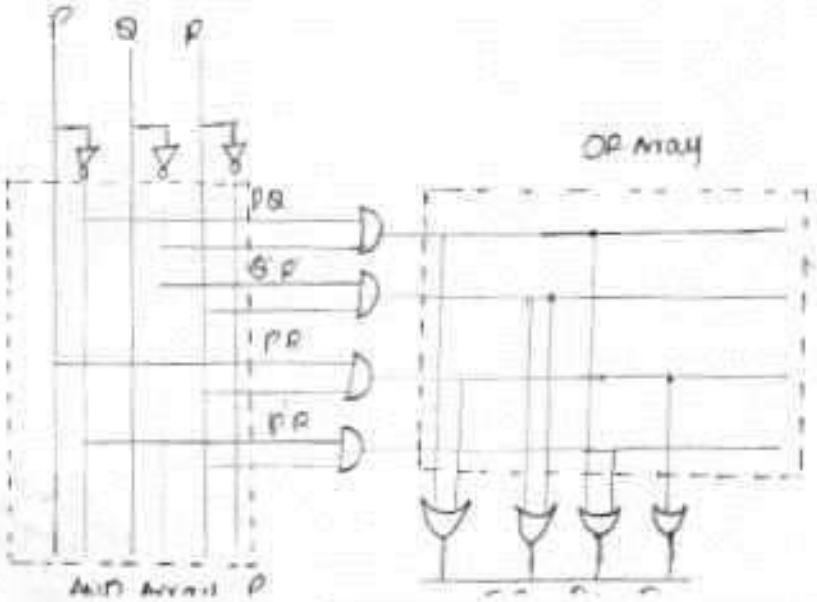


Fig ⑤ Internal structure of PLA

The inputs, P, Q and P are applied to the buffer to produce its Complement

The respective values are given as inputs to the AND gates to produce the "product terms".

The outputs from the (AND) array are given as inputs to the (OR) array. Thus, the output produced by the 'OR' gates is the 'Sum of product' terms.

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Computer Science and Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty : Dr.K.S.Sadasiva Rao Academic Year: 2018-19

Branch & Section: II-CSE-B Examination: I Internal

Course Name: **DIGITAL LOGIC DESIGN** Year: II Semester: I

S.No	HT No.	Question No.												Obj1	A1
		Q1a	Q1b	Q1c	Q2a	Q2b	Q2c	Q3a	Q3b	Q3c	Q4a	Q4b	Q4c		
Max. Marks ⟹		2	2	1	3	2		2.5	2.5		5			10	5
1	17X31A0563	1	2	1				2	2					10	5
2	17X31A0564	1	1	0										9	5
3	17X31A0565	1	1	1	3	2								9	5
4	17X31A0566	0	1		2	2								4	5
5	17X31A0567		1	1	3	2								10	5
6	17X31A0568	0	2		3	2								4	5
7	17X31A0569	1	1	1										7	5
8	17X31A0571	0	1	0	1	2								9	5
9	17X31A0572				2									2	5
10	17X31A0573	1	1		3	2								2	5
11	17X31A0574	1	1		2	2								9	5
12	17X31A0575				2	2		2	2					10	5
13	17X31A0576		1	1	2	2								9	5
14	17X31A0577	0	0	0	2	0								2	5
15	17X31A0578	1	0	0										10	5
16	17X31A0580				3	2		2	2					10	5
17	17X31A0583				3	2		2	2					10	5
18	17X31A0584				3	2								8	5
19	17X31A0586	2	2	1	3	2								10	5
20	17X31A0587	0	1	0	3	2								10	5
21	17X31A0589	0	1	0										8	5
22	17X31A0590	2	1	0	2	2								9	5
23	17X31A0591	1	1	1				2	1					10	5
24	17X31A0592				3	2		3						9	5
25	17X31A0593	1	1	1	3	2								9	5
26	17X31A0594	2	1	1	3	2								10	5
27	17X31A0595	0	1	1	1	2								4	5
28	17X31A0597	0	1	0				1	1					7	5
29	17X31A0598				3	2		2	2					5	5
30	17X31A05A0	0	1		3									3	5
31	17X31A05A1	1	1	1	1	2								9	5
32	17X31A05A3	0	0	0	2									4	5
33	17X31A05A4	2	1	1	3	2								10	5
34	17X31A05A6	2	2	1	3	2								10	5
35	17X31A05A7	0	1	1										2	5
36	17X31A05A8				3	2		2	2					9	5
37	17X31A05A9	1	2	1	2	2								9	5
38	17X31A05B0	2	2	1	3	2								9	5
39	17X31A05B1	0	1	1	3	2								10	5

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40	17X31A05B3	0	1	0	2									6	5
41	17X31A05B4	2	1	1				1	1					9	5
42	17X31A05B5				3			1						10	5
43	17X31A05B6				2	2		1	1					9	5
44	17X31A05B7	0												8	5
45	17X31A05B8	1	1	1										10	5
46	17X31A05B9	2	1	1	3									10	5
47															
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Performance Target set by the faculty / HoD	60%	60%	60%	60%	60%	60%	60%	60%	60%	60%	60%	60%	60%	60%	
Number of students performed above the target	8	6	20	32	28	0	8	6	0	0	0	0	35	46	
Number of students attempted	34	35	30	35	29	0	12	10	0	0	0	0	46	46	
Percentage of students scored more than target	24%	17%	67%	91%	97%		67%	60%					76%	100%	

CO Mapping with Exam Questions:

CO - 1	Y	Y	Y	Y	Y								y	y
CO - 2							Y	Y		Y			y	y

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CO - 3													y	y
CO - 4														
CO - 5														
CO - 6														

CO Attainment based on Exam Questions:

CO - 1	24%	17%	67%	91%	97%								76%	100%
CO - 2							67%	60%					76%	100%
CO - 3													76%	100%
CO - 4														
CO - 5														
CO - 6														

CO	Subj	obj	Asgn	Overall	Level
CO-1	59%	76%	100%	78%	2
CO-2	63%	76%	100%	80%	2
CO-3		76%	100%	88%	3
CO-4					
CO-5					
CO-6					

Attainment Level	
1	60%
2	80%
3	>80%

Overall Course Attainment = 2.33

Faculty

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SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Computer Science and Engineering

Course Outcome Attainment (Internal Examination-2)

Name of the faculty : K.S.Sadasiva Rao
Academic Year: 2018-19

Branch & Section: CSE-B
Examination: II Internal

Course Name: DIGITAL LOGIC DESIGN
Year, II InterSemester: I

S.No	HT No.	Question No.												Obj2	A2
		Q1a	Q1b	Q1c	Q2a	Q2b	Q2c	Q3a	Q3b	Q3c	Q4a	Q4b	Q4c		
Max. Marks ==>		3	2		2	3		3	2		2	3		10	5
1	17X31A0563	3	2		2	3								8	5
2	17X31A0564				2	1					2			8	5
3	17X31A0565	3	2		2	2								9	5
4	17X31A0566	3	1								1	2		5	5
5	17X31A0567	3	2		2	2								9	5
6	17X31A0568	3	2								2	1		6	5
7	17X31A0569	3	2		2	3								9	5
8	17X31A0571	3	2		2	3								9	5
9	17X31A0572	1	1								1			6	5
10	17X31A0573	3	2		2	1								8	5
11	17X31A0574				2	2					2			9	5
12	17X31A0575	3	2		2	2								9	5
13	17X31A0576	3	2								2			7	5
14	17X31A0577														
15	17X31A0578	2									2			7	5
16	17X31A0580	3	2								2	2		9	5
17	17X31A0583	3	2								2			7	5
18	17X31A0584	3	2		2	1								3	5
19	17X31A0586	3	2		2	1								6	5
20	17X31A0587	3	2		2	3								9	5
21	17X31A0589	3	2		2									8	5
22	17X31A0590	3	1								2			9	5
23	17X31A0591	1									2	1		4	5
24	17X31A0592	3			2	3								7	5
25	17X31A0593	3			2	3								7	5
26	17X31A0594	3	2		2	2								9	5
27	17X31A0595	2												6	5
28	17X31A0597	3	2								2			8	5
29	17X31A0598	3	2		2									8	5
30	17X31A05A0														
31	17X31A05A1	3	2		2	1								9	5
32	17X31A05A3	2									2			6	5
33	17X31A05A4	3	2								2	1		8	5
34	17X31A05A6	3	2		2	3								9	5
35	17X31A05A7	2									2			7	5
36	17X31A05A8	3	2		2	2								6	5
37	17X31A05A9	3	2								2	3		8	5
38	17X31A05B0	3	2								2			9	5
39	17X31A05B1	3	2		2	3								9	5
40	17X31A05B3	1	1		2									6	5
41	17X31A05B4	3	2								2			9	5
42	17X31A05B5				2	1					2			8	5
43	17X31A05B6	3	2		2	1								9	5

62

44	17X31A05B7				2	1					2	1		8	5
45	17X31A05B8	3	2								2			6	5
46	17X31A05B9	3	2		2	1								6	5
47															
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72															
Performance Target set by the faculty / HoD		60%	60%	60%	60%	60%	60%	60%	60%	60%	60%	60%	60%	60%	60%
Number of students performed above the target		37	29	0	26	14	0	0	0	0	19	3	0	32	44
Number of students attempted		40	33	0	26	23	0	0	0	0	21	7	0	44	44
Percentage of students scored more than target		93%	88%		100%	61%					90%	43%		73%	100%

CO Mapping with Exam Questions:

CO - 1														
CO - 2														
CO - 3	Y	Y												
CO - 4				Y	Y								y	y
CO - 5										Y	Y		y	y
CO - 6							Y	Y					y	y

CO Attainment based on Exam Questions:

CO - 1														

CO - 2														
CO - 3	93%	88%												
CO - 4				100%	61%								73%	100%
CO - 5										90%	43%		73%	100%
CO - 6													73%	100%

CO	Subj	obj	Asgn	Overall	Level
CO-1					
CO-2					
CO-3	90%			90%	3
CO-4	80%	73%	100%	84%	3
CO-5	67%	73%	100%	80%	2
CO-6		73%	100%	86%	3

Attainment Level	
1	60%
2	80%
3	>80%

Overall Course Attainment = 2.75

Faculty

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TUTORIAL TOPICS **SUBJECT:DIGITAL LOGIC DESIGN**

S.NO	Unit	TOPIC	Number of Sessions Planned	Teaching method/Aids	REFERENCE
1	1	Octal, Hexadecimal	1	Black Board	T1
2		Floating point number representation	1	Black Board	T1,W1
3		Hamming Code	1	Black Board	T1
4		Digital Logic Gates	1	Black Board	T1,W1
5	2	Four-Variable Map	1	Black Board	T1
6		sum of products , product of sums simplification	1	Black Board	T1
7		Five -Variable Map	1	Black Board	T1,W2
8		NAND and NOR implementation	1	Black Board	T1
9	3	Binary Adder-Subtractor	1	Black Board	T1,W2
10		Magnitude Comparator	1	Black Board	T1
11		Combinational circuit	1	Black Board	T1
12		Binary Multiplier	1	Black Board	T1
13	4	Flip-flops, analysis of clocked sequential circuits	1	Black Board,PPT	T1,W3
14		Registers, Shift registers, Ripple counters	1	Black Board,PPT	T1
15	5	Programmable Logic Array	1	Black Board	T2,W3
16		Programmable Array Logic	1	Black Board	T2,W3

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TEXT BOOKS:

1. Digital Design, M. Morris Mano, M.D.Ciletti, 5th edition, Pearson.(Units I, II, III, IV, Part of Unit V)
2. Computer System Architecture, M.Morris Mano, 3rd edition, Pearson.(Part of Unit V)

REFERENCE BOOKS:

1. Switching and Finite Automata Theory, Z. Kohavi, Tata McGraw Hill.
2. Fundamentals of Logic Design, C. H. Roth, L. L. Kinney, 7th edition, Cengage Learning.
3. Fundamentals of Digital Logic & Micro Computer Design, 5TH Edition, M. Rafiquzzaman, John Wiley.

WEB REFERENCES

W1 :https://www.logicdesign.co.uk/

W2:https://www.wiziq.com/tutorials/digital-logic-design

W3:www.nptel.iitm.ac.in

Faculty Signature

(E.Rupa)
(Asst.Prof/CSE, SIIET)

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2.2.1:Assess Learning Levels, Special programs for adv& Slow learners

Result Analysis:

Course Title	DIGITAL LOGIC DESIGN
Course Code	CS304ES
Programme	B.Tech
Year & Semester	IIyear I-semester, B- sec
Regulation	R16
Course Faculty	Dr.K.S.Sada Siva Rao, Professor , CSE

Weak Students:

S No	Roll no	No of backlogs	Internal-I Status	Internal-II Status
1	17X31A05B8	8	18-P	18-P
2	17X31A0567	6	22-P	23-P
3	17X31A0572	5	14-P	14-P
4	17X31A05A0	5	17-P	5-F
5	17X31A0564	5	16-P	18-P
6	17X31A0589	4	14-P	20-P
7	17X31A0590	3	20-P	20-P
8	17X31A0573	3	20-P	21-P
9	17X31A0576	3	20-P	19-P
10	17X31A05A1	3	20-P	22-P

Advanced learners:

S No	Roll No	(SGPA)	Gate Material
1	17X31A05B0	8.2	Number Conversion, Compliments, Combinational and sequential circuits, Minimization Logical Gates, Flip-Flops,Memory
2	17X31A0565	7.5	
3	17X31A05A6	7.3	
4	17X31A05A4	7.1	
5	17X31A0569	7.0	

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GATE MATERIAL

1. Convert the following:a)(110.011)2=(X)10 b)(1118)10=(Y)H

2. What is the gray code word for the binary number (101011)

3. The hexadecimal representation (657)8

4. The minimum number of NAND gates required to implement the Boolean function A+AB'+AB'C is equal to

5. A 32-bit wide main memory unit with a capacity of 1 GB is built using 256M ×4-bit DRAM chips. The number of rows of memory cells in the DRAM chip is 2^{14}. The time taken to perform one refresh operation is 50 nanoseconds. The refresh period is 2 milliseconds. The percentage (rounded to the closest integer) of the time available for performing the memory read/write operations in the main memory unit is .

6. Convert f(x)=x+y'z into canonical form?

7. Simplify to a sum of 3 terms: A'C'D'+AC'+BCD+A'CD'+A'+AB'C'

8. An SR flip flop is converted to _____ flip flop by inserting an inverter between S and R by assigning a single input.

9. Find the 7's complement of 65402(Octal Number)

10. (2FA0C)16 is equivalent to

11. The binary equivalent of (0.6875)10

12. The octal equivalent of(0.513)10

13. The complementary of the function F=X'YZ+X'Y'Z is F' ,where F' is

14. Considera 3 bit error detection and 1 bit error correction hamming code for 4 bit data.The extra parity bits required would be _____,and to detect 3 bit error,the minimum distance of the code should be_____

15. In 2's complementarithmetic ,explain the condition for overflow.

16. Following 7 bit single error correcting Hamming coded message is received as1000110.Determine if the message is correct,by assuming that at most 1-bit error could be corrected.If the message contains an error ,find the bit which is erroneous and give the correct message.

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17.Zero has two representation,what are there

18.2's complement representation of (-539)10 in hexadecimal is

19.What is equilvalent value for the decimal value 0.25

20.2's complement representationof decimal value(-15) is

21.Perform (11101100)2 – (00110010)2

22.Add the octal numbers$(341)_8$,$(125)_8$,$(472)_2$,$(577)_8$

23.Use the 8's complement method of subtraction to compute $(316)_8 - (451)_8$

24.Perform the excess-3 addition of 8,6.

25.The 2,764 is 65,536-bit EPROM organized as 8,192 words of 8 bits each.How many address lines does it have?

26.How many memory locations can 14 address bits access?

27.How many flip-flop circuits are needed to divide by 16?

28.What is the 2's complement of 0011 0101 1001 1100 number?

29.Convert the 1000 0000 0000 1111 signed binary to decimal number?

30.What is the hexadecimal equivalent of binary number 10101111

31.Digital design often starts by constructing a .....table.

32.The simplified form of the Boolean expression (X+Y+XY)(X+Z) is .....

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Name: G. Raga Sudha Course: B.Tech Year/Branch: IV / CSE
Subject: Cloud Computing Date: 23/11/19 Examination: Mid - II
H.T. No. 1 6 W 3 1 A 0 5 5 9 No. of Additionals 2

MARKS

Invigilator's Signature

2. Describe cloud provides Infra structure as a service

A:- Infra structure as a service :-

Cloud computing provides 3 services. they are software as a service, platform as a service, Infrastructure as a service.

1. Infrastructure as a service is provided in the form of storage room likely as data centers room and provide services to the customers or clients.
2. The computing is divided into fragments for various applications.
3. The Infrastructure as a service also provide hardware components. So, that the organizations can do whatever they want onit. They provide the resources like
   - → memory
   - → cpu cycles
   - → storage

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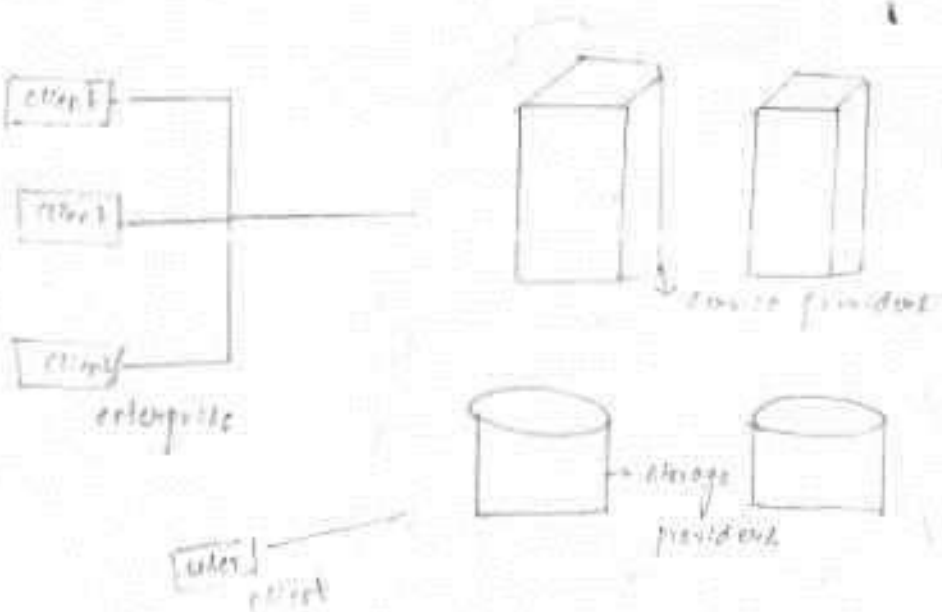

Fig:- Infrastructure as a service

4. Infrastructure as a service also provides the hardware applications to the customers.

5. Infrastructure as a service has scaled up and down according to the demand.

6. In Infrastructure as a service also client need not do anything but need to control the storage, connectivity and few applications.

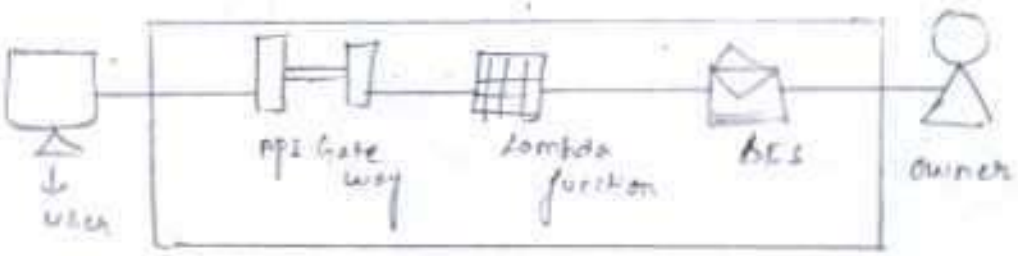

Fig:- AWS Architecture

Advantages of AWS :-

1. Easy to use.
2. No storage limits: If organizations launch any project applications they will guess what capacity they need.
3. Provide speed and agility.
4. Secure and reliable :- It is very secure and it protects the privacy as it is stored in the AWS data centers.

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Disadvantages of ABIS:-

1. Limitation for Biometrics that vary from one region to another. Biometrics include images, fingerprints
2. Limits on security

Amazon web services [aws services] :-

1. Aws is the cloud computing platform which provide services over an internet.
2. Aws provide a complete cloud service which is ready to use on any work load.
3. In Aws the user request the client by the method such as E-mail which takes all the information to amazon Api Gateway restful services.
4. Api Gateway restful service which have all the information from the user will transfer it to aws Lambda function.
5. Aws Lambda function will generate an E-mail and forward it to the 3rd party mail servers by using the SES [simple email services]

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6. The components of Amazon web services are amazon API Gateway service, aws lambda function, simple E-mail service.

7. API Gateway is the frontdoor to access the data, business applications and functionality. API provides the API end point by using aws lambda function

8. API is used for both small scale and large scale and API also helps the developers in managing, creating and securing API's.

9. AWS Lambda function runs the end point and all the information to aws lambda function will get through API Gateway.

10. Simple Email service is used to send E-mails and it is also used by monitoring inbox security

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINERING

B.TECH. IV YEAR I SEM., II Mid Term Examinations, NOVEMBER - 2019

CLOUD COMPUTING Date: 23/11/2019(FN)

Objective Exam

Name: G. Raga Sudha Hall Ticket No. 16X31A0559

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 10.

I choose the correct alternative:

1. Microsoft offers its own online collaboration tool called _____ [A]
   A) SharePoint B) Microsoft Assessment C) Microsoft planning D) All
2. Which of the following is a service models? [C]
   A) Private B) Public C) PaaS D) Hybrid
3. Manjrasoft has come up with a platform called [A]
   A) Aneka B) Rackspace C) VMware D) sales.com
4. STaaS stands for_____ [A]
   A) Storage as a service B) Software Storage as a service C) Storage as a standard
   D) Software as a service
5. _____ for both hosted on premises applications and data sources. [A]
   A) IaaS B) PaaS C) SaaS D) DaaS
6. Which of the following is associated with considerable vendor Lock-in? [B]
   A) IaaS B) PaaS C) SaaS D) CaaS
7. Which of the following is NOT Cloud application features? [D]
   A) Multitenancy B) Elasticity
   C) On-demand service D) Homogeneous cloud platform
8. Amazon EC2 is a computing service, whereas Amazon SQS and Amazon S3 are____ [B]
   A) Cloud B) Support C) Storage D) Platform
9. How many types of virtual private server instances are partitioned in an IaaS stack [A]
   A) 3 B) 1 C) 2 D)All
10. Cloud application in general refers to a _____ application [C]
    A) IaaS B) PaaS C) SaaS D) CaaS

73

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II Fill in the Blanks

11. Salesforce.com is a cloud computing and social enterprise SaaS provider based in San Francisco.
12. SOA stands for Service oriented architecture
13. Cloud anatomy cannot be considered the same as cloud architecture
14. Generally, the IaaS services are provided from the service provider cloud data center
15. The web application is not multitenant
16. In Cloud Computing the SaaS means Software as a service
17. In RAckspace, Cloud servers are provided persistent storage through RAID10 disk storage.
18. Service Model consists of the particular cloud computing platform.
19. Google cloud print is a service that extends the printers function to any device that can connect to the Internet
20. Conjunction is an enabling technology for peer to peer interaction
controll.

6.5.2 (Student evaluation process)

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Sheriguda (V), Ibrahimpatnam (M), R.R. Dist. Telangana - 501 510.
Approved by AICTE, New Delhi and Affiliated to JNTUH.

10
10

MARKS

Name: G. Raga Rudha Course: BTech Year/Branch: IV / CSE

Subject: CC Date: 17/9/19 Examination: Mid - I

H.T. No. 1 6 X 3 1 A 0 5 5 9 No. of Additionals 02

Invigilator's Signature

1. Define cloud computing and explain advantages and disadvantages of cloud Computing?

A:- **cloud Computing:-**

Cloud computing refers to storing and accessing data through or over an internet. It doesn't store the data in the hard disk of personal computer. cloud computing is based on service providers.

cloud computing is the internet based computing i.e the application doesn't access the resources directly, rather it provides the resourcepool through shared resources. It is the break down for "pay and use what you want". The resource units are managed centrally and placed in the location based servers in clusters. cloud computing can be

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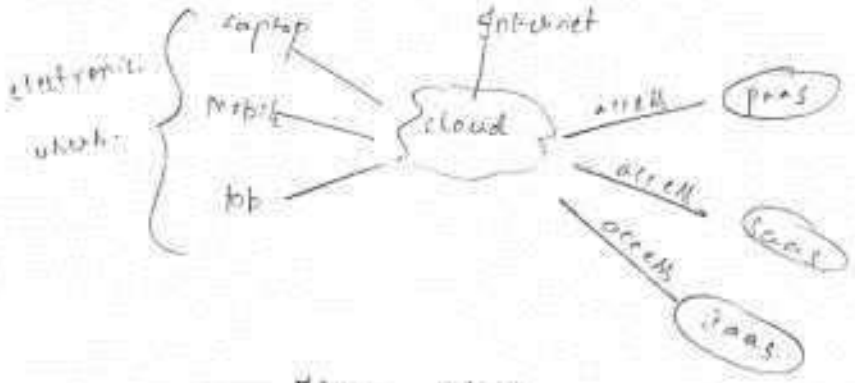

Fig :- cloud

advantages of cloud computing :-

1. Cost :- The major benifit of cloud computing is cost. It required low cost as we do Not Need to invest on Hardware.

2. Backup and restore data :- once the data is stored in the cloud the data can be easily restored and we can also easily backup the data.

3. Unlimited storage capacity :- The cloud provided unlimited storage capacity. The storage capacity is limitless in cloud.

4. Reliability :- It is one of the major advantage of cloud computing. The Reliability is nothing but we can easily get updated on the changes that are made.

5. mobility :- From cloud we can easily access data if we have Internet. If we are in remote places or Nearer locations then it is very easy to access data over an Internet.

6. High Speed :- deploy the Services in quality in fewer clicks.

Disadvantages of cloud computing :-

Security :- When different organizations are accessing data from one cloud there is chance for the third party member to access the data.

Technical :Much :- We can Not access the data

Performance can vary:- The performance can change depending upon the internet connection.

3. Explain the cloud deployment models.

A:- There are 4 deployment models in cloud computing. They are:-

1. private cloud
2. public cloud
3. Hybrid cloud
4. Community cloud.

① private cloud:-

Private cloud is managed by only one organization. The single organization owns and manages the private cloud within its premises. private cloud is more expensive than public cloud because it is managed by single organization. The data of private cloud is private and secure.

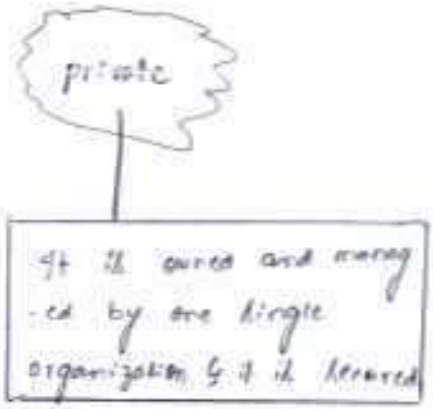

Fig:- private cloud

② public cloud:-

public cloud is the cloud where the multiple users use this cloud. So many users can store and access the data from the public cloud. It is used by Hardware (OS, memory, storage and by software (database, web apps) based on the subscriptions. It is used to share mails, transfer files and to access the different data which is stored in the cloud. We Need internet to access data from any cloud.

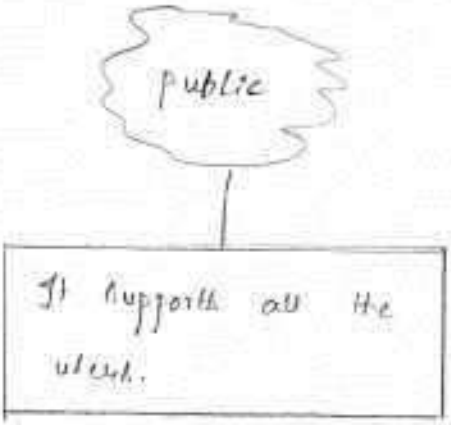

Fig:- public cloud.

③ Hybrid cloud:-

The Hibrid cloud is the cloud where the users can access the data from both interacted private and public cloud. The cloud which is both private and public cloud is Hybrid cloud. example, is the retailer wants to store or access the data in the cloud but is it a holiday he can store or access the data from the public easily. The cloud which is interconnected by both public and private is Hybrid cloud.

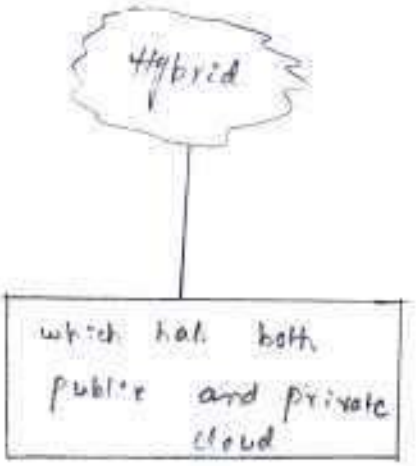

Fig:- Hybrid cloud.

④ Community cloud:-

This cloud supports multiple organizations. multiple organizations can store and access the data from the single cloud which is called as community cloud.

example:- if the police stations of different locations are storing data the data is stored in community cloud.

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINERING

B.TECH. IV YEAR I SEM., I Mid Term Examinations, SEPTEMBER – 2019

CLOUD COMPUTING Date: 16/09/2019(AN)

Objective Exam

Name: G. Raga Sudha Hall Ticket No. 16X31A0559

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 10.

I choose the correct alternative:

1. What are the key characteristics to be exhibited by Cloud Computing [D]
   A) Multitenancy B) Reliability C) Scalability D)All
2. SOA relies on of resources. [B]
   A) Physical Availability B) Virtualization C) Both a &b D) None
3. Web Services provided by the Cloud are [B]
   A) Iaas B) Paas C) SaaS D) All
4. The type of cloud computing that delivers applications through a browser to customers using a multiuser architecture [C]
   A) IaaS B) Paas C) SaaS D) MaaS
5. What is the biggest challenge of cloud computing? [C]
   A) Cost B) Bandwidth C) Security D) Performance
6. _____works by exposing Amazon's web –scale messaging infrastructure as a service [A]
   A) Amazon S3 B) Amazon Sample DB C) Amazon SQS D) Amazon EC2
7. Which is ranked first as the greatest challenge or issue of cloud computing? [A]
   A) Security B) Cost C) Availability D) Performance
8. Which service provides delivery of computer infrastructure as service [A]
   A) CaaS B) IaaS C) SaaS D) All
9. How many common methods are there to achieve identity federation? [D]
   A) 3 B) 4 C) 2 D)5
10. Which is ranked first as the greatest challenge or issue of cloud computing [A]
    A) Security B)Cost C)Availability D) Performance

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II Fill in the Blanks

11. Collaboration is the opiate of the masses in "cloud land".
12. IaaS stands for Infrastructure as a Service
13. Vector Processing is a kind of parallel processing for ~~System~~ concurrent processing.
14. Data propagation time increases in proportion to the number of processors added to SMP systems
15. multitenancy enables cost and resource sharing across the (often vast) user base.
16. Amazon S3 is a web service for content delivery.
17. The term cloud has been used historically as a metaphor for the Internet.
18. presence is a core component of an entity's real-time identity.
19. Simple is the ability for two XMPP servers in different domains to exchange XM stanzas.
20. Grid is an enabling technology for peer to peer interaction

Name: M. Bharathi Course: B.tech II Year/Branch: CSE-B

Subject: CRNS Lab Date: Examination: Lab Internal - 1

H.T. No. 17X31A0588 No. of Additionals 2

MARKS 10

Set II

1) Aim: To write a C program that Contains a string (char pointer) with a value "Hello world". The program should XOR each character in this string with 0 and displays the result

Source Code:

```
#include <stdio.h>
# include<Conio.h>
# include <stdlib.h>
# include <string.h>
void main()
{
char str[20], str1[11];
int i, len;
clrscr();
printf("Enter the string:");
gets(str);
len = strlen(str);
for(i=0; i<len; i++)
```

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```
}
str1[i] = str[i] ^ 0 ;
printf("%c", str[i]);
}
printf("\n");
getch();
}
```

Excepted Output:

Enter the string : Hello world

Hello world

Output :

Enter the string : Hello world

Hello world

2. Aim : To write a java program to perform encryption and decryption using Ceaser Cipher algorithm.

Source Code :

```
import java.io.*;
import java.util.*;
class Ceaser
{
```

```
static Scanner sc = new Scanner (System.in);
static BufferedReader br = new BufferedReader
                    (new InputStreamReader (System.in));
public static void main (String args[]) throws
                                    IOExcaption
{
System.out.println ("Enter the string:");
String str = br.readline();
System.out.println ("Enter the key:");
int key = sc.nextline();
String encrypted = encrypt (str, key);
System.out.println ("Encrypted text is :" + encrypted);
String decrypted = decrypt (encrypted, key);
System.out.println ("Decrypted text is :" + decrypted);
}
public static String encrypt (String str, int key)
{
String encrypted = " ";
```


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```
for (int i = 0; i< str.length(); i++)
{
int c = str.charAt(i);
if (Character.isUpperCase(c))
{
 c = c + (key % 26);
 if (c < 'z')
 c = c-26;
}
if (Character.isLowerCase(c))
{
 c = c + (key % 26);
 if (c < 'z')
 c = c-26;
}
encrypted + = (char)c;
}
return encrypted;
}
public static String decrypt (String str, int key)
{
String decrypted = " ";
for (i=0; i<str.length(); i++)
{
 int c = str.charAt(i);
```

```
if(Character.isUpperCase(c))
{
 c= c-(key%26);
 if (c<'A')
 c=c+26;
}
else if (Character.isLowerCase(c))
{
  c= c-(key%26);
  if(c<'a')
   c = c+26;
}
decrypted += (char) c;
}
return decrypted;
}
```

Expected Output :

```
Enter the string : hello
Enter the key : 2
Encrypted text is : jgnnq
Decrypted text is : hello
```


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Output :

Enter the string : hello

Enter the key : 3

Encrypted text is : khoor

Decrypted text is : hello

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For Examiners' Award only

Description	Marks
Design / Code	20
Execution	20
Output / Results	20
Viva - Exam	13
Total	73

Total Marks obtained	73
Maximum Marks	75

9/12/2020.

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Ch. Hari Vijaya. 9/12/2020.

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START WRITING FROM HERE

Set 4

1) Write a C program that Contains a string (char pointer) with a value 'Hello world' The program should AND or and XOR each character in this string with 127 and display the result

2) Write a C/Java program to implement the DES algorithm logic (or) Write a C/Java program to implement the Rijndael algorithm logic

1) Aim:

To write a C program that should AND, OR, XOR each character in 'Hello world'

Source Code:

```
#include<stdio.h>
#include<conio.h>
#include<stdlib.h>
void main()
{
int i, len;
char str1[10];
char str[11];
```

Expected output :

1) Enter the string : Hello world
Hello world
Hello world
Hello world

Acheal output :

2) Enter the string : Hello world
Hello world
Hello world
Hello world

1) 2) Aim : To write a C program to implem the DES algorithm logic.

Source code :

```
#include <stdio.h>
#include <conio.h>
#include <string.h>
#include <stdlib.h>
void main()
{
 int ch, i, lp;
 char cipher[50], plain[50], key[50];
```

```
clrscr();
printf ("enter the string");
gets (str);
len = strlen (str);
for (i=0; i<len; i++)
{
  str1[i] = str[i] ^ (127 % i);
  printf("%c", str1[i]);
}
printf("\n");
for (i=0; i<len; i++)
{
  str1[i] = str[i] & (127);
  printf ("%c", str1[i]);
}
printf ("\n");
for (i=0; i<len; i++)
{
  str1[i] = str[i] | (127 % i);
  printf ("%c", str1[i]);
}
printf("\n");
getch();
}
```

Enter your choice : 2

Data decryption

decrypted text is : hello

Enter your choice : 3

Original output:

------- MENU -------

1. Data encryption
2. Data decryption
3. exit

Enter your choice : 1

Data encryption

Enter plain text : hello

Enter the encryption key : 3

Decrypted text is : khoor

Enter your choice : 2

Data decryption

decrypted text is : hello

Enter your choice : 3

Name : K. Mounika

Roll No : 18X35A0502

Subject : Principles of programming language assignment-01

Year : IV CSE-C

1 Discuss the additional features of an attribute grammars ?

Ans An Attribute grammar is a device used to describe more of the structure of a programming language that can be described with a context-free grammar. An attribute grammar is an Extension to a context free grammar. The Extension allows certain language rules to be conveniently described such as type compatibility.

a) Static Semantics :-

A Syntax rule that is difficult to Specify with BNF, consider type compatibility rules. In Java, for Example, a floating point value cannot be assigned to an Integer type variable, although the opposite is legal.

The Static Semantics of a language is only indirectly related to the meaning of programs during Execution.

b) Basic Concepts :-

Attribute Grammar are Context-free grammar to which have been added attributes, attribute

Computation functions, and predicate functions. Attributes which are associated with grammar symbols are similar to variables in the sense that they can have values assigned to them.

Attribute computation functions, sometimes called semantic functions, are associated with grammar rules.

Predicate functions, which state the static semantic rules of the language, are associated with grammar rules.

c) Attribute Grammar defined :-

An Attribute grammar is a grammar which are following additional features :

i) Associated with each grammar symbol 'x' is a set of attributes A(x). The set A(x) consist of two disjoint sets S(x) and I(x) called synthesized and Inherited attributes.

ii) Associated with each grammar rule is a set of semantic functions and a possibly empty set of predicate functions over the attributes of the symbols in the grammar rule.

For a rule $X_0 \rightarrow X_1 \text{---} X_n$, the Synthesized attributes of X_0 are computed with Semantic functions of the form $S(X_0) = f(A(X_1), \ldots A(X_n))$

Inherited attribute of Symbols $X_j, 1 \leq j \leq n$, are Computed with a Semantic functions of the form $I(X_j) = f(A(X_0), \ldots A(X_n))$.

iii) A predicate function has the form of a Boolean Expression on the union of the attribute set $\{A(X_0), \ldots A(X_n)\}$ and a set of literal attribute values.

d) Examples of Attribute Grammars :-

Attribute Grammars can be used to describe Static Semantic, Consider the following fragment of an attribute Grammar that describes the rule that the name on the End of an Ada procedure must match the procedures name.

Syntax :-

<assign> → <var> = <Expr>

<Expr> → <var> + <var>

| <var>

<var> → A | B | C

The attributes for the non-terminals in the Example attribute grammar are described in the following paragraph.

i) Actual_type :- A Synthesized attribute associated with the non terminals <var> and <Expr>. It is used to Stored the actual type, int or real, of a Variable (or) Expressions.

ii) Expected_type :- An inherited attribute associated with the non_terminal <Expr>. It is used to store the type, Either int or real, that is Expected for the Expression.

Example :- An Attribute Grammar for Simple Assignment Statements.

1. Syntax rule :- <assign> → <Var> = <Expr>
   Semantic rule :- <Expr>.Expected_type ← <var>.actual type

2. Syntax rule :- <Expr> → <var>[2] + var[3]
   Semantic rule :- <Expr>.actual_type ← If (<var>[2].actual_type = int) and (<var>[3].actual type = int)
   then int
   Else real
   End if
   Predicate rule : <Expr>.actual type == <Expr>.Expected_type

3. Syntax rule : <Var> → A | B | C
   Semantic rule : <var>.actual_type ← look up(<var>.String>

The lookup function looks a given variable name in the Symbol table and returns the Variable type.

2. What are the significant characteristics of programming language ?

Ans Language Evaluation Criteria.

Characteristic	Readability	Writability	Readability
i) Simplicity	•	•	•
ii) Orthogonality	•	•	•
iii) Data types	•	•	•
iv) Syntax design	•	•	•
v) Support for abstraction		•	•
vi) Expressivity		•	•
vii) Type checking			•
viii) Exception Handling			•
ix) Restricted aliasing			•

i) Readability :- One of the most important Criteria for judging a programming language is the ease with which programs can be read and understand. Before 1970, Software development was largely though of in terms of writing code. In the 1970s, however the Software life-cycle concept was developed, coding

was relegated to a much smaller role, maintainance was recognized as a major part of the cycle, particularly in terms of cost.

a) Overall Simplicity :- The overall simplicity of a programming language strongly affects its readability. A language with a large number of basic constructs is more difficult to learn than one with a smaller number.

Example :- Count = Count + 1
Count += 1
Count ++
++ count

b) Orthogonality :- Orthogonality in a programming language means that a relatively small set of primitive constructs can be combined in a relatively small number of ways to build the control and data structures of the language. for Example a language has four primitive data types (integer, float, double and character) and two type operators (array and pointer).

ii) Writability :- Writability is a measure of how easily a language can be used to create programs for a chosen programs problems domain. Most of the language characteristics that effect readability also effect writability.

the following subsections describe the most important characteristics influencing the writability of a language.

desirable.

b) Exception Handling :- The ability of a program to intercept runtime Errors, (as well as other unusual conditions detectable by the program), take corrective measures, and then continue is an obvious aid to reliability. This language facility is called Exception handling.

c) Aliasing :- Aliasing is having two or more distinct names that can be used to access the same memory cell. most programming languages allow some kind of aliasing. for Example, two pointers set to point to the same variable. which is possible in most languages. In such a program, the programmer must always remember that changing the value pointed to by one of the two changes the value referenced by the other.

d) Readability and writability :- Both readability and writability influence reliability. A program written in a language that does not support natural ways to express the required algorithms will necessarily use unnatural approaches. unnatural approaches are less likely to be correct for all possible situations.

Readability affects reliability in both the writing and maintenance phases of the life cycle. programs that are difficult to read are difficult both to write and to modify.

a) Simplicity and Orthogonality :-

If a language has a large number of different constructs, some programmers might not be familiar with all of them. A smaller number of primitive constructs and consistent set of rules for combining them (i.e., Orthogonality) is much better than simply having a large number of primitives.

b) Support for Abstraction :-

Abstraction means the ability to define and then use complicated structures or operations in ways that allow many of the details to be ignored. Abstraction is a key concept in contemporary programming language design. This is a reflection of the central role that abstraction plays in modern program design methodologies. programming languages support two distinct, categories of abstraction, process and data.

iii) Reliability :- A program is said to be reliable if it performs to its specifications under all conditions.

a) Type checking :- Type checking is simply testing for type Errors, in a given program, Either by the Compiler or during program Execution. Type checking is an important factor in language reliability. Because run-time type checking is Expensive, Compile time type checking is more

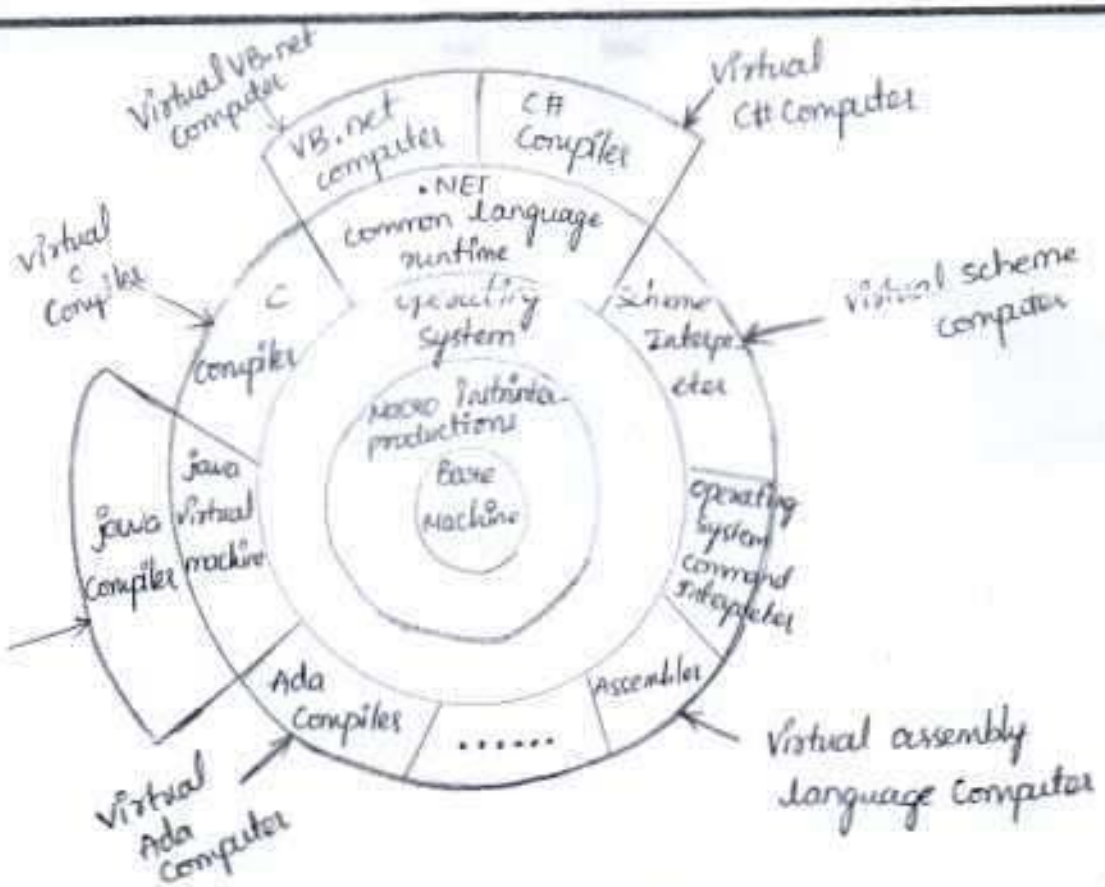

Fig:- Layered Interface of Virtual Computers, provided by a typical Computer system.

The language that a Compiler translates is called the "Source language". The process of Compilation and program Execution take place in several phases. The most important of which are shown in figure 3.

The lexical Analyzer gathers the characters of the Source program into lexical units. The lexical units of a program are identifiers, special words, operators and punctuation symbols.

3. Explain the three methods of Implementing a programming language ?

Ans: Implementation Methods :-

The Internal memory is used to store programs and data. The processor is a collection of circuits that provides a realization of a set of primitive operations, or machine instruction, such as those for arithmetic and logic operations In most computers, some of these instructions which are sometimes called macro instructions, called are actually implemented with a set of instructions called micro instructions which are defined at an even lower level.

The machine language of the computer is its set of instructions. In the absence of other language supporting software its own machine language is the only language that most hardware computers "understand".

i) Compilation :- programming languages can be implemented by any of three general methods. programs can be translated into machine language, which can be executed directly on the computer. This method is called a "compiler implementation" and has the advantage of very fast program execution, once the translation process is complete. Most production implementations of language such as C, COBOL, C++ and Ada are by compilers.

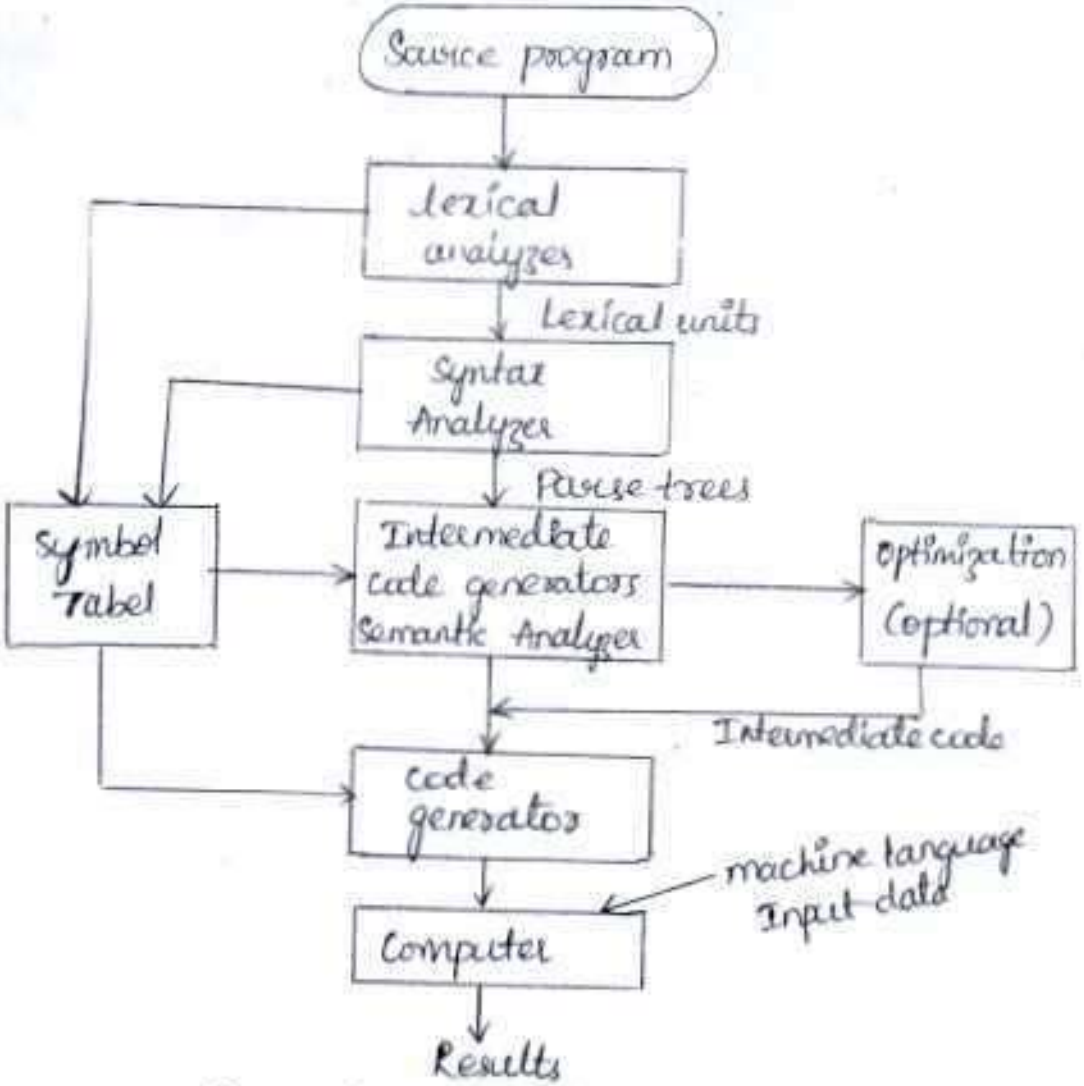

Fig :- The Compilation process

The Syntax Analyzer takes the lexical units from the lexical analyzer and uses them to construct hierarchical structures called parse trees. These parse trees represent the syntactic structure of the program.

The Intermediate code generator produces a program in a different language, at an intermediate level between the source program and the final output of the compiler; the machine language program; Intermediate languages.

The Semantic analyzer is an integral part of the Intermediate code generator. The semantic analyzer checks for

Errors, such as type Errors, that are difficult, if not impossible, to detect during syntax analysis.

Optimization, which improves programs by making them smaller or faster or both is often an optional part of compilation.

The code generator translates the optimized intermediate code version the program into an Equivalent machine language program.

The symbol table serves as a database for the compilation process.

ii) Pure Interpretation :- pure interpretation lies at the opposite end of implementation methods. with this approach, programs are interpreted by another program called an Interpreter, with no translation whatever.

pure interpretation has the advantage of allowing Easy implementation of many source_level debugging operations, because all run-time Error messages can refer to source_level units.

Disadvantage of pure interpretation is that it often requires more space.

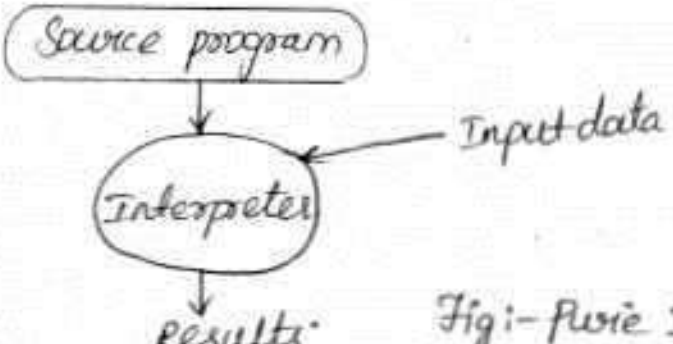

Fig:- Pure Interpretation

(iii) Hybrid Implementation Systems :

Some language implementation systems are compromise between compilers and pure interpreters ; they translate high level language programs to an intermediate language designed to allow easy interpretation. This method is faster than pure interpretation because the source language statements are decoded only once. Such implementation are called "Hybrid implementation systems".

Translating intermediate language code to machine code, it simply interprets the intermediate code.

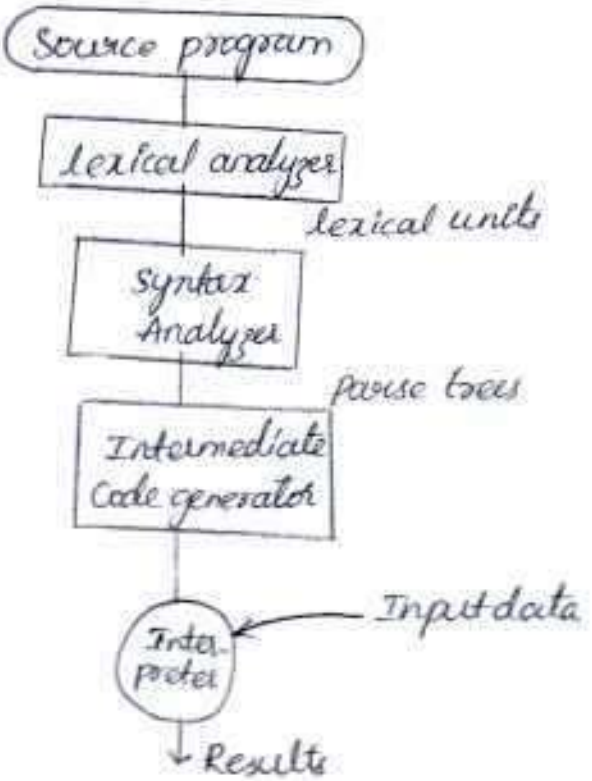

Fig:- Hybrid Implementation System

Perl implemented with a hybrid system. perl programs are partialy compiled to detect Errors before interpretation and to simplify the interpreter.

92

4. What is a variable and what are the attributes of variable ? Elaborate on address of a variable.

Ans Variables :- A program variable is an abstraction of a computer cell or collection of cells. programmers often think of variable names as names for memory locations, but there is much more to a variable than just a name.

A variable can be characterized as a sextuple of attributes (name, address, value, type, lifetime and scope).

i) Name :- Variable names are the most common names in programs. most variables have names.

ii) Address :- The address of a variable is the machine memory address with which it is associated. In many languages, it is possible for the same variable to be associated with different addresses at different times in the program.

The address of a variable sometimes called its l-value, because the address is what is required when the name of a variable appears in the left side of an assignment.

iii) Type :- The type of a variable determines the range of values the variable can store and the set of operations that are defined for values of the type. for example, the int type in Java specifies a value range of -2147483648 to 2147483647 and arithmetic operations that for addition, subtraction, multiplication, division and modulus.

iv) Value :- The value of a variable is the contents of the memory cell or cells associated with the variable. It is convenient to think of computer memory in terms of abstract cells, rather than physical cells. The physical cells, or individually addressable units, of most contemporary computer memories are byte-size, with a byte usually being eight bits in length. This size is too small for most program variables.

v) Life time :- The Lifetime of a variable is the time during which the variable is bound to a specific memory location. So the lifetime of a variable begins when it is bound to a specific cell and ends when it is unbound from that cell. To investigate scalar var storage bindings of variables, it is convenient to separate scalar variables into four categories, according to their lifetimes.

These categories are named static, stack-dynamic, Explicit heap-dynamic and Implicit heap-dynamic.

vi) Scope :- The scope of a variable is the range of statements in which that is visible. A variable is visible in a statement if it can be referenced in that statement.

Scope rules determine how references to variables declared outside the currently executing subprogram or block are associated with their declarations & thus their attributes.

A variable is local in a program unit or block if it is declared there. The non local variable of program unit or block.

5. Describe the three-Semantic models of parameter passing?

Ans Semantic models of parameter passing :-

Formal parameters are characterized by one of three distinct semantic models:

1) They can receive data from the corresponding actual parameter.
2) They can transmit data to the actual parameter.
3) They can do both. these models are called in mode, out mode, inout mode respectively.

There are two conceptual models of how data transfers take place in parameter transmission: Either an actual value is copied (to the caller, to the called, or both ways).

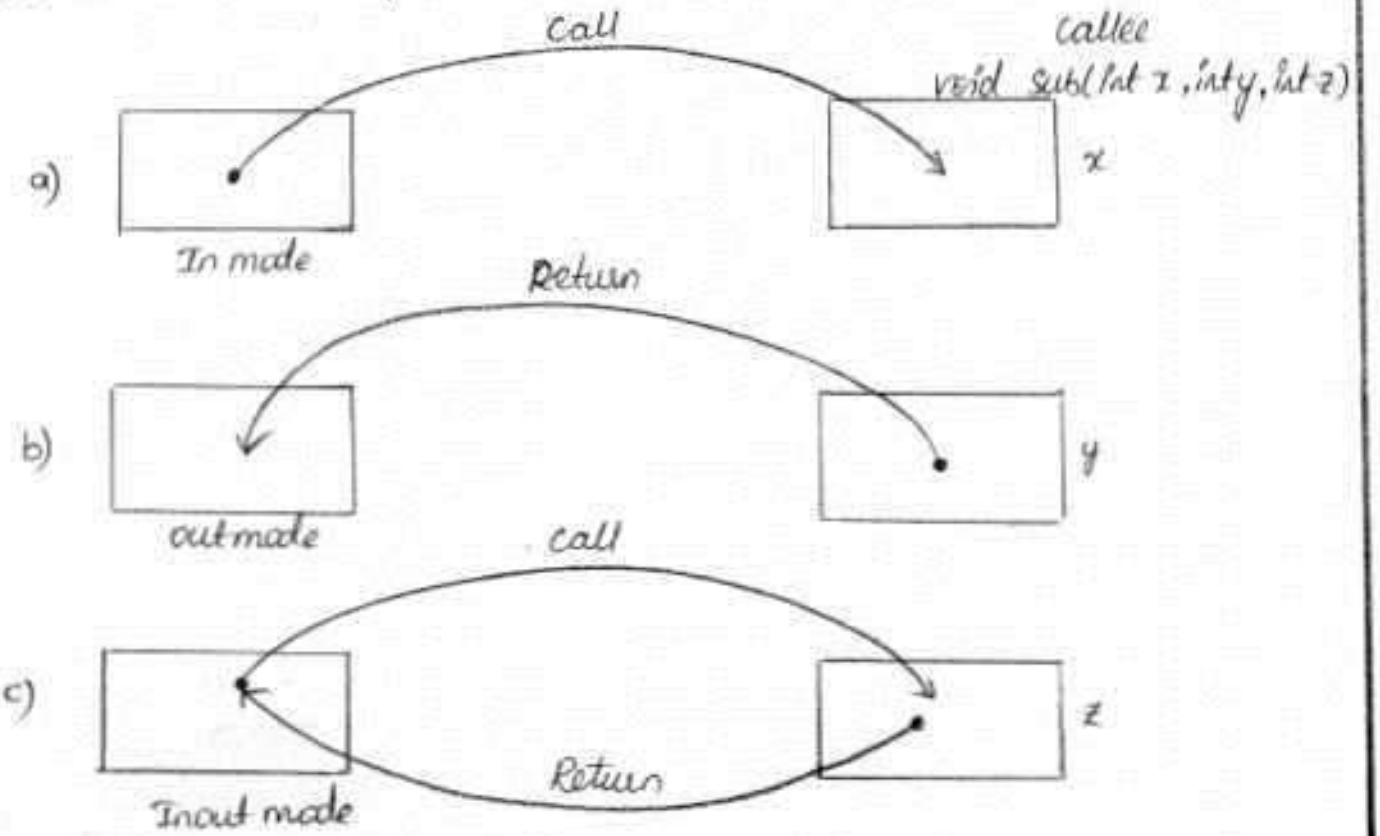

Figure: The three semantics models of parameter passing when physical moves are used.

Implementation models of parameter passing :-

1) pass-by-value :- passed by value, the value of the actual parameter is used to initialize the corresponding formal parameter, which then acts as a local variable in the sub program, thus implementing in-mode semantics.

pass-by-value is normally implemented by copy, because accessing often are more efficient with this approach. It could be implemented by transmitting an access path to the value of the actual parameter in the caller, but that would require that the value be in a write protected cell.

2) Pass-by-Result :- pass-by-Result is an implementation model for out-mode parameters, when a parameter is passed by result, no value is transmitted to the sub program. the corresponding formal parameter acts as a local variable, but just before control is transferred back to the caller, its value is transmitted back to the caller's actual parameter, which obviously must be a variable.

3) pass-by-value-Result :- pass-by-value Result is an implementation model for inout-mode parameters in which actual values are copied. It is in effect a combination of pass-by-value and pass-by-result.

pass-by-value-result is sometimes called pass-by-copy, because the actual parameter is copied to the formal parameter at subprogram entry and then copied

back at Subprogram termination.

4) Pass-by-Reference :- pass-by-Reference is a Second implementation model for Inout-mode parameters. Rather than copying data values back and forth, however, as in pass-by-value-result, the pass-by-reference method transmits an access path, usually just an address, to the called subprogram. This provides the access path to the cell storing the actual parameter. Thus the called subprogram is allowed to access the actual parameter in the calling program unit.

5) pass-by-Name :- pass-by-name is an Inout-mode parameter transmission method that does not correspond to a single Implementation model. When parameter are passed by name, the actual parameter is, in effect, textually substituted for the formal parameters in all its occurences in the subprogram.

Implementing parameter-passing methods :-

pass-by-value parameters have their values copied into stack locations. The stack locations then serve as storage for the corresponding formal parameters.

pass-by-result parameter are implemented as the opposite of pass-by-value. The values assigned to the pass-by-result actual parameters are placed in the stack,

where they can be retrieved by the calling program unit upon termination of the called Subprogram.

pass-by-value result parameters can be implemented directly from their Semantics as a combinations of pass-by-value and pass-by-result.

pass-by-reference parameters are perhaps the simplest to implement. Regardless of the type of the actual parameter, only its address must be placed in the Stack.

```
clrscr();
while(1)
{
printf("  --------- MENU ---------");
printf("\n1. Data encryption  3. exit
        2. Data decryption, \n");
printf(" Enter your choice");
scanf("%d", &ch);
switch(ch)
{
case 1: printf(" Data encryption \n");
        printf(" \n Enter the plain text: \n");
        fflush(stdin);
        gets(plain);
        printf("\n enter the encryption key :\n");
        scanf("%d", &kp);
        for(i=0; plain[i] != '\0'; i++)
          cipher[i] = plain[i] + kp;
        cipher[i] = '\0';
        printf(" Encryptedtext : \n");
        puts(cipher);
        break;
```

```
Case 2: printf ("Data decryption : \n");
        for (i=0; cipher[i] != '\0'; i++)
            plain[i] = cipher[i] - kp;
        printf("decrypted text is :\n");
        puts (plain);
        break;
Case 3: exit(0);
        break;
}
}
getch();
}
```

Expected output :

```
-------- MENU ------
1. Data encryption
2. Data decryption
3. exit
Enter your choice : 1
Data encryption
Enter plain text: hello
Enter the encryption key : 2
Decrypted text is : jgnnq
```

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Rollno : 18X35A0502

year : IV CSE-C

Subject : Principles of Programming language

Assignment - 02

1. Write short notes on

a) Parameters b) Procedures c) Pass by references

d) Type checking.

a) Parameters :-

Sub programs typically describe computations. There are two ways that a non method subprogram can gain access to the data that it is to process through direct access to non local variables or through parameters passing.

The parameters in the subprogram header are called formal parameters. They are sometimes thought of as dummy variables because they are bound to storage only when the subprogram is called and that binding is often through some other program variables.

b) Procedures :-

There are two distinct categories of subprogram procedures and functions - both of which can be viewed as approaches to extending the language. All subprograms are collections of statements that define parameterized computations. functions return values and procedures donot. In most languages that donot include procedures as a seperate form of subprogram function can be defined not to return values and they can be used as procedures.

c) Pass by reference :-

Pass by reference is a second implementation modes for inout-mode parameters. Rather than copying data values back and forth, however as in pass-by-value_result, the pass-by-reference method transmits an access path, usually just an address, to the called subprogram. This provides the access path to the cell storing the actual parameter. Thus the called subprogram is allowed to access the actual parameter in the calling program unit.

d) Type checking :-

Type checking is the process of verifying that each operation executed in a program aspects the system of the language. This generally means that all operands in any expression are of appropriate types and numbers.

---

2. Discuss how producer problem and defining philosophers Problem are solved using concurrency in Ada.

A: Task which is a form of a module is the basic Concurrency unit in Ada. A task contains two parts namely specification and a body.

The General form of Task in Ada.

```
task type p is
        Entry declarations
```

```
End P;
task body p is
    declaration part
begin
  Sequence of Statements
.
End P.;
```

Producer - Consumer problem :

Producer - Consumer task has two actions Entries namely "Give" and "Take" local data and the actions to be taken for these two Entries are defined in the body part. The body is a single - loop and contains two Entries are defined in the body part. The body is a single - loop and contains two alternatives denoted by the SELECT Statement.

Dining philosophers problem :

Dining philosopher problem consists of five philosophers Each philosopher has only two things to do i.e., Thinking and Eating.

A philosopher Enters into the dining room whenever he feels hungry. The Eating arrangement is simple Consisting of a round table on which a large serving bowl of Spaghetti five plates, one for each philosopher and five forks are placed. A philosopher wishing to Eat would go to his or her assigned place at the table and using the two forks one either side of his plate.

3. Define monitor. Explain how cooperation synchronization and competition synchronization are implemented using monitors.

A: Monitor :-

A Monitor is a program unit that consists of all the synchronization operations that can be performed on the shared data i.e., it encapsulates all the shared data structures along with their operations these by hiding their representation.

A monitor is an entity that can be added to any programming language particularly to those languages, that have a programming concept like 'module' or an 'abstract data type'. 'concurrent pascal' was the first programming language that includes the mirror.

1. Variable :

Any kind of data-variables can be Embedded in monitors.

2. Condition variable :

A special kind of variable called the 'condition variable' is also included in monitor, whose purpose is to do signaling inside the monitors.

3. Procedures :

The monitor incorporates certain procedures which are called from outside the monitor.

The general form of representing monitors in concurrent pascal is given below.

Competition Synchronization :-

Monitors possess a property in which the data shared between the processes resides in the monitor but not in any other units. As a shared data is stored inside the monitor, the monitor itself is responsible for providing synchronized access.

Cooperation Synchronization :

i. The Delay operation :

The 'Delay' operation takes one parameter which is a variable of type queue. Its function is to keep the process that calls it in the queue and give up its access rights to the data structures in the monitor.

ii- The Continue operation :

The 'Continue' operation also take a one parameter of type queue. Its function is to detach the process that calls it from the monitor so that, other processes can access the monitor.

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4. Explain the basic primitives of LISP. Give suitable Examples.

1. primitive Data types :

Atoms and lists are two primitives data types available in LISP. whereas function definitions and property lists belongs to the special type of lists.

Atoms :

An 'atom' in LISP refers to the most fundamental or the most basic data type.

i) A literal atom that represents symbols.

ii) A numeric atom which represents numbers.

Lists :- Another data type provided by LISP is a 'List' which is widely used in list processing.

A list usually contains Elements which are Enclosed in and in parenthesis.

Two types of list are,

i) Simple list

ii) Nested list

Numeric Atoms of Numbers :

An Integers, floating-point format of the hardware representation are used for the numbers in LISP In its hardware representation, a run time descriptor is also needed. Hence a numeric atom is one that can have a special type designator along with a pointer to the bit string representing the number rather than a pointer for a property list.

Strings :

In LISP, strings are expressed as String of symbols.

2. Structured Data Types :

Some vector of an array data object is provided by most of the LISP implementations.

i) MIvect :- A data object of type vector is created by this function whose subscript ranges from '0' to a given 'bound'

ii) getv (vector, subscript) :

A pointer stored at a specified subscript in the argument vector is returned by this functions.

iii) Putv :

It is used to assign a new value to a particular vector

Component.

Here, each atom occured in a function is looked up in the ob_list and a pointer to that atom is returned if it exists already else a new atom is created.

5. Write a detail note on Functions in ML ?

A: Many Scripting languages are Embedded with set of libraries that are used for Supporting certain functions. python is one such Scripting language that consists of module library. In contrast to other Scripting languages, python is neither capable of performing built-in high level String processing no supporting Gui operations. Therefore, to overcome these incapabilities module library is Embedded with in the language. due to which the language perforns the following functions

i) String handling Service

ii) Cryptography multimedia Services.

iii) GUI's and operating System Services

iv) Internet Services

v) Compilation. for Example the 're' module library Support powerful String matching Services using regular Expression.

2. Discuss how producer consumer problem and dining philosophers problem are solved using Concurrency in Ada.

A:- Task which is a form of a module is the basic Concurrency unit in Ada. A task Contains two parts namely specification and a body. The General form of task in Ada task type x entry declaration end x; task body x is declaration part begin sequence of statements end x;

.
.
.

A, B : x; where A & B are the tasks

Let us consider producer-consumer problem & dining philosopher's problem using concurrency.

Producer consumer problem :— producer consumer problem is a simple form of cooperation synchronization. This problem came into Existence in the development of os.

i. The sequence of stores to and removals from the buffer must be synchronized.

ii. If the buffer is Empty, the consumer unit must not be allowed to place new data in the buffer, in the same way if the buffer is full, the producer unit should not be allowed to place new data in the buffer.

iii. The producer consumer task has two Entries namely give and take. Local data and the actions to be taken for these two Entries are defined in the body part.

...

iv. The body is a Single_loop and contains two alternatives denoted by the Select; Statement. Guard is responsible for protecting each Entry and the Entry, give is accepted till

Count < boundary and the Entry take is accepted till Count > 0. An Input character A is allocated to pool, where the Entry give is accepted & a character is allocated from pool to B, when the Entry take is accepted. The updation of pointers pin and count are done.

Task producerconsumer is,

```
Entry give (A : In character);
Entry take (B : out character);
End;
task body producerconsumer is
boundary : constant integer := 100;
pool : array(1 .... boundary) of character,
pin : integer := 1;
pool : Integer := 0;
count : Integer := 0; begin
loop
select
when count < boundary ⇒
accept give ( A: In character) do
 → pout := pout mod count +1;
 → pool(pout) := A;
End give;
 count:= count - 1;
```

```
or when count > 0 =>
Accept take (B : out character) do
B := pool (pin);
End take;
Pin := pin mod boundary + 1;
Count := Count - 1;
or terminate;
End select;
End loop;
End producer consumer;
```

Dining philosophers problem :—

Five silent philosophers sit at a table around a bowl of spaghetti. The fork is placed between each pair of adjacent philosophers.

Each philosopher must alternately think & eat. Eating is not limited by the amount of spaghetti left. assume an infinite supply. However a philosopher can only eat while holding both the fork to the left and the fork to the right.

Each philosopher can pick up an adjacent fork, when available, and put it down, when holding it. These are separate actions : forks must be picked up & put down one by one.

The problem is how to design a discipline of behavior such that each philosopher won't starve i.e., can forever continue to alternate between eating & thinking.

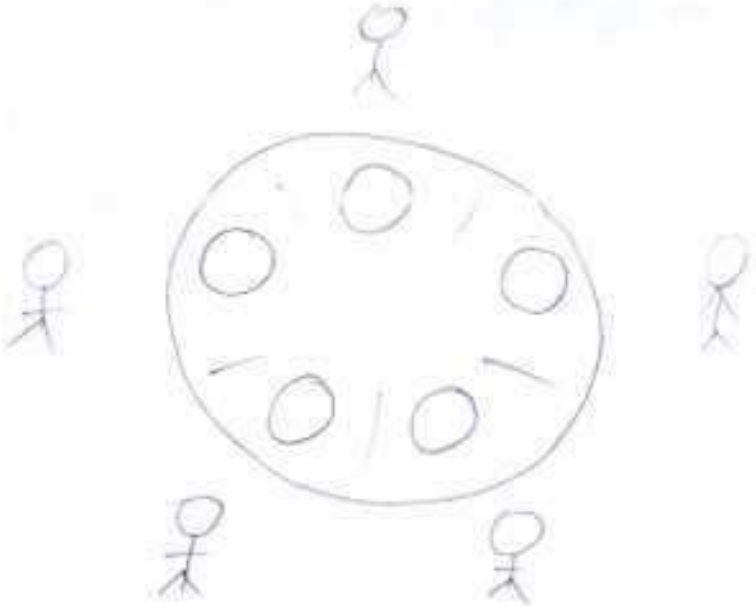

Fig:- Dining philosophers table

Solution to Dining philosophers problem :-

```
Procedure main is
-- declaration of tasks,
 forks, philosophers and
 room--
 fork ; array(0--4) of forks ;
 philosopher ; array (0---4) of forks ;
  begin
  -- Tasks such as
   fork (0--4) philosopher(0--4) and room automatically
                gets started here---
      for i in 0-- 4 loop
      philosopher(i), time (1 : Integer);
      End loop;
      -- main program terminates upon the termination of
                 all tasks---
        End ;
      task body forks is
```

```
begin
loop
accept putdown;
End loop;
End forks;
task body philosophers is,
 Entry Hime(to : in Integer);
  End;
  task body philosophes is
1 : Integer;
    begin
    accept Life(11 : in Integes) do 1 := 4;
    End;
    loop
    delay think(1);
    room.Enter;
    fork(1).pick up;
    fork(1+1) mod 5) pick up;
    delay Eattime(1);
    for(1).putdown;
     fork(1+1) mod 5) put down;
     room.Exit;
     End loop;
     End philosopher;
      task room is
      Entry Enter;
      Entry exit;
      End;
      task body room is
```

```
Occupancy : Integer := 0;
begin
loop
select
when occupancy < 4 =>
Accept Enter do
Occupancy :- occupancy + 1;
End;
or
Accept Exit do
occupancy := occupancy - 1;
End;
End select;
End loop;
End;
End room;
```