PMOS BIASED SENSE AMPLIFER DESIGN WITH LOW POWER AND HIGH PERFORMANCE

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Abstract:

Sense amplifiers plays a significant role in terms of its recital, functionality and reliability of the memory circuits. In this paper two new circuits have been proposed. The proposed circuit is PMOS biased sense amplifier,which provides very high output impedance and has reduced sense delay and power dissipation. As such, the proposed circuit performs the identical operations as that of conventional circuits but with the reduced the sense delay and power consumption

The growing gap between the processor and embedded memory speed is a major setback in the overall performance of electronic systems. Since the sense amplifier (SA) forms an integral part of the read circuitry in both volatile memories, such as SRAM, and non-volatile memories (NVMs), such as FLASH, its performance has a significant effect on the overall performance of memory. Access time, offset, power and area are the four important performance metrics of SA. The memory access time and input-offset of SA greatly affect the speed of the entire memory and therefore to patch up the gap between processor and memory speed, the SA is required to be fast and efficient.As one SA is employed for each bit line in the memory array, it is required to be compact in size and should have low power consumption. Furthermore scaling in technology makes it difficult to control the fabrication process leading to variation in process parameters causing unpredictability in the performance of SAs. Therefore, it is very important to keep this aspect in mind while designing and estimating the performance metrics of the SA

This thesis includes the study of various conventional SA designs in detail so as to have a better understanding of a basic SA and its operation and thus helping in understanding whatproblems are faced by designers in implementingthe SA designs and how these problems can be tackled. In addition to the conventional SA analysis, new sense amplifier designs have been proposed for both current sensing in FLASH memory and voltage sensing in SRAM. Keepingthe variation in process parameters due to scaling in mind, these proposed designs have been optimized in terms of access time, offset, power and area.

Keywords: Sense Amplifier, High Performance, PMOS Biased

1. INTRODUCTION

In any digital logic design memories are the most important blocks in DSP, microprocessors, microcontrollers, and computers. Audio players, digital cameras stores the data in the form of images, audio, video, speech in a flash memory should have less power with the display of memory capacity performance on high side on a single chip. Low sensing delay and increased higher capacities are required for improved quality of stored data. In order to accomplish the towering rate of staging, sense amplifiers are customarily applied to amplify the very small voltage difference on the bit lines at congruous sense timings . If the sense amplifiers enable signal is asserted early, the SA cannot amplify the minuscule voltage difference accurately. The overhead of access time and power consumption is incremented if the SAE is asserted tardy. Consequently, the optimum timing for SAE is critical for a high- speed and low-power SRAM. The memory cell need to have a mechanism in order to store data permanently and alter its contents electrically in a non-destructive way. The solution is to alter the threshold voltage of the all so that different threshold values may represent different states of the memory. The two basic

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states of a flash memory cell are called erased and programmed states. An erased cell is signified by a low threshold value whereas a high threshold value signifies a programmed cell. Equation 1.1 expresses the relation between the threshold voltage of MOS with the charge stored on the floating gate.

Where K denotes a constant which depends on gate and substrate material, channel doping and oxide thickness. C_{ox} denotes the gate oxide thickness and Q is the charge trapped into the oxide layer. From the equation it is clear that the parameter which can be kept in control to alter threshold of the device is Q which denotes the charge trapped in the oxide layer. There are charge injection techniques available to move charges in and out of the oxide. A normal MOS device cannot be used to retain the charges into its oxide thus the device has been modified. A floating gate (FG) device is used for this purpose. FG transistors have the capability to retain charge in their floating gate for an extended period even after the power supply is turned off.

During the Write/Program operation, the control gate and drain are biased at high voltage of 12V for the gate and 5 V for the drain (the voltages used for biasing are used as convention and may vary for different manufacturers), but the source is kept grounded. Under these circumstances, a very strong electric field develops which lets the electrons pass from the channel to the floating gate. These electrons overcome the potential barrier posed by the oxide layer and this mechanism is called Hot Electrons Injection .

Due to the presence of a high voltage on the drain node, the electrons flowing from the source to the drain gain energy due to the orthogonal electric field. Due to the presence of high electric fields, electron energy starts to increase and thus electrons are heated, some electrons gain energy high enough to overcome the barrier between the oxide layer and the silicon conduction band. These hot electrons need to overcome the barrier in the right direction so as to be collected inside the floating gate. The electrons trapped inside the floating gate causing the V_{TH} of the flash memory cell to rise. Thus, when a Read operation occurs, the cell appears to be in the switched off state or is logic programmed '0', since it is unable to conduct current due to its high V_{TH}. Thus writing data in a memory cell brings the cell from an erased state, which is typically called a logic state '1', to a logic state '0' or programmed state. The time required for this process is typically in the range of microseconds.

DMA test mode is used for the purpose of connecting the cell terminals directly to the external Input/output pads. This helps in characterization of the memory, the matrix and the reference cells in particular. It is a difficult task to filter the interference of the memory array. Many incorrect outputs can be obtained to the faults in circuitry if any. For example, if the voltages are applied in the wrong way or if there is a presence of any voltage spikes or glitches. The possibility of analyzing each and every cell is therefore a valuable opportunity. Even a single cell can be analyzed with the help of DMA thus proving to be a major test mode. The DMA test mode setup is shown in Fig. 7. It can be observed from Fig. 7. that in DMA the sense amplifier and the output latch are bypassed such that the drain node of the cell is directly connected to the external I/O pad which is further connected to the external supply. The supply voltage of this external supply is equal to that on the drain in case of a read operation. Also, the gate voltage supplied to selected cells in DMA mode is supplied through an external pin. This setup enables the manufacturer to measure cell current, transconductance and V_{TH} of cells under varying condition.

Operating in DMA mode so as to measure the cell current at different bias voltages is a tedious job. Therefore to increase the speed of this procedure, Fast DMA or FDMA was introduced. FDMA mode is similar to the read mode but in FDMA mode a constant reference current is maintained and the cell current is compared with it with the help of a sense amplifier. The reference current could be generated internally or could be generated externally with the help of the DMA pin.

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The gate voltage could be controlled by an external I/O pad similar to DMA mode. By varying this current and gate voltage the cell characteristics are plot. FDMA has an advantage over DMA being faster due to the read operation.

i.LITERATURE SURVEY

It is organized into five sections. discusses about few conventional SA designs and includes their detailed study. Firstly introduces a high speed low offset cross coupled latch type current sense amplifier for NVM applications and the Flash memory in particular. The design and its working has been explainedin detail, the design has been simulated an analyzed by incorporating VTH variations and the outputs have been presented. Section 4 discusses about the low offset high speed cross coupled latch type SA for SRAM applications, in which offset and sensing delay lowing have been achieved using body biasing techniques. Inthis section, the design has been explained in detail, it has been simulated and analyzed by incorporating MC VTH variations of 10mV in all the devices. The outputs for

this sense amplifier design for SRAM have been presented.

ii.EXISTING SYSTEM

Comparison of different current mode sense amplifiers is presented. In those circuits, we considered PMOS biased sense amplifier circuits as a references circuit for proposed method by, making some modificationsin it. In this circuit, there exists two differential amplifier circuits with current mirrors which it has to be modified in the proposed circuit

iii.PROPOSED SYSTEM

A fast access time and low power dissipation are achieved with newly developed circuits of sense amplifier for low voltage supply. In the proposed circuit Here minimizing the mirror transistor so we can have low power dissipation with high performance and less sense delay.

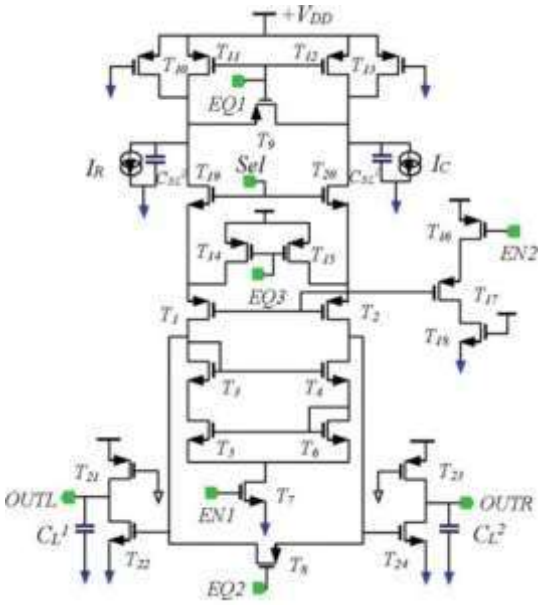

Fig.1 Existing Sense Amplifier circuit

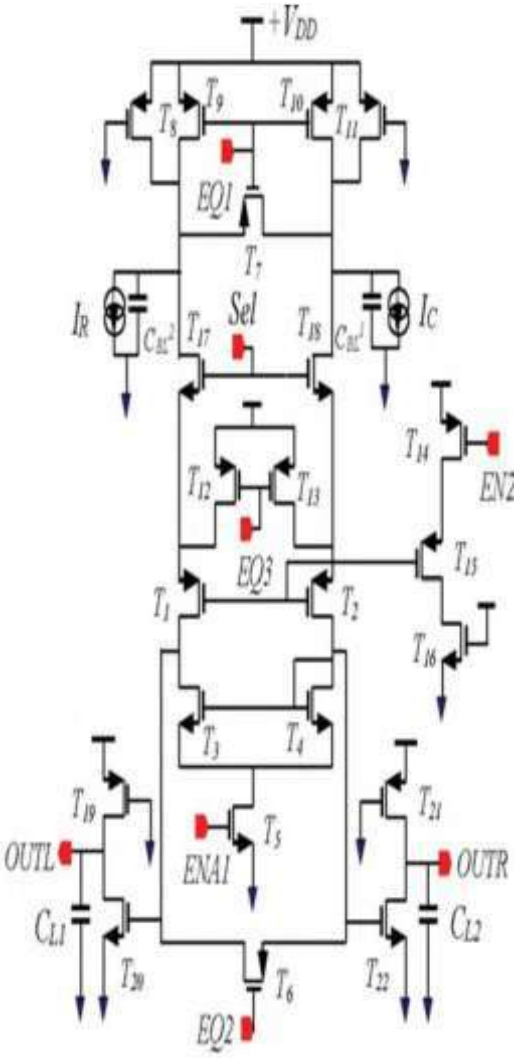

Fig 2: Proposed Sense Amplifier circuit

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CIRCUIT DIAGRAM

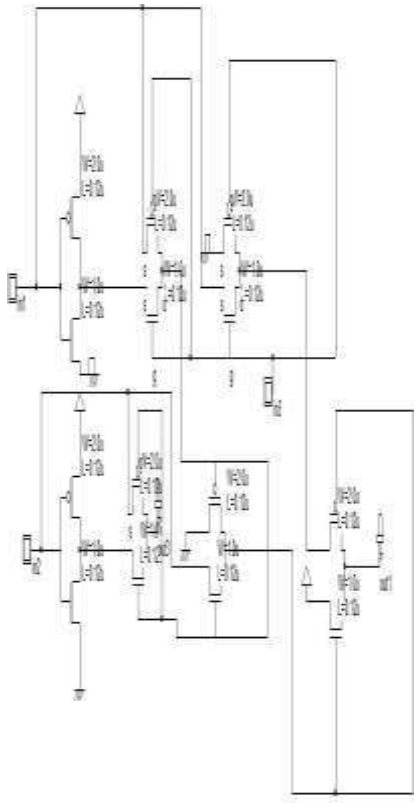

Fig 3 : PMOS Sense Amplifier

2.WORKING PRINCIPLE

It has three inputs and two outputs with five stages. It has Inversion amplifier means it inverse the input and perform the circuit and final output is given as inverse output for avoiding of confusion. Stages help for getting high performance with low power dissipation. It is the combination of PMOS and NMOS transistors which performs PMOS as Leading and NMOS as Lagging.

The circuit consists of 7 CMOS transistors which is the combination of PMOS and NMOS. When we provide inputs we get different type of outputs (don't care condition) according to inputs provided. When inputs are Low ,LED is in OFF state. When inputs are High, LED is in ON state.

3.SOFTWARE

DSCH Microwind is basically digital schematic circuit designing software. This is microwind simulation software which allows the users to simulate and design integrated circuit at physical description level. This is user friendly circuit simulation software and it supported by huge symbol libraries. Microwind unifies schematic entry, pattern based simulator, SPICE extraction of schematic, Verilog extractor, layout compilation, on layout mixed-signal circuit simulation. Microwind software helps to design various types of logic gates: AND, OR, NOR, NAND, XOR and many advanced design included with half adder, full adder etc.

The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user friendly environment for hierarchical logic design, and fast simulation with delay analysis which allows the design and validation of complex logic structures. DSCH also features the symbols, models and assembly support for 8051 and PIC 16F84 controllers. Designers can create logic circuits for interfacing with these controllers and verify software programs using DSCH.

In the first part of this article we will discuss the basic logic circuit. In the next part we will move to advanced design. Let's consider 2-input AND gate. Though most of you know AND gate operation but this article is totally introductory level discussion. there is no input signal so that the output is zero. A HIGH output results only if all the inputs to the AND gate are HIGH If none or not, all inputs to the AND gate are HIGH, a LOW output result. The function can be extended to any number of inputs.

- User-friendly environment for rapid design of logic circuits.
- Supports hierarchical logic design.
- Added a tool on fault analysis at the gate level of digital. Faults: Stuck-at-1, stuck-at-0.The technique allows

injection of single stuck-at fault at the nodes

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of the circuit.

- Improved interface between DSCH and Winspice.
- Handles both conventional pattern- based logic simulation and intuitive on screen mouse-driven simulation.
- Built-in extractor which generates a SPICE netlist from the schematic diagram(Compatible with PSPICETM and WinSpiceTM).
- Generates a VERILOG description of the schematic for layout conversion.

4.ADVANTAGES,DISADVANTAGES & APPLICATIONS

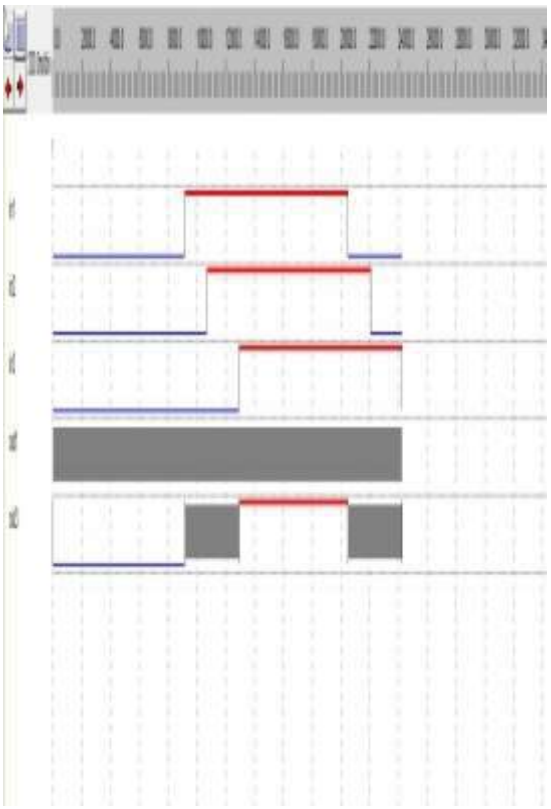
- This proposed sense amplifier which is implemented in PMOS process can work at voltage as low as 1V.
- As the proposed SA works at 3.3V, this design has 14% and 63% power delay product Improvement over the advanced current latch SA and conventional sense amplifier, respectively.
- Area is reduced by minimizing of transistors. Sense delay is also reduced

Disadvantages:

- Due to process variations, current mismatch in the evaluation branches of the sense amplifier circuit, resulting in operational failures. Size of this sense amplifier architecture is large.
- The worst power consumption is observed in this type of sense amplifier.

APPLICATION

- **Memory units.**
- Microprocessors.
- Microcontrollers .
- Computers**.**



5.RESULT

Fig.4: PMOS sense Amplifer Result.

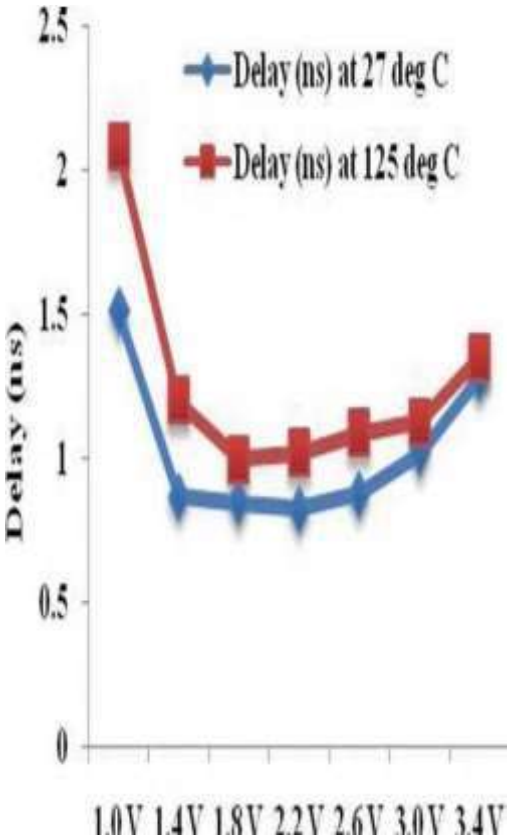


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Fig.5: Sensing delay vs Different Voltage.

6..CONCLUSION & FUTURE SCOPE

The main aim of this project is to provide low power dissipation with highperformance and less sense delay in memory units.

The proposed SA for NVM shows that capacitive coupling with the SA in order to couple the load results in lower power dissipation due to lowering of the coupling effect at nodes, also the proposed SA senses output faster at a lower voltage offset. The proposed SA for SRAM cell shows that when body biasing is used in order to strengthen the positive feedback in the cross coupled SA topology, the SA gives faster results due to lowering of threshold voltages of pull downs

Future Scope:

It has been established that SAs form an integral part of any memory and thus any improvement in the speed, yield and offset ofthe SA will contribute to significant improvement in the performance of memory circuits and such improvements will help bridge up the gap between processor speed and memory. In the future more such topologies could be explored and the current topologies could be analysed for layout work and chip area. Delay can be further reduced by improving the circuit design. Affect of processvariations and corner variations on the performance of the proposed sense amplifiers are not included. So effects of these variations are removed by proper design of circuits and accurate simulations. Yield measurements can be done.

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