Sri Indu Institute of Engineering & Technology

Recognized Under 2(f) of UGC Act 1956
Approved by AICTE, New Delhi
Affiliated to JNTUH, Hyderabad.

COURSE FILE

ON

ANALOG AND DIGITAL ELECTRONICS

Course Code - CS301ES

II B.Tech I-SEMESTER

A.Y.: 2022-2023

Prepared by

Mrs. S. ALEKHYA

Assistant Professor

B. Rahia Kaur
Computer Science & Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH.
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510.

PRINCIPAL
Sri Indu Institute of Engineering & Tech.
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Academic Year	2022-2023
Course Title	ANALOG AND DIGITAL ELECTRONICS
Course Code	CS301ES
Programme	B.Tech
Year & Semester	II year I-semester
Branch & Section	CSE-A
Regulation	R18
Course Faculty	Mrs. S. ALEKHYA, Assistant Professor

Index of Course File

S. No.	Name of the content
1	Institute vision and mission
2	Department vision and mission /PEO
3	POs /PSOs
4	Course Syllabus with Structure
5	Course Outcomes (CO)
6	Mapping CO with PO/PSO; Course with PO/PSO with Justification
7	Academic Calendar
8	Time table - highlighting your course periods including tutorial
9	Lesson plan with number of hours/periods, TA/TM, Text/Reference book
10	Web references
11	Lecture notes
12	List of Power point presentations / Videos
13	University Question papers
14	Internal Question papers, Key with CO and BT
15	Assignment Question papers mapped with CO and BT
16	Result Analysis to identify weak and advanced learners - 3 times in a semester
17	Result Analysis at the end of the course
18	Remedial class for weak students - schedule and evidences
19	Advance Learners- Engagement documentation
20	CO, PO/PSO attainment sheets
21	Attendance register (Theory/Tutorial/Remedial) - Teacher/Course delivery record; Continuous evaluation
22	Course file (Digital form)

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To continuous assess of teaching-learning process through institute-industry collaboration..

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students fraternity.

IM4: To create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders

B. Rahia Kanth
Computer Science & Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH.
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510.

PRINCIPAL
Sri Indu Institute of Engineering & Tech.
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a prominent knowledge hub for learners, strive for educational excellence with innovative and industrial techniques so as to meet the global needs.

Mission:

DM1 : To provide ambience that enhances innovations, problem solving skills, leadership qualities, decision making, team-spirit and ethical responsibilities.

DM2 : To impart quality education with professional and personal ethics, so as to meet the challenging technological needs of the industry and society.

DM3 : To provide academic infrastructure and develop linkage with the world class organizations to strengthen industry-academia relationships for learners.

DM4 : To provide and strengthen new concepts of research in the thrust area of Computer Science and Engineering to reach the needs of Government and Society.

B. Rahul Kaul
Computer Science & Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH.
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510.

PRINCIPAL
Sri Indu Institute of Engineering & Tech.
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

PROGRAM EDUCATIONAL OBJECTIVES

PEO1: To develop trained graduates with strong academic and technical skills of modern computer science and engineering.

PEO2: To promote trained graduates with leadership qualities and the ability to solve real time problems using current techniques and tools in interdisciplinary environment.

PEO3: To motivate the graduates towards lifelong learning through continuing education and professional development.

PROGRAM SPECIFIC OUTCOMES

PSO1 : **Professional Skills:** To implement computer programs of varying complexity in the areas related to Web Design, Cloud Computing, Network Security and Artificial Intelligence.

PSO2: **Problem-Solving Skills**: To develop quality products using open ended programming environment.

B. Rahia Kaur
Computer Science & Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH.
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510.

PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

PROGRAMME OUTCOMES (POs)

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design/development of solutions:**Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO6: **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech. in COMPUTER SCIENCE AND ENGINEERING

COURSE STRUCTURE & SYLLABUS (R18)

Applicable From 2018-19 Admitted Batch

II YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	CS301ES	Analog and Digital Electronics	3	0	0	3
2	CS302PC	Data Structures	3	1	0	4
3	MA303BS	Computer Oriented Statistical Methods	3	1	0	4
4	CS304PC	Computer Organization and Architecture	3	0	0	3
5	CS305PC	Object Oriented Programming using C++	2	0	0	2
6	CS306ES	Analog and Digital Electronics Lab	0	0	2	1
7	CS307PC	Data Structures Lab	0	0	3	1.5
8	CS308PC	IT Workshop Lab	0	0	3	1.5
9	CS309PC	C++ Programming Lab	0	0	2	1
10	*MC309	Gender Sensitization Lab	0	0	2	0
		Total Credits	**15**	**1**	**12**	**21**

II YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	CS401PC	Discrete Mathematics	3	0	0	3
2	SM402MS	Business Economics & Financial Analysis	3	0	0	3
3	CS403PC	Operating Systems	3	0	0	3
4	CS404PC	Database Management Systems	3	1	0	4
5	CS405PC	Java Programming	3	1	0	4
6	CS406PC	Operating Systems Lab	0	0	3	1.5
7	CS407PC	Database Management Systems Lab	0	0	3	1.5
8	CS408PC	Java Programming Lab	0	0	2	1
9	*MC409	Constitution of India	3	0	0	0
		Total Credits	**18**	**2**	**8**	**21**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, NewDelhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510
Website: https://siiet.ac.in/

Department of Computer Science and Engineering

Course Outcomes

Course : ANALOG & DIGITAL ELECTRONICS(C211)

Class: II-I SEM –CSE-A SECTION

After completing this course , the student will be able to:

C211.1	Know the characteristics of various components like pn junction diodes, zener diodes & their applications. (Knowledge , Understand)
C211.2	Understand the utilization of Transistors. (Application, Creation)
C211.3	Design and analyze small signal amplifier circuits. (Analysis, Synthesis)
C211.4	Know the Logic gates & Learn Postulates of Boolean algebra.(Knowledge, Understand)
C211.5	Minimization of Boolean Functions &Design and analyze Combinational logic circuits.(Knowledge, Analysis)
C211.6	Design and analyze and sequential circuits.(Knowledge, Analysis)

Mapping of course outcomes with program outcome

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C211.1	3	2	3	-	-	-	-	-	1	-	-	2	2	1
C211.2	3	2	2	-	-	-	-	-	-	-	-	2	2	-
C211.3	3	2	3	-	-	-	-	-	-	2	3	-	-	-
C211.4	3	2	2	-	-	-	-	-	-	2	1	-	2	-
C211.5	3	2	3	-	-	-	-	-	1	-	3	-	-	1
C211.6	3	2	2	-	-	-	-	-	-	-	3	2	-	-
C211	3	2	2.5	-	-	-	-	-	1	2	2.5	2	2	1

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, NewDelhi and Affiliated toJNTUH, Hyderabad)

Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam(M) ,Ranga Reddy Dist.,Telangana–501510

Website: https://siiet.ac.in/

CO-PO mapping Justification

C211.1 Know the characteristics of various components like pn junction diodes, zener diodes & their applications (Knowledge, Understand)

	Justification
PO1	Students will be able to Students will be able to understand open circuited P-N junction
PO2	Students will be able to understand how the diode acts as rectifierand study the characteristics of rectifiers.
PO3	Students will be able to understand the V-I characteristics of P-N junction.
PO9	Students will be able to understand the temperature effects anddiode resistance
PO12	Know about drift and diffusion capacitances.
PSO1	Students will be able to understand diode switching times.
PSO2	Students will be able to understand the concept of breakdown indiodes and study the operation and characteristics of Zener diode.

C211.2 Understand the utilization of Transistors. (Application , Creation)

	Justification
PO1	To study the operation of transistor as an amplifier.
PO2	To study the characteristics of CB,CE,CC configurations.
PO3	Compare various configurations of transistors.
PO12	Understand the concept of operating point and purpose of biasing.
PSO1	Study about bias compensation,thermal runaway.

C211.3 Design and analyze small signal amplifier circuits. (Analysis, Synthesis)

	Justification
PO1	Explain the operation of transistor at low frequencies.
PO2	Explain the operation of CE amplifier, study its frequency responseand gain bandwidth product.
PO3	Understand the operation of emitter follower.
PO11	Explain the operation of RC coupled two cascaded CE andmultistage CE amplifiers.
PO12	Students will be able to understand the operation, V-Icharacteristics of JFET, MOSFFET.

C211.4 Know the Logic gates & Learn Postulates of Boolean algebra.. (Knowledge, Understand)

	Justification
PO1	Students will be able to understand the arithmetic operations carried by digital systems.
PO2	Students will be able to understand the OR, AND, NOT, EX-OR,DTL gates and modified DTL gates.
PO3	Students will be able to understand the RTL and modified CMOS gates.
PO10	Students will be able to Solve the Complements.
PO11	Students will be able to understand the EX-OR function.
PSO1	Students will be able to Understand the Boolean Laws & Theorems.

C211.5 Minimization of Boolean Functions &Design and analyze Combinational logic circuits(Knowledge, Analysis)

	Justification
PO1	To design functions using universal gates.
PO2	Students will be able to understand the design and analysis ofsequential logic circuits.
PO3	Students will be able to understand the
PO9	Students will be able to analyze the design of decoders, encoders.
PO11	To design Comparators, Multipliers.
PSO2	Students will be able to analyze the design of multiplexers & De multiplexers

C211.6 Design and analyze combinational and sequential circuits. (Knowledge, Analysis)

	Justification
PO1	Students will be able to understand the design and analysis ofcombinational logic circuits.
PO2	Students will be able to understand the design and analysis ofSequential logic circuits.
PO3	Students will be able to understand construction of latches and flipflops.
PO11	Analyse the clocked sequential circuits and perform state reductionand assignments.
PO12	Students will be able to understand the concept of memory.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

ACADEMIC CALENDAR 2022-23

B. Tech./B.Pharm. II YEAR I & II SEMESTERS

I SEM

S. No	Description	Duration	
		From	To
1	Commencement of I Semester classwork	**28.11.2022**	
2	1st Spell of Instructions	28.11.2022	21.01.2023 (8 Weeks)
3	First Mid Term Examinations	23.01.2023	30.01.2023 (1 Week)
4	Submission of First Mid Term Exam Marks to the University on or before	04.02.2023	
5	2nd Spell of Instructions	31.01.2023	29.03.2023 (8 Weeks)
6	Second Mid Term Examinations	31.03.2023	08.04.2023 (1 Week)
7	Preparation Holidays and Practical Examinations	10.04.2023	15.04.2023 (1 Week)
8	Submission of Second Mid Term Exam Marks to the University on or before	15.04.2023	
9	End Semester Examinations	17.04.2023	29.04.2023 (2 Weeks)

Note: No. of Working / Instructional Days: 93

II SEM

S. No	Description	Duration	
		From	To
1	Commencement of II Semester classwork	**01.05.2023**	
2	1st Spell of Instructions (including Summer Vacation)	01.05.2023	08.07.2023 (10 Weeks)
3	**Summer Vacation**	15.05.2023	27.05.2023 (2 Weeks)
4	First Mid Term Examinations	10.07.2023	15.07.2023 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	22.07.2023	
6	2nd Spell of Instructions	18.07.2023	11.09.2023 (8 Weeks)
7	Second Mid Term Examinations	12.09.2023	16.09.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	19.09.2023	23.09.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	23.09.2023	
10	End Semester Examinations	25.09.2023	07.10.2023 (2 Weeks)

Note: No. of Working / Instructional Days: 92

24/11/22

REGISTRAR

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC)
Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956
(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

TIME TABLE FOR A.Y 2022-23

Class: II-B. Tech CSE -A **Semester: I** **LH. NO: A-301** **W.E.F:28-11-2022**

Period/ Day	1 9:40-10:30	2 10:30-11:20	3 11:20-12:10	4 12:10-1:00	1:00-1:30	5 1:30-2:20	6 2:20-3:10	7 3:10-4:00
Monday	COSM	ITWS LAB(BATCH-I)/ A&DE LAB(BATCH-II)			LUNCH	A&DE	DS	C++
Tuesday	COSM	C++	COA	DS		A&DE	CO-C/SS/DAA	
Wednesday	C++	COSM	INT	COA		DS LAB(BATCH-I)/ C++ LAB(BATCH-II)		
Thursday	DS	GS LAB		COSM/DS(T)		C++	A&DE	SPORTS
Friday	COA	DS LAB(BATCH-II)/ C++ LAB(BATCH-I)				A&DE	LIB	DS/COSM(T)
Saturday	C++	DS	COUN	COA		ITWS LAB(BATCH-II)/ A&DE LAB(BATCH-I)		

(T) – Tutorial (concern faculty)

Subject Code	Subject Name	Name of the Faculty	Subject Code	Subject Name	Name of the Faculty
CS301ES	Analog and Digital Electronics	Mrs. S.Alekhya	CS309PC	C++ Programming Lab	Mrs P H Swarna Rekha/ Mrs.P.Souwjanya/ Mrs.G.Swapna
CS302PC	Data Structures	Mrs. D.Rajeshwari	MC309	Gender Sensitization Lab	Mrs S Swapna
MA303BS	Computer Oriented Statistical Methods	Mrs. B.Ramadevi		CO-C/SS/DAA	Mrs. D.Rajeshwari
CS304PC	Computer Organization and Architecture	Dr. Sasikumar D	Sports	Sports	Mr K Veera Kishore
CS305PC	Object Oriented Programming Using C++	Mrs P H Swarna Rekha	Internet	Internet	Mrs. Ch Sai Vijaya
CS306ES	Analog and Digital Electronics Lab	Mrs. S.Alekhya	LIB	Library	Mrs P H Swarna Rekha
CS307PC	Data Structures Lab	Mrs. D.Rajeshwari/ Mrs D.Uma/ Mrs.A.Sudha	COUN	Counselling	Mrs.R.Sravanthi
CS308PC	IT Workshop Lab	Mrs T Ramya Priya/ Mrs.Ch.Sai Vijaya/ Mrs. Jakkala Priyanka			
Class In-Charge : Mrs. D.Rajeshwari		Mentor 1 : Mrs. D.Rajeshwari		Mentor 2: Mrs P H Swarna Rekha	

Class In-Charge HOD PRINCIPAL

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, NewDelhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510

Website: https://siiet.ac.in/

LESSON PLAN

Course Title	ANALOG AND DIGITAL ELECTRONICS
Course Code	CS301ES
Programme	B.Tech
Year & Semester	II-year I-semester
Regulation	R18
Course Faculty	Mrs. S. ALEKHYA, Assistant Professor , CSE

.

S.NO	UNIT	TOPIC	No. of Sessions Planned	Teaching Method/ Aids	REFERENCE
1	I	Introduction to Semiconductors & Their types	1	BB	T1,R1
2		Formation of PN Junction& Open circuited P-N Junction	1	BB	T1,R1
3		Understand how the diode acts as rectifier and study thecharacteristics of rectifiers	1	BB	T1,R1
4		Diode Resistances & Problems	1	BB	T1,R1
5		Diode Switching Times & Breakdown mechanisms	1	BB	T1,R1
6		Diode capacitances, Introduction to Rectifiers	1	BB	T1,R1
7		Operation of Tunnel diode & LED	1	BB	T1,R1
8		Types of Rectifiers & Half wave Rectifier working	1	BB	T1
9		Full Wave Rectifier Working	1	BB	T1,R1
10		Efficiency& Ripple factor of Rectifiers	1	BB	T1
11		Clippers, Clampers	1	BB	T1,R1
12		Voltage Comparator	1	BB	T1
13		Capacitor Filter &Inductor Filter Working	1	BB	T1
14		Problems on Rectifiers	1	BB	T1

15		Introduction to transistors, Types& Construction	1	BB	T1,R1
16		Working of NPN & PNP Transistor	1	BB	T1,R1
17		CB Configuration Characteristics	1	BB	R1
18		CE Configuration Characteristics	1	BB	T1,R1
19		CC Configuration Characteristics	1	BB	T1,R1
20		Comparison of Transistor Configurations	1	BB	R1
21		Transistor as an Amplifier	1	BB	T1,R 1
22		Load line Analysis	1	BB	T1
23		Operating point & Stabilization & Need of Biasing	1	BB	T1,R1
24	**II**	Various Biasing techniques	1	BB	R1
25		Base Resistor biasing Technique	1	BB	T1,R1
26		Thermal Run away, Bias Compensation Techniques	1	BB	T1
27		Transistor at low Frequencies	1	BB	R1
28		CE Amplifier Frequency response	1	BB	T1,R1
29		Gain bandwidth Product	1	BB	T1,R1
30		Two stage RC Coupled Amplifier	1	BB	T1,R1
31		Multistage Amplifiers	1	BB	R1
32		Introduction to FETs, Difference between BJT & FET	1	BB	T1,R1
33		Construction & Working of JFET	1	BB	T1,R1
34		Drain Characteristics of JFET	1	BB	T1,R1
35		Construction &Working of E-MOSFET	1	BB	T1,R1
36		Construction & Working of D-MOSFET	1	BB	T1,R 1
37		Operation of Low frequency CS, CD Amplifiers	1	BB	T1,R1
38	**III**	Introduction to Digital Electronics & Number Systems	1	BB	T2,R2
39		OR, AND, NOT, EX-OR,NAND and NOR Gates	1	BB	T2,R2
40		DTL Gates, Modified DTLGates	1	BB	R2
41		RTL, DCTLand CMOS gates	1	BB	T2,R2
42		HTL and TTLgates and their out put stages	1	BB	T2
43		Comparison Of Various Logic Families.	1	BB	T2,R2
44		Realization of all Gates using Universal gates	1	BB	T2,R2
45		De-Morgan's Law	1	BB	T2,R2

46		Introduction to Boolean laws & theorems	1	BB	T2,R2
47		Properties of Boolean Algebra	1	BB	T2,R2
48		Canonical & standard Forms of Boolean functions	1	BB	R2
49		Digital Logic gates	1	BB	T2,R2
50		K-Map Method to simplify Boolean functions	1	BB	T2,R2
51		Don't Care Conditions & Importance	1	BB	T2,R2
52		Realization of Boolean function using NAND	1	BB	T2
53	**IV**	Realization of Boolean function using NOR Implementation	1	BB	T2,R2
54		Exclusive-OR Function	1	BB	T2
55		Operation of Binary Adder- Subtractor	1	BB	T2
56		Decimal Adder	1	BB	T2,R2
57		Various types of Binary Multiplier	1	BB	T2,R2
58		Magnitude Comparator	1	BB	T2,R2
59		Encoders	1	BB	R2
60		Decoders	1	BB	T2,R2
61		Multiplexers	1	BB	T2,R2
62		Introduction to Sequential Circuits, Comparison between Sequential & Combinational Logic Circuits	1	BB	T2,R2
63		Latches & Flip Flops	1	BB	T2
64		Analysis of Clocked Sequential Circuits	1	BB	R2
65		State Reduction and Assignment	1	BB	T2,R2
66	**V**	Various Types of Shift Registers	1	BB	T2,R2
67		Ripple Counters	1	BB	T2,R2
68		Comparison between Synchronous counters	1	BB	R2
69		Various Memories	1	BB	T2

TEXTBOOKS:

1. Integrated Electronics: Analog and Digital Circuits and Systems, 2/e, Jaccob Millman, Christos Halkias and Chethan D. Parikh, *Tata McGraw-Hill Education*, India, 2010.
2. Digital Design, 5/e, Morris Mano and Michael D. Cilette, *Pearson*, 2011.

REFERENCE BOOKS:

1. Electronic Devices and Circuits, Jimmy J Cathey, *Schaum's outline series*, 1988.
2. Digital Principles, 3/e, Roger L. Tokheim, *Schaum's outline series*, 1994.

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, NewDelhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510

Website: https://siiet.ac.in/

WEB REFERENCES

S.NO	WEB LINK
1	https://youtu.be/Xmu31a-59vw?si=gfJXSZViN8mdPQWt
2	https://youtu.be/EW_2MhFu7tE?si=4n6QMxzw1_fGBc9e
3	https://youtu.be/7ukDKVHnac4?si=allIyPwtTRr3x7GC
4	https://youtu.be/PMOaS967Yus?si=XZ8MiVQCaC2PWcZ6
5	https://drive.google.com/file/d/13iz8a_gtYePRHcebU6k_e938rNcl8sg9/view?usp=sharing
6	https://youtu.be/y-aYzGdlM-8?si=qD8NeC7TweFvfGR4

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, NewDelhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510

Website: https://siiet.ac.in/

LECTURE NOTES

UNIT- 1 LINK:
https://drive.google.com/file/d/1wVpCU_v7tpZPv0N4xIcg28Mz6qzvOHld/view?usp=drive_link

UNIT- 2 LINK:
https://drive.google.com/file/d/1s2a8_sCDp6lIB2K6sQHu1nWpw5T2X0lI/view?usp=sharing

UNIT- 3 LINK:
https://drive.google.com/file/d/1Agf57FMrVJw3xvzCHkQWooYlVv4pJCDi/view?usp=sharing

UNIT- 4 LINK:
https://drive.google.com/file/d/1bee1J8tVAOcJ2BWwJ8g1PqrgSnbLDQIu/view?usp=sharing

UNIT- 5 LINK:

https://drive.google.com/file/d/1wmuasAskyEz2el5lCedE2P8HfzC9NFy9/view?usp=sharing

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, NewDelhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510

Website: https://siiet.ac.in/

List of Power point presentations

Unit-1 Link :

https://drive.google.com/file/d/1SJubq18YAq5gTvZocoSsBghGO_Q_ZyKg/view?usp=sharing

Unit-2 Link :

https://drive.google.com/file/d/1J3meKz5Mko9FJ_ZiMFD5ZhOMMaD1_c_-/view?usp=drive_link

Unit-3 Link :

https://drive.google.com/file/d/14sGTs3zD9jw8UgJq_cyrfE5P9dcAHpbb/view?usp=sharing

Code No: 153AB **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, October - 2020
ANALOG AND DIGITAL ELECTRONICS
(Common to CSE, IT)

Time: 2 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a)	Define Diffusion capacitance? Also derive the expression for C_D?	
b)	Draw and explain the V-I characteristics of a tunnel diode?	[8+7]
2.a)	What is LED? Explain the construction of LED in brief?	
b)	Explain the working of a full wave rectifier with necessary waveforms?	[7+8]
3.a)	Explain the input and output characteristics of common base configuration.	
b)	Explain thermal run away and thermal stability.	[8+7]
4.	Analyse CE-CE amplifier interms of gains and Impedances.	[15]
5.a)	Draw and explain the CS amplifier with current source load.	
b)	Explain the small signal MOSFET circuit model.	[8+7]
6.a)	Explain ECL gate and write the advantages and disadvantages.	
b)	Draw CMOS NOT gate and then explain the same.	[8+7]
7.	Simplify the following Boolean function using Quine – McClusky method. $F(A, B, C, D) = \sum m (0, 2, 3, 6, 7, 8, 10, 12, 13)$	[15]
8.a)	What is state assignment? Explain with a suitable example?	
b)	Realize D and T flip flops using Jk flip flops.	[8+7]

---ooOoo---

Code No: 153AB **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2021
ANALOG AND DIGITAL ELECTRONICS
(Common to CSE, IT, ITE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Derive the expression for ripple for the circuit FWR with inductor filter.
b) Explain the working of semiconductor photo diode. [8+7]

2.a) Explain V-I characteristics of a tunnel diode and write its applications.
b) Define clipping and clamping circuits. Differentiate clipping and clamping circuits. [7+8]

3.a) Draw the circuit diagram of an NPN junction transistor in CE configuration and describe its characteristics.
b) For the transistor amplifier circuit, when signal changes by 0.012 V, the base current changes by 9 μA and collector current by 1.3 mA. If the collector load R_C = 6 KΩ, R_L = 12 KΩ. Determine input resistance, current gain and voltage gain. [9+6]

4.a) What is the necessity of biasing circuits? Derive the expression for stability factor of self-bias circuit.
b) Derive the expressions for Zi, Zo and Av for common drain J-FET amplifier. [8+7]

5.a) Draw a totem-pole output buffer with a TTL gate. Explain its operation.
b) Draw the circuit of an improved version of D.T.L. 3-input NAND gate, and explain its operations with the help of Truth Table. If h_{FE} of each transistor is 40, find FAN-OUT of the circuit. [8+7]

6.a) Simplify the following function using K-map.
$F(A,B,C,D) = \Sigma(1,3,4,5,6,11,13,14,15)$
b) Draw the logic circuit of a 3 to 8 decoder and explain its working. [7+8]

7.a) Design a 4-bit comparator circuit using logic gates.
b) Design a modulo 10 counter using JK flipflops and explain its timing diagram. [7+8]

8.a) Using D-Flip flops and waveforms, explain the working of a 4-bit SISO shift register.
b) Difference between static and dynamic RAM. Draw the circuits of one cell of each and explain its working. [7+8]

---ooOoo---

Code No: 153AB **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, September - 2021
ANALOG AND DIGITAL ELECTRONICS
(Common to CSE, IT, ITE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Explain the characteristics and applications of a photodiode.
b) How does the reverse saturation current of a diode varies with temperature? Explain. [7+8]

2.a) Draw a circuit diagram of series inductor filter with half wave rectifier. Explain with input and output waveforms.
b) Explain negative peak clipper with and without reference voltage. [8+7]

3.a) Explain self bias. Derive the expression for S? Why it is widely used.
b) Prove that the transistor acts as an amplifier with suitable circuit diagram. [7+8]

4. Derive the expression for A_{VS}, A_{IS}, R_i, R_o of transistor amplifier using CB configuration. [15]

5.a) Explain the operation and characteristics of N- channel JFET.
b) Discuss any two applications of FET. [8+7]

6.a) Explain about Transistor–Transistor logic. Also mention the types of output configuration.
b) Prove that AND-OR network is equivalent to NAND-NAND network. [8+7]

7.a) Give the simplest logic circuit for following logic equation where d represents don't care conditions.
$F(A,B,C,D) = \sum m(7) + d(10, 11, 12, 13, 14, 15)$.
b) Design a 32:1 multiplexer using 16:1 Mux and 2:1 multiplexer? [9+6]

8.a) Explain 4 bit parallel in serial out shift register.
b) Explain about RAM with neat sketches. [8+7]

---ooOoo---

Code No: 153AB **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, March - 2022
ANALOG AND DIGITAL ELECTRONICS
(Common to CSE, IT, ECM, ITE, CSE(SE), CSE(CS), CSE(N))

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
Each Carries Equal Marks
- - -

1.a) Explain the operation of PN junction under forward bias condition with its characteristics.
b) Describe the operation of Half Wave Rectifier with and without filters. [7+8]

2.a) Explain about RC coupled amplifier and sketch the frequency response plot of an RC coupled amplifier
b) A transistor operating in CB configuration has I_C = 2.98mA, I_E = 3.00 mA and I_{CO} =0.01 mA. What current will flow in the collector circuit of this transistor when connected in CE configuration with a base current of 30μA. [10+5]

3.a) What is thermal runaway? What is the condition for thermal stability in CE configuration?
b) Derive the expression for stability factor S in self-bias circuit. [8+7]

4.a) Explain the operation of JFET and draw the drain and transfer characteristics.
b) Explain about 2 input TTL NAND Gate. [10+5]

5.a) Convert the decimal number $(128.25)_{10}$ into binary, octal, hexadecimal number system.
b) Build basic gates AND, NOT, OR using NAND and NOR gates. [6+9]

6.a) Simplify the following Boolean expression into one literal. W′X(Z′+YZ) + X(W+Y′Z).
b) What is multiplexer? Draw circuit diagram of 8:1 multiplexer. Explain its working in brief. [6+9]

7.a) Design a full subtractor circuit by using K-map method and draw the logic diagram.
b) Explain 4-bit ring counter with circuit diagram and waveforms. [8+7]

8.a) Draw the logic diagram of clocked RS flip-flop using NAND gates and explain its working.
b) With a neat diagram, explain 3-bit parallel in serial out shift register. [7+8]

---ooOoo---

Code No: 153AB **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, April/May - 2023
ANALOG AND DIGITAL ELECTRONICS
(Common to CSE, IT, ECM, ITE, CE(SE), CSE(CS), CSE(N))

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	Give the applications of PN junction diode.	[2]
b)	Discuss about diode switching times.	[3]
c)	Discuss about gain bandwidth product in amplifier using BJT.	[2]
d)	What is thermal runway?	[3]
e)	Define de morgan laws.	[2]
f)	Define the pinch-off voltage. Why the name field effect is used for the device FET?	[3]
g)	Differentiate between encoder and decoder.	[2]
h)	How Decimal Adder different from Binary adder?	[3]
i)	What is excitation table? Write the excitation tables for the SR flip flop.	[2]
j)	What is state assignment? Explain with a suitable example.	[3]

PART – B

(50 Marks)

2.a) Define and derive the equation for diffusion capacitance.
b) Explain positive and negative diode clipper circuits. [4+6]

OR

3.a) Briefly discuss about PN junction diode and light emitting diode.
b) Discuss about half wave rectifier with and without capacitive filter. [5+5]

4.a) Explain the input and output characteristics of a transistor in CE configuration.
b) Draw a Self-bias circuit and explain its operation. Derive the equation for Stability factor. [5+5]

OR

5.a) Explain various methods used for coupling of multistage amplifiers with their frequency response.
b) Draw and explain equivalent circuit of transistor at low frequencies. [6+4]

6.a) Draw the circuit diagram of common drain amplifier and derive expression for voltage Gain using FET .
b) Simplify the following function and realize using universal gates
F (A,B,C) = A'BC' + ABC + B'C' + A'B' [5+5]

OR

7.a) Explain the construction and principle of operation of Enhancement mode N-channel MOSFET.

b) Explain the operation of TTL with neat diagram. [5+5]

8.a) Minimise the following Boolean function using K-map and design a logic circuit using NAND gates.

$$F=\Sigma m\,(0,3,4,7,8,10,12,14)+d(2,6)$$

b) Construct a 3*8 decoder using logic gates and its truth table. [5+5]

OR

9.a) Express the function (xy+z)(y+xz) in canonical SOP and POS forms.

b) Implement the following Boolean function with a multiplexer.

$$F(A,B,C,D)=\sum(1, 3, 4, 11, 12, 13, 14,15)$$ [5+5]

10.a) Draw and explain the logic diagram of 4-bit ring counter with the help of timing diagrams.

b) Realize D-FF and T-FF using JK-FF. [5+5]

OR

11.a) Explain about the universal shift registers.

b) Discuss in detail about various types of ROM. [5+5]

---ooOoo---

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

Set –I

I - Mid Examinations, JAN-2023

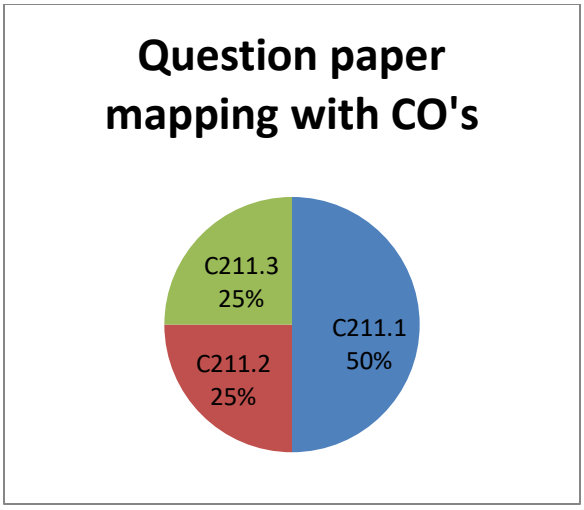
Year &Branch: III CSE (A,B,C),CSE(CS), CSE(IOT) Date:23/01/2023

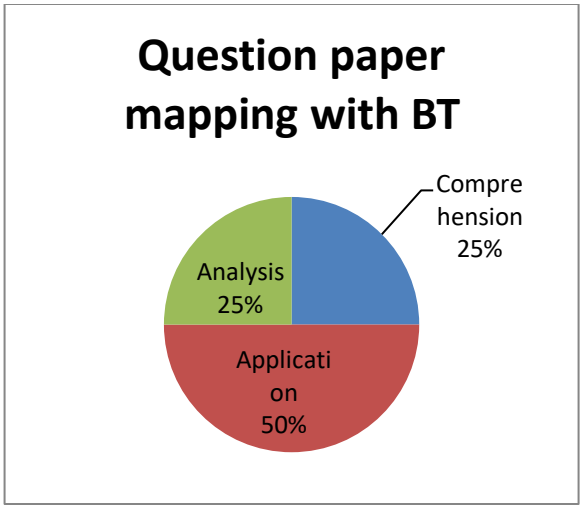
Subject: A&DE Max. Marks: 10 Time: 60 mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

1	Explain the operation of PN junction diode under Forward bias and Explain the V-I characteristics?	(5)	C211.1	(Comprehension)
2.	Define rectifier. Explain Bridge full wave rectifier With a circuit diagram?	(5)	C211.1	(Application)
3	Justify how the transistor acts as an amplifier?	(5)	C211.2	(Application)
4	Compare CB,CE,CC Configurations?	(5)	C211.3	(Analysis)





SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 **Set – II**

II - Mid Examinations, March -2023

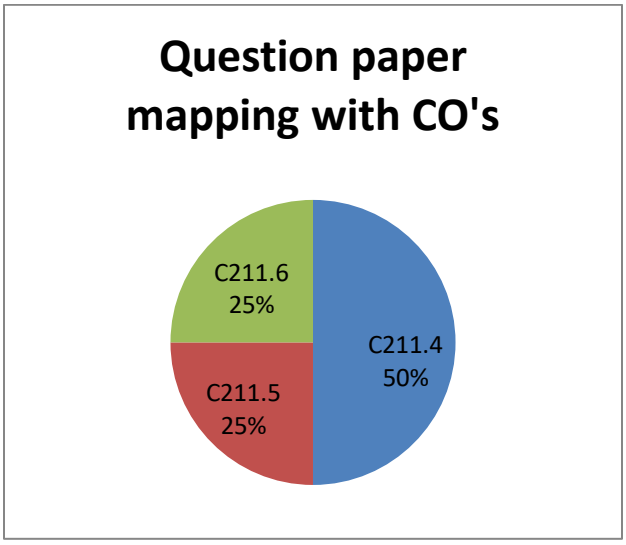
Year &Branch: II CSE (A, B, C),CSE(CS),CSE(IOT) Date: 31-03-2023 (FN)

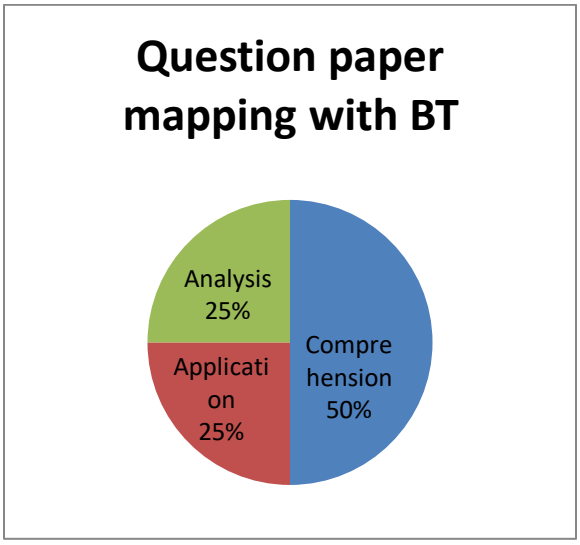
Subject: A&DE Max. Marks: 10 Time: 60mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

1	Compare all the logic families?	(5)	C211.4	(Comprehension)
2.	Simplify the following Boolean Expression using 4 variable K map method and draw the logic circuit for expression. Y=A'B+A'BC+BC'+AB'	(5)	C211.4	(Application)
3	Define Magnitude Comparator? Explain 2-Bit magnitude comparator?	(5)	C211. 5	(Comprehension)
4	Explain NAND and NOR Latch?	(5)	C211. 6	(Analysis)





SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

B-Tech I - Mid Examinations, JAN -2023

Objective Type Exam

Year & Branch: II –CSE(A,B,C),CSE(CS), CSE(IOT) Date:23-01-2023(FN)

Subject: A&DE Max. Marks: 10 Time: 20 mins

Name: ……..Roll No……..

I Choose the correct answers.

1. The diode _____. ( )

(A) is the simplest of semiconductor devices

(B) has characteristics that closely match those of a simple switch

(C) is a two-terminal device

(D) All of the above

2. Which of the following are applications of diode? ( )

(A) Rectifier

(B) Switch

(C) Clippers

(D) all of the above

3. How many terminals does a diode have? ( )

(A)1

(B)2

(C)3

(D)4

4. Ripple factor of half wave rectifier? ( )

(A) 1.21

(B) 0.48

(C)1.1

(D) 0.7

5. In which of the following color(s) is (are) LEDs presently available? ( )

(A) Yellow
(B) White
(C) Orange
(D) All of the above

6. A transistor has---------- ( )
   (A) One PN junction
   (B) Two PN junction
   (C) Three PN junction
   (D) Four PN junction
7. The number of depletion regions in a transistor is------- ( )
   (A) 4
   (B) 3
   (C) 2
   (D) 1
8. The base of a transistor is---------- doped. ( )
   (A) Heavily
   (B)Moderately
   (C)Lightly
   (D) None of the above
9. A Transistor is a-----operated device. ( )
   (A) Current
   (B) Voltage
   (C) Both voltage and current
   (D) None of the above
10. In a transistor is------ ( )
   (A)IC=IB+IE
   (B)IE=IC-IB
   (C)IB=IC+IE
   (D)IE=IB+IC

II .Fill in the Blanks

11. The efficiency of a full wave rectifier_____

12. Write the relation between α & β _____

13. The_____ configuration is widely used

14. Types of diode resistance _____

15. How many types of clippers_____

16. cut-in voltage in Si_____.

17. Units of frequency_____

18. CRO stands for_____.

19. IC= $^{\beta}$IB+_____

20. The Emitter base junction in a transistor is always operated in _____

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

B-Tech II - Mid Examinations, March -2023

Objective Type Exam

Year & Branch: II –CSE(A,B,C),CSE(CS), CSE(IOT) Date:31-03-2023(FN)

Subject: A&DE Max. Marks: 10 Time: 20 mins

Name: ……..Roll No……..

I Choose the correct answers.

1. Expression for AND Gate ( )

   A. Y=A+B

   B. Y=AB

   C. Y=A-B

   D. None of the above

2. Each term in sum of product is called as- -- - -- ( )

   A. Min terms

   B. Max terms

   C. Both A & B

   D. Complimentary terms

3. The universal gate is …… ( )

   A. OR gate

   B. NAND gate

   C. Both A & B

   D. AND gate

4. How many NAND gates are required to construct OR gates ( )

   A. 1

   B. 4

   C. 3

   D. 2

5. What is the radix of hexadecimal number system ( )

A. 2

B. 8

C. 10

D. 16

6.To make a Quad how many Min/Max terms are required in a K-Map ( )

A.2

B.4

C.8

D.1

7. A Karnaugh map (K-map) is a theoretical form of representing _____ ( )

A. Circuit diagram

B. Block diagram

C. Logic diagram

D. Venn diagram

8. When R=1;S=0 the output Q=---------- ( )

A. 0

B .1

C .No Change

D. Undefined

9. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?( )

A. AND or OR gates

B. XOR or XNOR gates

C. NOR or NAND gates

D. AND or NOR gates.

10. Latches are _____ triggered. ( )

A. Level Triggered.

B. Edge Triggered.

C. Count Triggered

D. Pulse Triggered.

II .Fill in the Blanks

1. According to De-Morgan's Theorem (AB)'=_____

2. What are general outputs of a Comparator_____

3. _____ NOR gates are required to construct Ex-OR gates.

4. Multiplexer is also called as_____.

5. How many selective lines are needed for 8x1 MUX_____.

6. The terms present in Product of sums are called as_____.

7. Encoder Contains _____ no. of inputs &_____ no. of outputs.

8. Examples of Sequential logic circuits_____

9. Flip Flops are _____ Triggered.

10. ROM is a _____Memory.

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

I - Mid Examinations, JAN-2023

Year &Branch: III CSE (A,B,C),CSE(CS), CSE(IOT) Date:23/01/2023(FN)

Subject: A&DE Max. Marks: 10 Time: 60 mins

ANSWERKEY

Descriptive paper key link:

https://drive.google.com/file/d/19Fwx2QxI0yrcYsez_Vs7zdxc5ALx7EPp/view?usp=drive_link

Objective Key Paper

I Choose the correct answers

1. D
2. D
3. B
4. A
5. D
6. B
7. C
8. C
9. A
10. D

II . Fill in the Blanks

1. 81.2
2. α = β/(1+β) ; $\beta = \frac{\alpha}{(1-\alpha)}$
3. CE
4. Static, dynamic
5. 3
6. 0.7
7. HZ
8. Cathode Ray Oscilloscope
9. $(1+^{\beta})$ICO
10. forward bias

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

II - Mid Examinations, March -2023

Year &Branch: II CSE (A, B, C),CSE(CS),CSE(IOT) Date: 31-03-2023 (FN)

Subject: A&DE Max. Marks: 10 Time: 60mins

ANSWERKEY

Descriptive paper key link:

https://drive.google.com/file/d/19IYXEWqjXYJduvoQkRRuUSSHWiPmZX7n/view?usp=drive_link

Objective Key Paper

I Choose the correct answers

1. B
2. A
3. B
4. C
5. D
6. B
7. D
8. A
9. C
10. A

II . Fill in the Blanks

1. A'+B'
2. A=B, A>B, A<B
3. 5
4. Data selector
5. 3
6. Max Terms.
7. 2^n inputs &n Outputs
8. Counters, Registers, Flip flops
9. Edge
10. Non Volatile

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, NewDelhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510

Website: https://siiet.ac.in/

A&DE ASSIGNMENT-1 QUESTIONS

1.a) Explain the Operation of PN Junction under Forward Bias?(C211.1) (Comprehension)

b) With a neat Sketch explain the V-I Characteristics of PN Junction Diode? (C211.1) (Comprehension)

2. Discuss the working of Tunnel Diode? (C211.1)(Understanding)

3. Explain the Operation of Bridge Full Wave Rectifier? (C211.1)(Knowledge)

4. Explain the Working of NPN Transistor? (C211.2) (Understanding)

5. Explain how the Transistor acts as an Amplifier? (C211.2) (Application)

6. Write the Comparison Between CB,CE,CC Configurations? (C211.3) (Analysis)

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, NewDelhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510

Website: https://siiet.ac.in/

A&DE ASSIGNMENT-2 QUESTIONS

1. Explain the Construction & Operation of N Channel JFET? (C211.4) (Comprehension)
2. Discuss the Operation of CMOS Circuit? (C211.4)(Understanding)
3. Define Magnitude Comparator? Explain the operation of Two Bit Magnitude Comparator & Draw its Logic Diagram? (C211. 5)(Knowledge)
4. Realize all the gates by using NAND & NOR Logic? (C211.6) (Analysis)
5. Compare all the Logic Families? (C211. 5) (Analysis)

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510
Website: https://siiet.ac.in/

Result Analysis:

Course Title	ANALOG AND DIGITAL ELECTRONICS
Course Code	CS301ES
Programme	B. Tech
Year &Semester	II year I- semester, A sec
Regulation	R18
Course Faculty	Mrs. S. ALEKHYA ,Assistant Professor, ECE

SLOW LEARNERS:

S No	Roll No	No Of Backlogs	Internal-I Status	Internal-II Status
1	21X31A0507	2	18	22
2	21X31A0510	3	20	15
3	21X31A0512	3	18	11
4	21X31A0516	2	19	5
5	21X31A0522	2	24	22
6	21X31A0528	2	23	5
7	21X31A0530	1	25	21
8	21X31A0539	2	23	19
9	21X31A0544	2	10	5
10	21X31A0546	1	21	15
11	21X31A0548	1	22	17
12	21X31A0549	1	21	16
13	21X31A0552	1	22	16
14	21X31A0556	3	23	24
15	21X31A0561	3	21	20

ADVANCED LEARNERS:

S.NO	ROLL.NO.	GATE MATERIAL
1	21X31A0504	Semiconductor Devices ,Transistors, FETs, Rectifiers, Logic Gates, Combinational Logic Circuits, & Sequential Logic Circuits
2	21X31A0506	
3	21X31A0509	
4	21X31A0520	
5	21X31A0525	
6	21X31A0526	
7	21X31A0527	
8	21X31A0533	
9	21X31A0534	
10	21X31A0540	
11	21X31A0545	
12	21X31A0557	
13	21X31A0559	
14	21X31A0560	
15	21X31A0564	
16	21X35A0508	

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, NewDelhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510

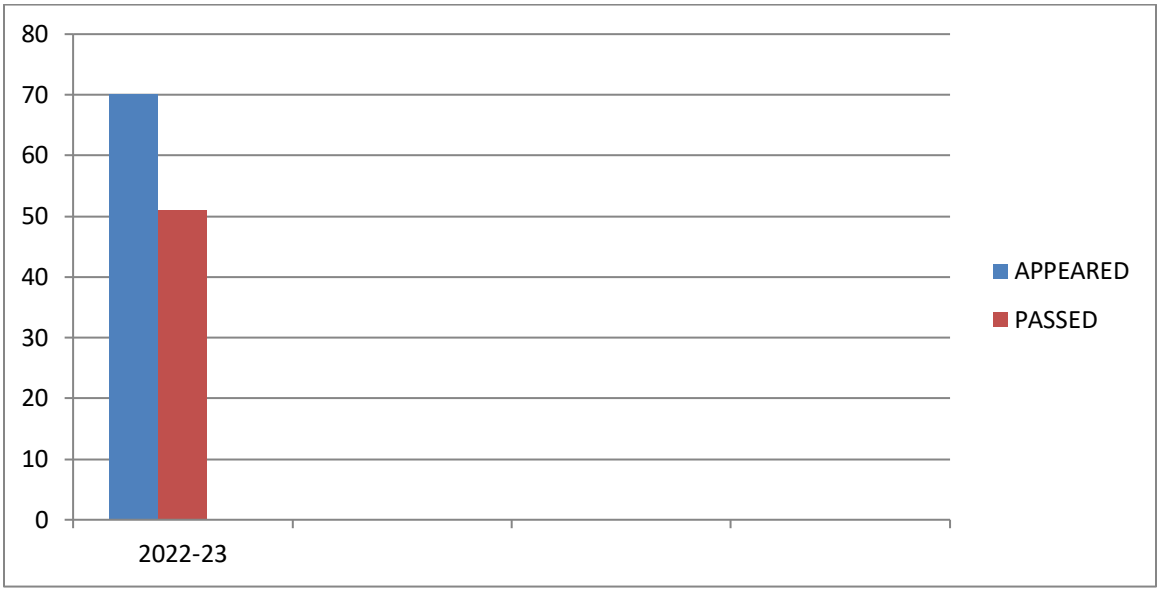
Website: https://siiet.ac.in/

ANALOG & DIGITAL ELECTRONICS RESULT ANALYSIS

CSE-A

ACADAMIC YEAR	COURSE NAME	NUMBEROF STUDENTS		QUESTIONPAPER SETTING		PASS%
		APPEARED	PASSED	INTERNAL	EXTERNAL	
2022-23	ANALOG &DIGITAL ELECTRONICS	70	51	COURSE FACULTY	JNTUH	72.8

ANALOG AND DIGITAL ELETRONICS (C211) RESULT ANALYSIS



SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC)
Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956
(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siet.ac.in/

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

REMEDIAL CLASSES TIME TABLE

A.Y 2022-23

SEMESTER-I

BRANCH/ SEC	MON 4.00 PM-5.00 PM	TUE 4.00 PM-5.00 PM	WED 4.00 PM-5.00 PM	THUR 4.00 PM-5.00 PM	FRI 4.00 PM-5.00 PM
II CSE-A	A&DE	DS	C++	COA	COSM
II CSE-B	DS	A&DE	COSM	C++	COA
II CSE-C	COSM	COA	A&DE	DS	C++
III CSE-A	SE	FLAT	CN	WT	PPL
III CSE-B	WT	CN	SE	PPL	FLAT
III CSE-C	FLAT	WT	PPL	CN	SE
IVCSE-A	C&NS	DM	CC	POE	RTS
IV CSE-B	CC	RTS	C&NS	DM	POE
IV CSE-C	RTS	CC	POE	C&NS	DM

HOD
Computer Science & Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH.
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL
PRINCIPAL
Sri Indu Institute of Engineering & Tech.
Sheriguda(Vill), Ibrahimpatnam,
Dist. Telangana -501 510

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty : S.ALEKHYA Academic Year: 2022-23

Branch & Section: CSE - A Examination: I Internal

Course Name: ELECTRONICS Year: II Semester: I

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj1	A1
Max. Marks ==>		**5**		**5**		**5**		**5**		**10**	**5**
1	21X31A0501	5		4						10	5
2	21X31A0502	3						5		10	5
3	21X31A0503	4						5		9	5
4	21X31A0504	5		5						10	5
5	21X31A0505	4						5		10	5
6	21X31A0506	5						5		10	5
7	21X31A0507			3						10	5
8	21X31A0508	4						5		9	5
9	21X31A0509	5						5		10	5
10	21X31A0510	3						4		8	5
11	21X31A0511	5		5						9	5
12	21X31A0512	4		2						7	5
13	21X31A0513	4						5		8	5
14	21X31A0514	4		4						9	5
15	21X31A0515	5		4						10	5
16	21X31A0516			3				2		9	5
17	21X31A0517	4						5		10	5
18	21X31A0518	5		4						10	5
19	21X31A0519	4						4		10	5
20	21X31A0520	4		4						9	5
21	21X31A0521	4						4		10	5
22	21X31A0522	4						5		10	5
23	21X31A0523	5		5						10	5
24	21X31A0524	5		5						10	5
25	21X31A0525	5		5						10	5
26	21X31A0526	5						5		10	5
27	21X31A0527	4						5		10	5
28	21X31A0528	4		4						10	5
29	21X31A0529			5				5		10	5
30	21X31A0530			5				5		10	5
31	21X31A0531	2						2		8	5
32	21X31A0532	5		1						10	5
33	21X31A0533	5						5		10	5
34	21X31A0534	5				5				10	5
35	21X31A0535	0						2		7	5
36	21X31A0536	4		4						8	5
37	21X31A0537	4						4		10	5
38	21X31A0538	5						5		8	5
39	21X31A0539	3						5		10	5
40	21X31A0540	5						5		10	5
41	21X31A0541	5		3						6	5
42	21X31A0542	5		3						9	5

43	21X31A0543	3		4						7	5
44	21X31A0544	2								3	5
45	21X31A0545	5				5				10	5
46	21X31A0546	3								8	5
47	21X31A0547					2		3		4	5
48	21X31A0548			3				5		9	5
49	21X31A0549	3						3		10	5
50	21X31A0550	3		2						9	5
51	21X31A0552	4						4		9	5
52	21X31A0554	5		5						10	5
53	21X31A0555	4		2						10	5
54	21X31A0556	4						5		9	5
55	21X31A0557			5				5		10	5
56	21X31A0559	4		5						10	5
57	21X31A0560					5		5		10	5
58	21X31A0561	3		3						10	5
59	21X31A0562			5				5		10	5
60	21X31A0563	5		4						5	5
61	21X31A0564					5		5		9	5
62	21X31A0565	5		5						10	5
63	22X35A0501			4				4		10	5
64	22X35A0502	4		4						10	5
65	22X35A0503	4		4						10	5
66	22X35A0504	5		5						10	5
67	22X35A0505	5						5		10	5
68	22X35A0506	4		4						10	5
69	22X35A0507	4		4						10	5
70	22X35A0508	5						5		10	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		56	0	33	0	4	0	33	0	67	70
Number of students attempted		59	0	37	0	5	0	36	0	70	70
Percentage of students scored more than target		95%		89%		80%		92%		96%	100%

CO Mapping with Exam Questions:

CO - 1	Y						Y		Y	Y
CO - 2					Y				Y	Y
CO - 3			Y						Y	Y
CO - 4										
CO - 5										
CO - 6										

% Students Scored >Target %	95%		89%		80%		92%		96%	100%

CO Attainment based on Exam Questions:

CO - 1	95%						92%		96%	100%
CO - 2					80%				96%	100%

CO - 3			89%						96%	100%
CO - 4										
CO - 5										
CO - 6										

CO	**Subj**	obj	Asgn	Overall	Level
CO-1	93%	96%	100%	96%	3.00
CO-2	80%	96%	100%	92%	3.00
CO-3	89%	96%	100%	95%	3.00
CO-4					
CO-5					
CO-6					

Attainment (Internal 1 Examination) = **3.00**

Attainment Level	
1	40%
2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-2)

Name of the faculty: S.ALEKHYA | Academic Year: 2022-23

Branch & Section: CSE - A | Examination: II Internal

Course Name: ANALOG & DIGITAL ELECTRON | Year: II | Semester: I

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj4	A4
Max. Marks ==>		5		5		5		5		10	5
1	21X31A0501	5				2				10	5
2	21X31A0502	5				5				10	5
3	21X31A0503	4						4		9	5
4	21X31A0504	5				5				10	5
5	21X31A0505			1		5				9	5
6	21X31A0506	5		5						10	5
7	21X31A0507	4				4				9	5
8	21X31A0508	4				3				9	5
9	21X31A0509					4				9	5
10	21X31A0510			1						9	5
11	21X31A0511	3				4				8	5
12	21X31A0512					2				4	5
13	21X31A0513	4				4				8	5
14	21X31A0514	4				3				8	5
15	21X31A0515					4		5		9	5
16	21X31A0516			2		3				4	5
17	21X31A0517			4		4				8	5
18	21X31A0518	4				4				8	5
19	21X31A0519	5				5				9	5
20	21X31A0520	5				3				9	5
21	21X31A0521			2				3		4	5
22	21X31A0522	4						3		10	5
23	21X31A0523	5						5		10	5
24	21X31A0524	5						4		10	5
25	21X31A0525			5		5				9	5
26	21X31A0526	5				5				10	5
27	21X31A0527	4				4				10	5
28	21X31A0528			4		3				3	5
29	21X31A0529	5						5		10	5
30	21X31A0530	4						2		10	5
31	21X31A0531			2		4				3	5
32	21X31A0532					3				9	5
33	21X31A0533			5		4				10	5
34	21X31A0534	5				5				10	5
35	21X31A0535			2				3		4	5
36	21X31A0536					4		1		7	5
37	21X31A0537	3						5		10	5
38	21X31A0538	5						1		10	5
39	21X31A0539	3		1						10	5
40	21X31A0540	5				5				10	5
41	21X31A0541	2								9	5
42	21X31A0542					4		3		9	5
43	21X31A0543	4								7	5
44	21X31A0544			2		3				4	5

45	21X31A0545	5				5				10	5
46	21X31A0546	1								9	5
47	21X31A0547					2		3		4	5
48	21X31A0548					2		1		9	5
49	21X31A0549			1				2		8	5
50	21X31A0550							1		8	5
51	21X31A0552	4						2		5	5
52	21X31A0554			5		4				10	5
53	21X31A0555					1		1		10	5
54	21X31A0556	5		4						10	5
55	21X31A0557	5				5				10	5
56	21X31A0559	4				5				10	5
57	21X31A0560	5				5				10	5
58	21X31A0561	4				4				7	5
59	21X31A0562	4						3		8	5
60	21X31A0563	2						2		9	5
61	21X31A0564	3				4				9	5
62	21X31A0565					3				10	5
63	22X35A0501	5				4				10	5
64	22X35A0502			2		4				10	5
65	22X35A0503	1				2				10	5
66	22X35A0504	3				4				9	5
67	22X35A0505			5		4				10	5
68	22X35A0506	5		2						8	5
69	22X35A0507	5		2						8	5
70	22X35A0508	5						5		10	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		40	0	8	0	39	0	13	0	61	70
Number of students attempted		44	0	20	0	45	0	22	0	70	70
Percentage of students scored more than target		91%		40%		87%		59%		87%	100%

CO Mapping with Exam Questions:

CO - 1										
CO - 2										
CO - 3										
CO - 4	Y						Y		Y	Y
CO - 5			Y						Y	Y
CO - 6					Y				Y	Y

% Students Scored >Target %	91%		40%		87%		59%		87%	100%

CO Attainment based on Exam Questions:

CO - 1										
CO - 2										
CO - 3										
CO - 4	91%						59%		87%	100%
CO - 5			40%						87%	100%
CO - 6					87%				87%	100%

CO	Subj	obj	Asgn	Overall	Level
CO-1					
CO-2					
CO-3					
CO-4	75%	87%	100%	87%	3.00
CO-5	40%	87%	100%	76%	3.00
CO-6	87%	87%	100%	91%	3.00

Attainment (Internal Examination-2) = **3.00**

Attainment Level	
1	40%
2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty : S.ALEKHYA Academic Year: 2022-23

Branch & Section: CSE - A Year / Semester: II / I

Course Name: ANALOG & DIGITAL ELECTRONICS

S.No	Roll Number	Marks Secured
1	21X31A0501	26
2	21X31A0502	26
3	21X31A0503	35
4	21X31A0504	47
5	21X31A0505	26
6	21X31A0506	51
7	21X31A0507	15
8	21X31A0508	14
9	21X31A0509	30
10	21X31A0510	16
11	21X31A0511	30
12	21X31A0512	8
13	21X31A0513	29
14	21X31A0514	29
15	21X31A0515	26
16	21X31A0516	7
17	21X31A0517	40
18	21X31A0518	29
19	21X31A0519	29
20	21X31A0520	29
21	21X31A0521	13
22	21X31A0522	29
23	21X31A0523	32
24	21X31A0524	29
25	21X31A0525	31
26	21X31A0526	34
27	21X31A0527	35
28	21X31A0528	12
29	21X31A0529	26
30	21X31A0530	11
31	21X31A0531	5
32	21X31A0532	26
33	21X31A0533	43
34	21X31A0534	51
35	21X31A0535	12
Max Marks		75

S.No	Roll Number	Marks Secured
36	21X31A0536	16
37	21X31A0537	41
38	21X31A0538	29
39	21X31A0539	4
40	21X31A0540	50
41	21X31A0541	26
42	21X31A0542	29
43	21X31A0543	26
44	21X31A0544	6
45	21X31A0545	46
46	21X31A0546	5
47	21X31A0547	26
48	21X31A0548	14
49	21X31A0549	16
50	21X31A0550	13
51	21X31A0552	13
52	21X31A0554	37
53	21X31A0555	29
54	21X31A0556	29
55	21X31A0557	30
56	21X31A0559	26
57	21X31A0560	48
58	21X31A0561	31
59	21X31A0562	32
60	21X31A0563	34
61	21X31A0564	44
62	21X31A0565	32
63	22X35A0501	26
64	22X35A0502	36
65	22X35A0503	29
66	22X35A0504	26
67	22X35A0505	43
68	22X35A0506	29
69	22X35A0507	11
70	22X35A0508	32

Class Average mark	27
Number of students performed above the target	39
Number of successful students	70

Attainment Level	% students
1	40%
2	50%

Percentage of students scored more than target	56%
Attainment level	**3**

3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment

Name of the faculty : S.ALEKHYA
Branch & Section: CSE - A
Course Name: ANALOG & DIGITAL ELECTRONICS

Academic Year: 2022-23
Examination: I Internal
Year: II
Semester: I

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00		3.00	3.00	3.00
CO2	3.00		3.00	3.00	3.00
CO3	3.00		3.00	3.00	3.00
CO4		3.00	3.00	3.00	3.00
CO5		3.00	3.00	3.00	3.00
CO6		3.00	3.00	3.00	3.00
Internal & University Attainment:			3.00	3.00	
Weightage			25%	75%	
CO Attainment for the course (Internal, University			0.75	2.25	
CO Attainment for the course (Direct Method)			3.00		

Overall course attainment level **3.00**

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Program Outcome Attainment (from Course)

Name of Faculty:	S.ALEKHYA	Academic Year:	2022-23
Branch & Section:	CSE - A	Year:	II
Course Name:	ANALOG & DIGITAL ELECTRONIC	Semester:	I

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	3	-	-	-	-	-	1	-	-	2	2	1
CO2	3	2	2	-	-	-	-	-	-	-	-	2	2	-
CO3	3	2	3	-	-	-	-	-	-	2	3	-	-	-
CO4	3	2	2	-	-	-	-	-	-	2	1	-	2	-
CO5	3	2	3	-	-	-	-	-	1	-	3	-	-	1
CO6	3	2	2	-	-	-	-	-	-	-	3	2	-	-
Course	**3.00**	**2.00**	**2.50**						**1.00**	**2.00**	**2.50**	**2.00**	**2.00**	**1.00**

CO	**Course Outcome Attainment**
CO1	3.00
CO2	3.00
CO3	3.00
CO4	3.00
CO5	3.00
CO6	3.00
Overall course attainment level	**3.00**

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainment	**3.00**	**2.00**	**2.50**						**1.00**	**2.00**	**2.50**	**2.00**	**2.00**	**1.00**

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956

(Approved by AICTE, NewDelhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510

Website: https://siiet.ac.in/

ASSIGNMENTS AND ATTENDANCE REGISTER

Assignment-1 Script link:

https://drive.google.com/file/d/1zt62BZKRFl7CIXwiBkyKqZh7mf6EpAap/view?usp=sharing

Assignment-2 Script link:

https://drive.google.com/file/d/1Ljz_6EAB3bfcWfmAu_ebV2oCngCflcRB/view?usp=sharing

Attendance Register Link:

https://drive.google.com/file/d/1IcI0VHYYyJAo7zpJ_NIkkWCjtW1_63XV/view?usp=sharing