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COURSE FILE

ON

DIGITAL SIGNAL PROCESSING LAB

Course Code - EC604PC

III B.Tech II-SEMESTER

A.Y.: 2022-2023

Prepared by

Mr. T. NARESH Assistant Professor

Head of the Department Electronics and Communication Engg. Dept SRI INDU INSTITUTE OF ENGG & TECH Sheriguda(V), Ibrahimpalnam(M), R.R.Dist-501510 Sri Indu Institute of Engineering & Tech Sheriguda(Vill), Ibrahimpatnam R.R. Dist. Telangana-501 510.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Name of the Physical	DIGITAL SIGNAL PROCESSING LAB
laboratory Course Code	EC604PC
Room No	C-002
Name of the lab In	
charge	
Name of the	T.NARESH
faculty In charge	

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INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To Continuous assess of teaching-learning process through institute-industry collaboration.

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.

IM4: To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

Head of the Department Electronics and Communication Engg. Dept SRI INDU INSTITUTE OF ENGG & TECH Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510 Sri Indu Institute of Engineering & Tech Sheriguda(Vill), Ibrahimpatnam R.R. Dist. Telangana-501 510.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

DM1: To facilitate an academic environment that enables student's centric learning.

DM2: To provide state-of-the-art hardware and software technologies to meet industry requirements.

DM3: To continuously update the Academic and Research infrastructure.

DM4: To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

Head of the Department Electronics and Communication Engg. Dept SRI INDU INSTITUTE OF ENGG & TECH Sheriguda(V), ibrahimpalnam(M), R.R.Dist-501 510 Sri Indu Institute of Engineering & Tech Sheriguda(Vill), Ibrahimpatnam R.R. Dist. Telangana-501 510.



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PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

PEO1: Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.

PEO2: Graduates with ability to execute innovative ideas for Research and Development with continuous learning.

PEO3: Graduates inculcated with industry based soft-skills to enable employability.

PEO4: Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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PROGRAM OUTCOMES

- 1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- 2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- 3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- 4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- 5. **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
- 6. **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- 7. **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- 8. **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- 9. **INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- 10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.
- 11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- 12. **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

https://siiet.ac.in

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING COURSE STRUCTURE & SYLLABUS (R18)

Applicable From 2018-19 Admitted Batch

III YEAR I SEMESTER

S. No.	Course Code	Course Title	L	Т	Р	Credits
1	EC501PC	Microprocessors & Microcontrollers	3	1	0	4
2	EC502PC	Data Communications and Networks	3	1	0	4
3	EC503PC	Control Systems	3	1	0	4
4	SM504MS	Business Economics &Financial Analysis	3	0	0	3
5		Professional Elective-I	3	0	0	3
6	EC505PC	Microprocessors & Microcontrollers Lab	0	0	3	1.5
7	EC506PC	Data Communications and Networks Lab	0	0	3	1.5
8	EN508HS	Advanced Communication Skills Lab	0	0	2	1
9	*MC510	Intellectual Property Rights	3	0	0	0
		Total Credits	18	3	8	22

IIIYEARIISEMESTER

S. No.	Course Code	Course Title	L	Т	Р	Credits
1	EC601PC	Antennas and Propagation	3	1	0	4
2	EC602PC	Digital Signal Processing	3	1	0	4
3	EC603PC	VLSI Design	3	1	0	4
4		Professional Elective-II	3	0	0	3
5		Open Elective-I	3	0	0	3
6	EC604PC	Digital Signal Processing Lab	0	0	3	1.5
7	EC605PC	e-CAD Lab	0	0	3	1.5
8	EC606PC	Scripting Languages Lab	0	0	2	1
9	*MC609	Environmental Science	3	0	0	0
		Total Credits	18	3	8	22

EC604PC: DIGITAL SIGNAL PROCESSING LAB

B.Tech. III Year II Semester

L T P C 0 0 3 1.5

The Programs shall be implemented in Software (Using MATLAB / Lab View / C Programming/ Equivalent) and Hardware (Using TI / Analog Devices / Motorola / Equivalent DSP processors).

Note: - Minimum of 12 experiments has to be conducted.

List of Experiments:

- 1. Generation of Sinusoidal Waveform / Signal based on Recursive Difference Equations
- 2. Histogram of White Gaussian Noise and Uniformly Distributed Noise.
- 3. To find DFT / IDFT of given DT Signal
- 4. To find Frequency Response of a given System given in Transfer Function/ Differential equation form.
- 5. Obtain Fourier series coefficients by formula and using FET and compare for half sine wave.
- 6. Implementation of FFT of given Sequence
- 7. Determination of Power Spectrum of a given Signal(s).
- 8. Implementation of LP FIR Filter for a given Sequence/Signal.
- 9. Implementation of HP IIR Filter for a given Sequence/Signal
- 10. Generation of Narrow Band Signal through Filtering
- 11. Generation of DTMF Signals
- 12. Implementation of Decimation Process
- 13. Implementation of Interpolation Process
- 14. Implementation of I/D Sampling Rate Converters
- 15. Impulse Response of First order and Second Order Systems.



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Website: https://siiet.ac.in/

Digital Signal Processing Lab

CO's, PO's, PSO's MAPPING

Class: III ECE- C

Course Outcomes

After completing this course, the student will be able to:
C 326.1 Apply knowledge of digital filter design for various applications.
C326.2. Analyze various signals in transform domain.
C326.3. Apply MultiMate concepts in different areas.
C326.4. Perform real time experiments on processors such as audio and speech processing.
C326.5. Work with MATLAB functions
C326.6. Enable students to analyze and design different signals & filters using MATLAB.

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO/														
CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C326.1	3	-	2	1	-	1	-	-	-	-	-	-	1	2
C326.2	2	3	-	2	-	-	-	-	-	-	-	-	1	3
C326.3	-	-	-	2	3	2	-	-	-	-	-	-	1	2
C326.4	-	3	-	1	2	-	-	-	-	-	-	1	1	3
C326.5	3	-	-	1	-	2	-	-	-	-	1	=	1	3
C326.6	-	3	-	2	2	-	1	-	-	-	-	=	1	2
C326	2.7	3	2	1.5	2.3	1.6	1				1	1	1	2.5



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Digital Signal Processing Lab

LIST OF EXPERIMENTS AND THEIR CO, PO/PSO MAPPING

S.No	Name of The Experiment	CO	PO	PSO
1	Generation of Sinusoidal Waveform /Signal based on Recursive Difference Equations	2,5	1,2,4,6,11	1,2
2	Histogram of White Gaussian Noise and Uniformly Distributed Noise.	4,5	1,2,4,5,6,11	1,2
3	To find DFT / IDFT of given DT Signal	2,5	1,2,4,6,11	1,2
4	To find Frequency Response of a given System given in Transfer Function/ Differential equation form.	2,5	1,2,4,6,11	1,2
5	Obtain Fourier series coefficients by formula and using FET and compare for half sine wave.	5,6	1,2,4,5,6,7,11	1,2
6	Implementation of FFT of given Sequence	5,6	1,2,4,5,6,7,11	1,2
7	Determination of Power Spectrum of a given Signal(s).	5,6	1,2,4,5,6,7,11	1,2
8	Implementation of LP FIR Filter for a given Sequence/Signal	1,6	1,2,3,4,5,6,7	1,2
9	Implementation of HP IIR Filter for a given Sequence/Signal	1,6	1,2,3,4,5,6,7	1,2
10	Generation of Narrow Band Signal through Filtering	1,5	1,3,4,6,11,	1,2
11	Generation of DTMF Signals	2,5	1,2,4,6,11	1,2
12	Implementation of Decimation Process.	3,4,5	1,2,4,5,6,7,11,12	1,2
13	Implementation of Interpolation Process	3,4,5	1,2,4,5,6,7,11,12	1,2
14	Implementation of I/D Sampling Rate Converters	3,4,5	1,2,4,5,6,7,11,12	1,2
15	Impulse Response of First order and Second Order Systems.	3,4,5	1,2,4,5,6,7,11,12	1,2



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING Class Timetable

CLASS: III-B.Tech ECE-C

A.Y:2022-23

SEMESTER: II

LH: C-203

TIME/	T	**						200
DAY	9:40-10:30	10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00- 1:30	V 1:30-2:20	VI 2:20.2:10	VII
MON	DSP	ESD	VLSID	A&P(T)/DSP(T)	1.50	1.50-2.20	2:20-3:10	3:10-4:00
TUE	A&P	IM	DSP				e-CAD LAB / DSF	LAB
WED	ESD	120000	THE COURT	VLSID	L	ESD	CO	-CU/DAA
		FAI	A&P	DSP(T)/VLSID(T)	U	DSP	IM	LID
THU	VLSID	ES	5	SL LAB	N	8-75		LIB
FRI	ES	A&P	ESD		C	A&P	ESD	COUN
SAT	VLSID	DSP		VLSID(T)/A&P(T)	H	FAI	IM	SPORTS
*(T)	- Tutorial Con		VLSIL	(ADJUNCT)			DSP LAB / e-CAD	

Course Name	Name of the Faculty	Course Code	Course	Name of the
A&P-Antennas and Propagation	Dr.K.Srinivasa Reddy	EC604PC	DSP LAB-Digital Signal Processing Lab	T.Naresh/ Dr.K.Srinivasa Reddy/K.Padma
Den pi i i i		EC605PC	e-CAD LAB-e - CAD Lab	G.Swathi/ B.Ashwini/A.Apsara
DSP-Digital Signal Processing	T.Naresh	EC606PC	SL LAB-Scripting Languages Lab	Ch.Prabhakar/B.Ashwini/K.Bha skar Reddy
VLSID-VLSI Design	G.Swathi	¥ .	FAI-Fundamentals of	K.Bhaskar Reddy
ESD-Embedded System		*MC609	ES-Environmental Science	K.Mounika
Design(Professional Elective-II)	K.Mallaiah	COUN		
VLSID(ADJUNCT)	G.Chandra	SPORTS	Sports	P.Srilatha/Y.Rajani
IM-Industrial Management	sekhar	LIB	Library	P.Srilatha/K.Padma
(Open Elective-I)	K.V.Nagamani	CO- CU/DAA	Co-Curricular/Dept.	M.Srilatha/P.Krishna Rao A.Sindhuja/G.Swathi/G.Anitha
	Name A&P-Antennas and Propagation DSP-Digital Signal Processing VLSID-VLSI Design ESD-Embedded System Design(Professional Elective-II) VLSID(ADJUNCT) IM-Industrial Management (Open Florible-II)	Name Faculty A&P-Antennas and Propagation Dr.K.Srinivasa Reddy DSP-Digital Signal Processing T.Naresh VLSID-VLSI Design ESD-Embedded System Design(Professional Elective-II) VLSID(ADJUNCT) G.Chandra sekhar IM-Industrial Management (Open Elective-I) K.V.Nagamani	Name Faculty Code Code A&P-Antennas and Propagation Dr.K.Srinivasa Reddy EC604PC EC605PC DSP-Digital Signal Processing T.Naresh EC606PC VLSID-VLSI Design G.Swathi *MC609 ESD-Embedded System Design(Professional Elective-II) VLSID(ADJUNCT) G.Chandra SPORTS Sekhar LIB IM-Industrial Management (Open Elective-I) K.V.Nagamani CO-	Name Faculty Code Name Faculty Dr.K.Srinivasa Reddy Dr.K.Srinivasa Reddy EC604PC EC605PC Code Name Dr.K.Srinivasa Processing Lab EC605PC Code Name DSP LAB-Digital Signal Processing Lab EC605PC Code Name COUN Code Name COUN Counseling VLSID(ADJUNCT) G.Chandra SPORTS Sports LIB Library

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DIGITAL SIGNAL PROCESSING LAB

LAB EXTERNAL EXAM QUESTION PAPER

1. Write a Matlab program for the Generation of Sinusoidal Waveform / Signal based on Recursive Difference Equations 2. Write a Matlab program for the Histogram of White Gaussian Noise and Uniformly Distributed Noise. 3. Write a Matlab program for the To find DFT / IDFT of given DT Signal 4. Write a Matlab program for finding the To find Frequency Response of a given System given in Transfer Function/ Differential equation form. 5. Write a Matlab program for finding Obtain Fourier series coefficients by formula and using FET and compare for half sine wave. 6. Write a Matlab program for the Implementation of FFT of given Sequence 7. Write a Matlab program for Determination of Power Spectrum of a given Signal(s). 8. Write a Matlab program for Implementation of LP FIR Filter for a given Sequence/Signal. 9. Write a Matlab program for the Implementation of HP IIR Filter for a given Sequence/Signal 10. Write a Matlab program for the Generation of Narrow Band Signal through Filtering 11. Write a Matlab program for Generation of DTMF Signals 12. Write a Matlab program for Implementation of Decimation Process 13. Write a Matlab program for Implementation of Interpolation Process 14. Write a Matlab program for Implementation of I/D Sampling Rate Converters

15. Write a Matlab program for Impulse Response of First order and Second Order Systems.



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III ECE Regular Lab External Exams Timetable

A.Y: 2022-23

SEM: II

S.No.	Name of the Lab	Year/ Sec	Date & Time of the Lab Exam	Name of the Lab Internal Examiners
		III ECE-A	03.07.2023(FN)	Mr.T.Naresh
1	Digital Signal Processing Lab	III ECE-B	04.07.2023(FN)	Mr.T.Naresh
	Lau	III ECE-C	05.07.2023(FN)	Mr.T.Naresh
	-	III ECE-A	04.07.2023(FN)	Mrs.S.Alekhya
2	e-CAD Lab	III ECE-B	05.07.2023(FN)	Mr.K.Srikanth
		III ECE-C	03.07.2023(FN)	Mrs.S.Alekhya
	Scripting	III ECE-A	05.07.2023(FN)	Mr.M.Sagar
3	Languages	III ECE-B	03.07.2023(FN)	Mr.K.Anup Kumar
	Lab	III ECE-C	04.07.2023(FN)	Mr.D.Nagaraju
4	Computer Vision Lab	III CSE(IOT)	03.07.2023(FN)	Mr.K.Srikanth
5	IoT Lab	III CSE(IOT)	04.07.2023(FN)	Mr.I.Venu

Timings: - FN: 10:00 AM To 01:00 PM

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R R Dist Telangane -501 510



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

III ECE Regular Lab External Examiners from GNITC

A.Y: 2022-23

SEM: II

S.No.	Name of the Lab	Year/ Sec	Date & Time of the Lab Exam	Name of the Lab Internal Examiners	Name of the Lab External Examiner & Contact Details
	1	III ECE-A	03.07.2023	Mr.T.Naresh	Mr.M. Ravinder Asst Prof 9491108268
,1	Digital Signal Processing	III ECE-B	04.07.2023	Mr.T.Naresh	Mr.D Naresh Asst Prof 9885248584
	Lab	III ECE-C	05.07.2023	Mr.T.Naresh	Dr.Md.Rashid Mahmood Prof 9999254431
		III ECE-A	04.07.2023	Mrs.S.Alekhya	Prof.A Mohan Prof 9989298588
2	e-CAD Lab	III ECE-B	05.07.2023	Mr.K.Srikanth	Dr. B. Mythily Devi Asst Prof 8985858946
		III ECE-C	03.07.2023	Mrs.S.Alekhya	Mr.ChNarasimhuli Asst Prof 9849825884
3	Computer Vision Lab	III CSE (IOT)	03.07.2023	Mr.K.Srikanth	Mr NVS. Murthy Asst Prof 9701196375
4	IoT Lab	III CSE (IOT)	04.07.2023	Mr.I.Venu	Mr D .Surendra Rao Assoc Prof 9849935889

HODE TO the Department

Electronic and Communication Engg. Depl

SRTINDU INSTITUTE OF ENGG & TECH

SHERMUND (V), Ibrahmpathann, M. K. K. Ulsi-201 210.

PRINCIPAL

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Digital Signal Processing Lab

LAB OCCUPANCY CHART

A.Y: 2022-23

Year/Semester: III/II

Lab No: C-002

Period/	1	2	3	4	01:00 -	5	6	7
Day	9:40-10:30	10:30-11:2	11:20 - 12:10	12:10 - 1:00	01:30	1:30-2:20	2:20-	3:10-4:00
Monday		D	SP Lab III ECE-	-A	L	DSP Lab III ECE-C		CE-C
Tuesday					U	DSP I	ab III E	ECE-B
Wednesday						МАП	NTANA	NCE
Thursday		N	MAINTANANC	Е	N	DSP L	ab III E	CE-A
Friday					C	DSP I	ab III E	ECE-B
Saturday		1			н	DSP I	ab III E	CE-C

S.No.	Class	Faculty In-charge	Supporting Faculty
1	DSP Lab III ECE-A	Mr.Y RAJU	Dr T Ramakrishna
2	DSP Lab III ECE-B	Ms.Apasara	Ms.M.Srilatha
3	DSP Lab III ECE-C	Mr.T Naresh	Dr K Srinivas Reddy

S.No.	Class	Lab In-charge	
1	DSP Lab II ECE-A, B&C	Mr.T Naresh	

Lab In-charge

Head of The Department

Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V), Ibrahimpatham(M), R.H.Disi-50. STU



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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

- All students must observe the dress code while in the laboratory
- Foods, drinks and smoking are **NOT** allowed
- All bags must be left at the indicated place.
- The lab time table must be strictly followed.
- Be **PUNCTUAL** for your laboratory session.
- Experiment must be completed within the given time.
- Noise must be kept to minimum.
- Workspace must be kept clean and tidy at all time.
- Handle all apparatus with care.
- All students are liable for any damage to equipment due to their own negligence.
- All equipment, apparatus, tools and components must be **RETURNED** to their original place after use.
- Students are strictly **PROHIBITED** from taking out any items from the laboratory.
- Report immediately to the lab supervisor if any injury occurred.
- Report immediately to the lab supervisor if any damages to equipment.

BEFORE LIVING LAB

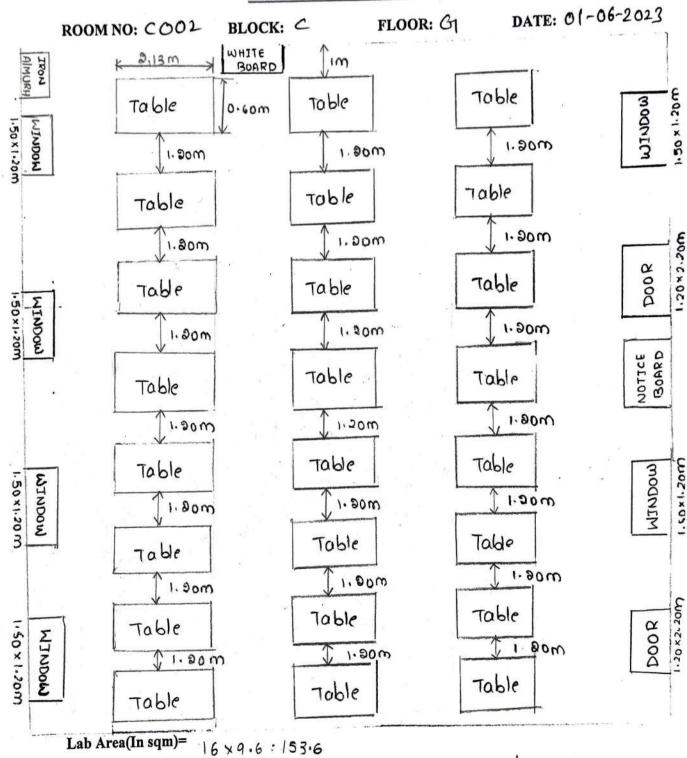
- Place the stools under the lab bench.
- Turn off the power to all instruments.
- Please check the laboratory notice board regularly for updates.



SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

DIGITAL SIGNAL PROCESSING LAB

PHYSICAL LAB FLOOR PLAN



Lab In-charge

Head of The Department

Flectronics and Communication Engg. Dept SRITHOU MEST CUTE OF ENGG 8 TECH. Sheriquia(V), Ibraninipananum, R.H.Dist on 5 m.



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LAB MANUAL LINK

https://drive.google.com/file/d/1s59o6bnXXBvh3hJ9wc6vqh-wW3hWzsW5/view?usp=sharing

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty: T NARESH 2022-23
Branch & Section: ECE - C I internal

Course Name: DSP LAB Year/Semester: III/II

S.No	HT No.	A+A+CD+MG	T+P+C+R	DDE
Max. Max	arks ==>	5	5	15
1	21X35A0401	4	4	12
2	21X35A0402	4	3	12
3	21X35A0403	5	4	13
4	21X35A0404	5	4	13
5	21X35A0405	5	4	14
6	21X35A0406	4	4	13
7	21X35A0407	4	5	15
8	21X35A0408	4	4	13
9	21X35A0409	4	5	14
10	21X35A0410	0	0	14
11	21X35A0411	4	4	13
12	21X35A0413	4	5	14
13	21X35A0414	4	5	14
14	21X35A0415	4	3	12
15	21X35A0416	4	3	12
16	21X35A0417	4	4	14
17	21X35A0418	5	4	14
18	21X35A0419	3	3	11
19	21X35A0420	4	4	13
20	21X35A0421	3	4	12
21	21X35A0422	4	4	13
22	21X35A0423	4	4	13
23	21X35A0424	3	4	12
24	21X35A0425	4	3	12
25	21X35A0426	4	4	12
26	21X35A0427	4	4	14
27	21X35A0428	3	4	12
28	21X35A0429	4	3	12
29	21X35A0430	4	4	14
30	21X35A0431	4	5	14
31	21X35A0432	4	3	12
32	21X35A0433	4	4	14
33	21X35A0434	3	3	11
Target se	et by the faculty /	3.00	3.00	9.00
Number performe	of students ed above the target	32	32	33
Number attempte	of students d	33	33	33

Percentage of students	97%	97%	100%
scored more than target	2170	2170	10070

CO Mapping with Exam Questions:

CO - 1	y	y	у
CO - 2	y	y	у
CO - 3	y	y	у
CO - 4	y	y	у
CO - 5	y	y	у
CO - 6	y	y	y

CO Attainment based on Exam Questions:

CO - 1	97%	97%	100%
CO - 2	97%	97%	100%
CO - 3	97%	97%	100%
CO - 4	97%	97%	100%
CO - 5	97%	97%	100%
CO - 6	97%	97%	100%

СО	Intrnal practica	DDE	OveralI	Level
CO-1	97%	100%	98%	3
CO-2	97%	100%	98%	3
CO-3	97%	100%	98%	3
CO-4	97%	100%	98%	3
CO-5	97%	100%	98%	3
CO-6	97%	100%	98%	3

Attainment Level			
1	60%		
2	70%		
3	>80%		

3

Attainment (Internal 1 Examination) =

Note:

A+A+CD+MG: AIM+APPARATUS+CIRCUIT DIAGRAM+MODEL GRAPH

 $T+P+C+R\ :\ THEORY+PROCEDURE+CALCULATION+RESULT$

DDE: Day to Day Evaluation

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty: T NARESH 2022-23
Branch & Section: ECE - C II internal

Course Name: DSP LAB Year/Semester: III/II

S.No	HT No.	A+A+CD+MG	T+P+C+R	DDE
Max. Ma	arks ==>	5	5	15
1	21X35A0401	4	4	12
2	21X35A0402	4	3	12
3	21X35A0403	5	4	13
4	21X35A0404	5	4	13
5	21X35A0405	5	4	14
6	21X35A0406	4	4	13
7	21X35A0407	4	5	15
8	21X35A0408	4	4	13
9	21X35A0409	4	5	14
10	21X35A0410	0	0	14
11	21X35A0411	4	4	13
12	21X35A0413	4	5	14
13	21X35A0414	4	5	14
14	21X35A0415	4	3	12
15	21X35A0416	4	3	12
16	21X35A0417	4	4	14
17	21X35A0418	5	4	14
18	21X35A0419	3	3	11
19	21X35A0420	4	4	13
20	21X35A0421	3	4	12
21	21X35A0422	4	4	13
22	21X35A0423	4	4	13
23	21X35A0424	3	4	12
24	21X35A0425	4	3	12
25	21X35A0426	4	4	12
26	21X35A0427	4	4	14
27	21X35A0428	3	4	12
28	21X35A0429	4	3	12
29	21X35A0430	4	4	14
30	21X35A0431	4	5	14
31	21X35A0432	4	3	12
32	21X35A0433	4	4	14
33	21X35A0434	3	3	11
Target set by the faculty / HoD		3.00	3.00	9.00
Number of students performed above the target		32	32	33
	of students	33	33	33

Percentage of students scored more than target	97%	97%	100%
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CO Mapping with Exam Questions:

CO - 1	y	y	у
CO - 2	y	y	у
CO - 3	y	y	у
CO - 4	y	y	у
CO - 5	y	y	у
CO - 6	y	y	y

CO Attainment based on Exam Questions:

CO - 1	97%	97%	100%
CO - 2	97%	97%	100%
CO - 3	97%	97%	100%
CO - 4	97%	97%	100%
CO - 5	97%	97%	100%
CO - 6	97%	97%	100%

СО	Intrnal practica	DDE	OveralI	Level
CO-1	97%	100%	98%	3
CO-2	97%	100%	98%	3
CO-3	97%	100%	98%	3
CO-4	97%	100%	98%	3
CO-5	97%	100%	98%	3
CO-6	97%	100%	98%	3

Attainment Level								
1	60%							
2	70%							
3	>80%							

3

Attainment (Internal 1 Examination) =

Note:

A+A+CD+MG: AIM+APPARATUS+CIRCUIT DIAGRAM+MODEL GRAPH

 $T+P+C+R\ :\ THEORY+PROCEDURE+CALCULATION+RESULT$

DDE: Day to Day Evaluation



Department of Electronics and Communication Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty: T NARESH Academic Year: 2022-2023

Branch & Section: ECE-C Year / Semester: III/II

Course Name: DSP LAB

	Tvallic.	DSI L/ID
S.No	Roll Number	Marks Secured
1	21X35A0401	66
2	21X35A0402	64
3	21X35A0403	69
4	21X35A0404	69
5	21X35A0405	68
6	21X35A0406	65
7	21X35A0407	71
8	21X35A0408	67
9	21X35A0409	69
10	21X35A0410	56
11	21X35A0411	63
12	21X35A0413	68
13	21X35A0414	72
14	21X35A0415	57
15	21X35A0416	58
16	21X35A0417	67
17	21X35A0418	72
18	21X35A0419	56
19	21X35A0420	63
20	21X35A0421	71
21	21X35A0422	65
22	21X35A0423	71
23	21X35A0424	61
24	21X35A0425	57
25	21X35A0426	71
26	21X35A0427	70
27	21X35A0428	58
28	21X35A0429	61
29	21X35A0430	64
30	21X35A0431	72
31	21X35A0432	59
32	21X35A0433	57
33	21X35A0434	55
Max Ma	arks	75
~1 ·		

Class Average mark	60
Number of students performed above the target	24
Number of successful students	33
Percentage of students scored more than target	73%
Attainment level	3

Attainment Level	% students
1	60%
2	70%
3	>80%

Department of Electronics and Communication Engineering

Course Outcome Attainment

Name of the faculty: T NARESH Academic Year: 2022-2023

Branch & Section: ECE-C

Course Name: DSP LAB Year: Ш II Semester:

	1st					
Course Outcomes	Course Outcomes Internal 2nd Internal Exam Exam		Internal Exam	University Exam	Attainment Level	
CO1	3.00 3.00		3.00	3.00	3.00	
CO2	3.00	3.00	3.00	3.00	3.00	
CO3	CO3 3.00 3.00		3.00	3.00	3.00	
CO4	3.00 3.00		3.00	3.00	3.00	
CO5	3.00 3.00		3.00	3.00	3.00	
CO6	CO6 3.00 3.00		3.00	3.00	3.00	
Inter	nal & Unive	ersity Attainment:	3.00	3.00		
		Weightage	70%	30%		
CO Attainment for th	e course (In	ternal, University)	2.10	0.90]	
CO Attainment for	the course ((Direct Method)		3.00]	

Overall course attainment level

3.00

Department of Electronics and Communication Engineering

Program Outcome Attainment (from Course)

Name of Faculty: T NARESH Academic Year: 2022-2023

Branch & Section: ECE-C Year: III
Course Name: DSP LAB Semester: II

CO-PO mapping

	- I- I-	<u> </u>												
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3		2	1		1							1	2
CO2	2	3		2									1	3
CO3				1	3	2							1	2
CO4		3		2	2	-						1	1	3
CO5	3			1	-	2					1		1	3
CO6		3		2	2	-	1						1	2
Course	2.67	3.00	2.00	1.50	2.33	1.67	1.00				1.00	1.00	1.00	2.50

со	Course Outcome Attainment	
	3.00	
CO1		
	3.00	
CO2		
	3.00	
CO3		
	3.00	
CO4		
	3.00	
CO5		
CO6	3.00	
Overall course a	tainment level 3.00	

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
со														
Attainme														
nt	2.67	3.00	2.00	1.50	2.33	1.67	1.00				1.00	1.00	1.00	2.50

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)