Sri Indu Institute of Engineering & Technology

Recognized Under 2(f) of UGC Act 1956
Approved by AICTE, New Delhi
Affiliated to JNTUH, Hyderabad.

COURSE FILE

ON

DIGITAL SYSTEM DESIGN

Course Code – EC303PC

II B.Tech I-SEMESTER

A.Y.: 2022-2023

Prepared by

Mrs. G.Anusha
Assistant Professor

Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year	2022-2023
Course Title	DIGITAL SYSTEM DESIGN
Course Code	EC303PC
Programme	B.Tech
Year & Semester	II year I-semester
Branch & Section	ECE-A
Regulation	R18
Course Faculty	Mrs. G.Anusha, Assistant Professor

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INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To Continuous assess of teaching-learning process through institute-industry collaboration.

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.

IM4: To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

DM1: To facilitate an academic environment that enables student's centric learning.

DM2: To provide state-of-the-art hardware and software technologies to meet industry requirements.

DM3: To continuously update the Academic and Research infrastructure.

DM4: To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

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PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

PEO1: Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.

PEO2: Graduates with ability to execute innovative ideas for Research and Development with continuous learning.

PEO3: Graduates inculcated with industry based soft-skills to enable employability.

PEO4: Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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PROGRAM OUTCOMES

1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

6. **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY
HYDERABADB.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING COURSE STRUCTURE & SYLLABUS (R18)
Applicable From 2018-19 Admitted Batch

II YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC301PC	Electronic Devices and Circuits	3	1	0	4
2	EC302PC	Network Analysis and Transmission Lines	3	0	0	3
3	EC303PC	Digital System Design	3	1	0	4
4	EC304PC	Signals and Systems	3	1	0	4
5	EC305ES	Probability Theory and Stochastic Processes	3	0	0	3
6	EC306PC	Electronic Devices and Circuits Lab	0	0	2	1
7	EC307PC	Digital System Design Lab	0	0	2	1
8	EC308ES	Basic Simulation Lab	0	0	2	1
9	*MC309	Constitution of India	3	0	0	0
		Total Credits	**18**	**3**	**6**	**21**

II YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	MA401BS	Laplace Transforms, Numerical Methods & Complex Variables	3	1	0	4
2	EC402PC	Electromagnetic Fields and Waves	3	0	0	3
3	EC403PC	Analog and Digital Communications	3	1	0	4
4	EC404PC	Linear IC Applications	3	0	0	3
5	EC405PC	Electronic Circuit Analysis	3	0	0	3
6	EC406PC	Analog and Digital Communications Lab	0	0	3	1.5
7	EC407PC	IC Applications Lab	0	0	3	1.5
8	EC408PC	Electronic Circuit Analysis Lab	0	0	2	1
9	*MC409	Gender Sensitization Lab	0	0	2	0
		Total Credits	**15**	**2**	**10**	**21**

***MC – Satisfactory/Unsatisfactory**

EC303PC: DIGITAL SYSTEM DESIGN

B.Tech. II Year I Sem. L T P C

3 1 0 4

Pre-Requisites: Nil

Course Objectives:

- To understand common forms of number representation in logic circuits
- To learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
- To understand the concepts of combinational logic circuits and sequential circuits.
- To understand the Realization of Logic Gates Using Diodes & Transistors.

Course Outcomes: Upon completing this course, the student will be able to

- Understand the numerical information in different forms and Boolean Algebra theorems
- Postulates of Boolean algebra and to minimize combinational functions
- Design and analyze combinational and sequential circuits
- Known about the logic families and realization of logic gates.

UNIT - I:

Number Systems: Number systems, Complements of Numbers, Codes- Weighted and Non-weighted codes and its Properties, Parity check code and Hamming code.

Boolean Algebra: Basic Theorems and Properties, Switching Functions- Canonical and Standard Form, Algebraic Simplification, Digital Logic Gates, EX-OR gates, Universal Gates, Multilevel NAND/NOR realizations.

UNIT - II:

Minimization of Boolean functions: Karnaugh Map Method - Up to five Variables, Don't Care Map Entries, Tabular Method,

Combinational Logic Circuits: Adders, Subtractors, Comparators, Multiplexers, Demultiplexers, Encoders, Decoders and Code converters, Hazards and Hazard Free Relations.

UNIT - III

Sequential Circuits Fundamentals: Basic Architectural Distinctions between Combinational and Sequential circuits, SR Latch, Flip Flops: SR, JK, JK Master Slave, D and T Type Flip Flops, Excitation Table of all Flip Flops, Timing and Triggering Consideration, Conversion from one type of Flip-Flop to another.

Registers and Counters: Shift Registers – Left, Right and Bidirectional Shift Registers, Applications of Shift Registers - Design and Operation of Ring and Twisted Ring Counter, Operation of Asynchronous and Synchronous Counters.

UNIT - IV

Sequential Machines: Finite State Machines, Synthesis of Synchronous Sequential Circuits- Serial Binary Adder, Sequence Detector, Parity-bit Generator, Synchronous Modulo N –Counters. Finite state machine-capabilities and limitations, Mealy and Moore models.

UNIT - V

Realization of Logic Gates Using Diodes & Transistors: AND, OR and NOT Gates using Diodes and Transistors, DCTL, RTL, DTL, TTL, CML and CMOS Logic Families and its Comparison, Classification of Integrated circuits, comparison of various logic families, standard TTL NAND Gate- Analysis & characteristics, TTL open collector O/Ps, Tristate TTL, MOS & CMOS open drain and tristate outputs, CMOS transmission gate, IC interfacing- TTL driving CMOS & CMOS driving TTL.

TEXT BOOKS:

1. Switching and Finite Automata Theory - Zvi Kohavi & Niraj K. Jha, 3rd Edition, Cambridge, 2010.
2. Modern Digital Electronics – R. P. Jain, 3rd Edition, 2007- Tata McGraw-Hill

REFERENCE BOOKS:

1. Digital Design- Morris Mano, PHI, 4th Edition,2006

COURSE : Digital System Design(C213) **CLASS:**II-ECE A&B

Course Outcomes:

After completing this course the student will be able to:

C213.1:State the Boolean algebra, different number systems and codes. (Knowledge)

Change one number system into another number system.(Application)

C213.2: Design the different combinational logic circuits.(Synthesis)

Modify and transform one form of Boolean equation to another form and simplify the Boolean equation in K-Map.(Application, Comprehension)

C213.3:Design the different Sequential circuits.(Synthesis)

Analyze and compare the flipflops and transform one flipflop to another flipflop. (Analysis, Evaluation)

C213.4: Design synchronous and asynchronous counters.(Synthesis)

Analyze and differentiate the sequential machine.(Analysis)

C213.5:Define, Differentiate between logic families and realization of logic gates using diodes and transistors. (Knowledge, Analysis)

C213.6: Design the digital system.(Synthesis)

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C213.1	3	2	-	-	-	-	-	-	-	-	-	-	2	3
C213.2	3	3	3	-	-	-	-	-	-	-	2	3	3	3
C213.3	3	2	3	-	-	-	-	-	-	-	-	-	2	3
C213.4	3	1	3	-	-	-	-	-	-	-	3	-	3	3
C213.5	3	-	3	-	-	-	-	-	-	-	-	2	3	3
C213.6	2	-	3	-	-	-	-	-	-	-	-	-	3	3
AVG	**3.00**	**2.00**	**3.00**								**2.5**	**2.5**	**3**	**3**

CO-PO mapping Justification CO-PSO Mapping Justification

PO1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments

PO12 **LIFE-LONG LEARNING:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

PSO1 **Design Skills:** Design, analysis and development a economical system in the area of Embedded system & VLSI design

PSO2 **Software Usage:** Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx

C213.1: State the Boolean algebra, different number systems and codes. (Knowledge)

Change one number system into another number system.(Application)

	Justification
PO1	Students get the knowledge of Boolean algebra, different number systems, codes and different logic gates. (level-3)
PO2	Students solve problems on number system, conversion of SOP&POS forms and Multilevel NAND/NOR Realizations. (level-2)
PSO1	Moderate Students able to design, analysis and develop a economical system in the area of Embedded system & VLSI design (level-2)
PSO2	Moderate Students will able to investigate and solve the engineering problems using MATLAB, Keil,e-CAD and Xilinx. (level-3)

C213.2: Design the different combinational logic circuits.(Synthesis)

Modify and transform one form of Boolean equation to another form and simplify the Boolean equation in Karnaugh Map.(Application, Comprehension)

	Justification
PO1	Students get the knowledge on Combinational circuits and Karnaugh map(level-3)
PO2	Students solve problems on Karnaugh map and Tabular Method.(level-2)
PO3	Students able to design Adders,Comparators and Encoders. (level-2)
PO11	Students are able to solve the complex problems and design the circuits(level-3)
PO12	Students are able to design and modify different combinational circuit's with the chage with a broadcast context of technological change.(level-2)
PSO1	Students gain knowledge of digital logic design, circuit analysis, and hardware description languages (HDLs) like Verilog or VHDL (level-2)
PSO2	Absolutely, becoming proficient in MATLAB, Keil, e-CAD, and Xilinx tools can equip students to investigate and solve engineering problems effectively(level-3)

C213.3:Design the different Sequential circuits.(Synthesis)

Analyze and compare the flipflops and transform one flipflop to another flipflop. (Analysis, Evaluation)

	Justification
PO1	Students get the knowledge on Flipflops, Registers and Counters.(level-3)
PO2	Students solve problems on .(level-2)
PO3	Students able to design Adders,Comparators and Encoders. (level-3)
PSO1	Learn about logic gates, flip-flops, sequential circuits, and combinational circuits. (level-2)
PSO2	Get hands-on experience with tools like Cadence, Synopsys, or Xilinx for design, simulation, and synthesis. (level-3)

C213.4: Design synchronous and asynchronous counters.(Synthesis)

Analyze and differentiate the sequential machine.(Analysis)

	Justification
PO1	Students get the knowledge on State diagram,Parity-bit generator and FSM.(level-3)
PO2	Students solve problems on Sequence Detector.(level-3)
PO3	Students able to design Synchronous Sequential circuits,Synchronous and Asychronous counters. (level-2)
PO11	Utilize engineering knowledge to guide decision-making, problem-solving, and innovation within the project (level-2)
PSO1	Familiarize yourself with Xilinx design tools like Vivado or ISE for FPGA design and implementation(level-2)
PSO2	Learn how to integrate these tools in a cohesive workflow for tackling complex engineering challenges (level-3)

C213.5: Define and Differentiate between logic families and realization of logic gates using diodes and transistors.(Knowledge, Analysis)

	Justification
PO1	Students get the knowledge on logic families.(level-3)
PO3	Moderate students will learn and implement the realization of different logic gates(level-3)
PO12	Apply newly acquired knowledge and skills to practical projects or real-world scenarios. (level-2)
PSO1	Implement the design through synthesis tools and place & route algorithms considering area, power, and performance constraints. (level-3)
PSO2	Practice implementing designs onto Xilinx FPGAs, including synthesis, place and route, and verification (level-3)

C213.6: Design the digital system.(Synthesis)

	Justification
PO1	Students get the knowledge on Logic gates,Boolean Algebra,K-Map,Combinational and Sequential circuits.(level-2)
PO3	Students able to analyse and design complex engineering problems by applying the principles of mathamatics and natural Sciences.(level-3)
PSO1	Create the Register-Transfer Level (RTL) design using HDLs (Verilog or VHDL) for logic synthesis. (level-3)
PSO2	Integrate necessary sensors, actuators, and communication interfaces considering cost-effectiveness and functionality. (level-3)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

ACADEMIC CALENDAR 2022-23

B.Tech./B.Pharm. II YEAR I & II SEMESTERS

I SEM

S. No	Description	Duration	
		From	To
1	Commencement of I Semester classwork	**28.11.2022**	
2	1st Spell of Instructions	28.11.2022	21.01.2023 (8 Weeks)
3	First Mid Term Examinations	23.01.2023	30.01.2023 (1 Week)
4	Submission of First Mid Term Exam Marks to the University on or before	04.02.2023	
5	2nd Spell of Instructions	31.01.2023	29.03.2023 (8 Weeks)
6	Second Mid Term Examinations	31.03.2023	08.04.2023 (1 Week)
7	Preparation Holidays and Practical Examinations	10.04.2023	15.04.2023 (1 Week)
8	Submission of Second Mid Term Exam Marks to the University on or before	15.04.2023	
9	End Semester Examinations	17.04.2023	29.04.2023 (2 Weeks)

Note: No. of Working / Instructional Days: 93

II SEM

S. No	Description	Duration	
		From	To
1	Commencement of II Semester classwork	**01.05.2023**	
2	1st Spell of Instructions (including Summer Vacation)	01.05.2023	08.07.2023 (10 Weeks)
3	**Summer Vacation**	15.05.2023	27.05.2023 (2 Weeks)
4	First Mid Term Examinations	10.07.2023	15.07.2023 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	22.07.2023	
6	2nd Spell of Instructions	18.07.2023	11.09.2023 (8 Weeks)
7	Second Mid Term Examinations	12.09.2023	16.09.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	19.09.2023	23.09.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	23.09.2023	
10	End Semester Examinations	25.09.2023	07.10.2023 (2 Weeks)

Note: No. of Working / Instructional Days: 92

Sd./-xxxx
REGISTRAR

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC)
Accredited by NAAC A+ Grade, Recognized under 2(f) of UGC Act 1956.
(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana – 501 510
https://siiet.ac.in/

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Class Timetable

CLASS: II-B.Tech ECE-A **A.Y:2022-23** **SEMESTER: I** **LH: C-101**

TIME/ DAY	I 9:40-10:30	II 10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00-1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON	EDC	COI	EDC LAB / DSD LAB		LUNCH	DSD	NATL	SPORTS
TUE	PTSP	NATL	DSD	COI		EDC	SS	DSD(T)/SS(T)
WED	SS	PTSP	DSD LAB / BS LAB			DSD	SS(T)/EDC(T)	EDC
THU	NATL	PTSP	COI	EDC(T)/DSD(T)		SS	DSD	COUN
FRI	SS	EDC	COI	PTSP		LIB	CO-CU/DAA	
SAT	EDC	DSD	SS	NATL		PTSP	BS LAB / EDC LAB	

*(T) – Tutorial Concern Faculty

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the Faculty
EC301PC	EDC-Electronic Devices and Circuits	K.Rajender	EC306PC	**EDC LAB** - Electronic Devices and Circuits Lab	K.Rajender/B.Ashwini/M.Srilatha
EC302PC	NATL-Network Analysis and Transmission Lines	M.Nagaraju	EC307PC	**DSD LAB** - Digital System Design Lab	G.Anusha/T.Divya/P.Krishna Rao
EC303PC	DSD-Digital System Design	G.Anusha	EC308ES	**BS LAB** - Basic Simulation Lab	P.Rajendra/T.Naresh
EC304PC	SS-Signals and Systems	P.Rajendra	LIB	Library	B.Ashwini/Dr.K.Srinivasa Reddy
EC305ES	PTSP-Probability Theory and Stochastic Processes	T.Naresh	COUN	Counseling	K.Rajender/G.Anusha/G.Anitha
*MC309	COI-Constitution of India	S.Swapna	CO-CU/DAA	Co-Curricular/Dept.Assc.Act.	K.Rajender/T.Naresh/D.Aruna
			SPORTS	Sports	G.Anitha/P.Sumana

Class Incharge

Head of The Department

PRINCIPAL
Principal
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana -501 510

LESSON PLAN

Programme: B.Tech	Academic Year: 2022-23
Year: II	Semester: I
Course Title: Digital System Design	Course Code: EC303PC
Name of Faculty: G.Anusha	Number of lectures per week: 3

Unit-I Syllabus

Number Systems: Number systems, Complements of Numbers, Codes- Weighted and Non-weighted codes and its Properties, Parity check code and Hamming code.
Boolean Algebra: Basic Theorems and Properties, Switching Functions- Canonical and Standard form, Algebraic Simplification, Digital Logic Gates, EX-OR gates, Universal Gates, Multilevel NAND/NOR realizations

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
2	Review of Numbers Systems	T2, R 1	BB
1	Complements of Numbers	T2, R 1	BB
1	Binary Codes	T2, R 1	BB
2	Binary Coded Decimal Code and its Properties	T2, R 2	BB
1	Unit Distance Codes	T2, R 2	BB
1	Error Detecting And Correcting Codes	T1, R2	BB
2	Basic Theoram And Properties	T1, R2	BB
1	Switching Functions	T1	BB
1	Canonical and Standard Form	T1, R1	BB
1	Problem on Hamming Codes and minimization of Switching functions	T1, R1	BB
1	Digital Logic gates	T1	BB
1	Properties of XOR Gates	T1	BB
1	Universal Gates	T1, R2	BB
2	Multilevel NAND/NOR Realizations	T1, R2	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Student able to State the Boolean algebra different number systems and codes, Change one number system into another number system.			

*Session Duration: 50 minutes

*Total Number of Hours/Unit: 18

Unit-II Syllabus

Minimization of Boolean functions: Karnaugh Map Method - Up to five Variables, Don't Care Map Entries, Tabular Method,
Combinational Logic Circuits: Adders, Subtractors, Comparators, Multiplexers, Demultiplexers,Encoders, Decoders and Code converters, Hazards and Hazard Free Relations..

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Introduction, The Minimization of Switching function using Theoram	T1, R 2	BB
2	The Karnaugh Map Method-Up to Five Variable Maps	T2,R 2	BB
1	Don't care Map Entries	T2,R 2	BB
1	Tabular Method	T2,R 1	BB
1	Design of Combinational Logic :Adders	T2	BB
1	Subtractors ,Comparators	T2,R1	BB
1	Multiplexers,Demultiplexers	T2,R2	BB
1	Decoders ,Encoders	T1	BB
1	Code Converters	T2	BB
1	Problems on K-Map,Tabular method and design of combinational Circuits	T1, R 2	BB
2	Root Locus Technique – The Root Locus Concept, Definition Construction of Root Loci – Rules,	T2, R 1	BB
1	Hazards and Hazards Free Relations	T2, R 1	BB
Gap beyond syllabus (if any):			
Gap within the syllabus (if any)			
Course Outcome 1: Student able to design the different combinational logic circuits,Modify and transform one form of Boolean equation to another form and we can simplify the Boolean equation in K-Map.			

*Session Duration: 50 minutes

*Total Number of Hours/Unit: 14

Unit-III Syllabus

Sequential Circuits Fundamentals: Basic Architectural Distinctions between Combinational and Sequential circuits, SR Latch, Flip Flops: SR, JK, JK Master Slave, D and T Type Flip Flops, Excitation Table of all Flip Flops, Timing and Triggering Consideration, Conversion from one type of Flip-Flop to another.
Registers and Counters: Shift Registers – Left, Right and Bidirectional Shift Registers, Applications of Shift Registers - Design and Operation of Ring and Twisted Ring Counter, Operation of Asynchronous and Synchronous Counters

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Basic Architectural Distinctions between Combinational and Sequential Circuits	T1,R1	BB
2	Latches and Flipflops	T1	BB
1	SR,JK,Race Around Conditions in JK	T1, R 1	BB
1	JK Master Slave	T1, R 1	BB
1	D and T Type Flipflops	T1, R 1	BB
2	Excitation Table of all Flip Flops	T1, R 2	BB
1	Design of a Clocked Flip-Flop	T1, R 1	BB
1	Timing and Triggering Consideration	T1, R2	BB
1	Conversation from one type of Flip-Flop to another	R1	BB
1	Shift Registers,Data Transmission in Shift Registers	T2,R2	BB
1	Operation of Shift Registers and its applications	T2	BB
1	Design and Operation of Ring Counter	R1	BB
1	Applications of Shift Registers	T1,R2	BB
1	Twisted Ring Counter	T1	BB
2	Operations of Asynchronous And Synchronous Counters	T1	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Student able to design the different Sequential Circuits.Analyse and compare the flipflops and transform one flipflop to another flipflop**.**			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 18

Unit-IV Syllabus

Sequential Machines: Finite State Machines, Synthesis of Synchronous Sequential Circuits-Serial Binary Adder, Sequence Detector, Parity-bit Generator, Synchronous Modulo N – Counters. Finite state machine-capabilities and limitations, Mealy and Moore models.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Introduction to finite state machines	R1	BB
2	Synthesis of Synchronous Sequential Circuits	R2	PPT
1	Serial Binary Adder	R1	PPT
1	Sequence Detector	R1	PPT
1	Parity Bit Generator	R1	BB
1	Design of Synchronous Modulo N-Counters	R1	BB
1	Capabilities and Limitations of Finite State Machines	R1	BB
2	Mealy and Moore Models	R1	PPT
1	Lag Controller Design in Frequency Domain – Procedures, Problems	R1	BB
1	Lead Controller Design in Frequency Domain – Procedure, Problems	R1	BB
1	Lead-Lag Controller Design in Frequency Domain – Procedure, Problems	R1	BB
1	Analog and digital implementation of controllers	R1	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Students able to design synchronous and asynchronous counters. Analyze and differentiate the sequential machines.			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 14

Unit-V Syllabus

Realization of Logic Gates Using Diodes & Transistors: AND, OR and NOT Gates using Diodes and Transistors, DCTL, RTL, DTL, TTL, CML and CMOS Logic Families and its Comparison,Classification of Integrated circuits, comparison of various logic families, standard TTL NAND Gate-Analysis & characteristics, TTL open collector O/Ps, Tristate TTL, MOS & CMOS open drain and tristate outputs, CMOS transmission gate, IC interfacing- TTL driving CMOS & CMOS driving TTL.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
2	Realization of logic gates using Diodes and Transistors	R1,T1	BB
2	Explain about Logic Families:DCTL,RTL,DTL,TTL,CML and CMOS	R1	BB
1	Comparison of various logic families	R1	BB
1	Clasification of Integrated Circuits	R1	BB
2	TTL NAND Gate-Analysis & characteristics	R1	BB
2	TTL open collector O/Ps,Tristate outputs	R1	BB
2	MOS & CMOS open drain and tristate outputs	R1	BB
1	CMOS Transmission gate	R1	BB
2	IC Interfacing -TTL driving CMOS & CMOS driving TTL	R1	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Student able to get knowledge on logic families and realization of basic gates using diodes and transistors.			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 14

TEXT BOOKS:
T1. Switching and Fininte Automata Theory-Zvi Kohavi & Niraj K.Jha,3rd Edition,Cambridge.
T2: Modern Digital Electronics – R. P. Jain, 3rd Edition, 2007- Tata McGraw-Hill

REFERENCE BOOKS:
R1. Switching Theory and Logic Design – A Anand Kumar,3rd Edition ,PHI,2013

R2. Digital Design -Morris Mano,4th Edition ,Pearson.

WEB REFERENCES:

W1. https://ecm2d.weebly.com/uploads/2/2/4/1/22419142/chapter-1.pdf

W2. https://www.tutorialspoint.com/5-variable-k-map-in-digital-electronics

W3. https://unacademy.com/content/gate-cse-it/difference-between-combinational-and-sequential-circuit/

W4. https://www.javatpoint.com/finite-state-machine

W5. https://www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956
(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

Lecture notes

Unit 1 link:

https://drive.google.com/file/d/1z3J0CK8RpAMpuHVD47IeW3fSb4f9TcVe/view?usp=drive_link

Unit 2 link: https://drive.google.com/file/d/1K-ZUp5XuxZPpqRWg-nLUi8hgP6VXPK5r/view?usp=sharing

Unit 3 link:

https://drive.google.com/file/d/1z3J0CK8RpAMpuHVD47IeW3fSb4f9TcVe/view?usp=drive_link

Unit 4 link:

https://drive.google.com/file/d/1z3J0CK8RpAMpuHVD47IeW3fSb4f9TcVe/view?usp=drive_link

Unit 5 link:
https://drive.google.com/file/d/1pxIdlsQO8HEzOTtKieN_OAL7FdpOwXGH/view?usp=sharing

Power point presentation

PPT link:

https://drive.google.com/file/d/1pPMVZ7BgKy2y3hwMARyPQ8u6C3TGkdP9/view?usp=sharing

Code No: 153AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, April/May - 2023
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	Given that $(292)_{10} = (1204)_b$, determine the value of b.	[2]
b)	Write short notes on weighted binary codes.	[3]
c)	What is the difference between Decoder and Demultiplexer?	[2]
d)	Define a combinational logic circuit and give some examples.	[3]
e)	What is a Flip-Flop? What is the difference between Flip Flop and Latch	[2]
f)	Give the excitation table and characteristic equations of SR and JK Flip Flops	[3]
g)	What is Meely and Moore models?	[2]
h)	What are Finite State Machines and what are their limitations?	[3]
i)	Draw the circuit diagram of OR gates using discrete components.	[2]
j)	State advantages and disadvantages of TTL.	[3]

PART – B

(50 Marks)

2.a) Perform the following using BCD arithmetic.
i) $(79)_{10} + (177)_{10}$ ii) $(481)_{10} + (178)_{10}$
b) Obtain the Dual and complement to the following Boolean expressions [4+6]
i) $F = AB + A(B + C) + \bar{B}(B + D)$ ii) $F = A + B + A\bar{B}C$

OR

3.a) Place the following equations into proper canonical form.
i) $F(A, B, C) = A\bar{B} + AC + BC$ ii) $F(A, B, C, D) = (A + \bar{B})(A + \bar{B} + D)$
b) State and prove consensus theorem. [6+4]

4.a) Simplify F(A,B,C,D) = ∑ (4,5,6,7,12,13,14) +d(1,9,11,15) using K-map
b) With a neat design procedure, explain the implementation of a 4-bit Magnitude Comparator. [5+5]

OR

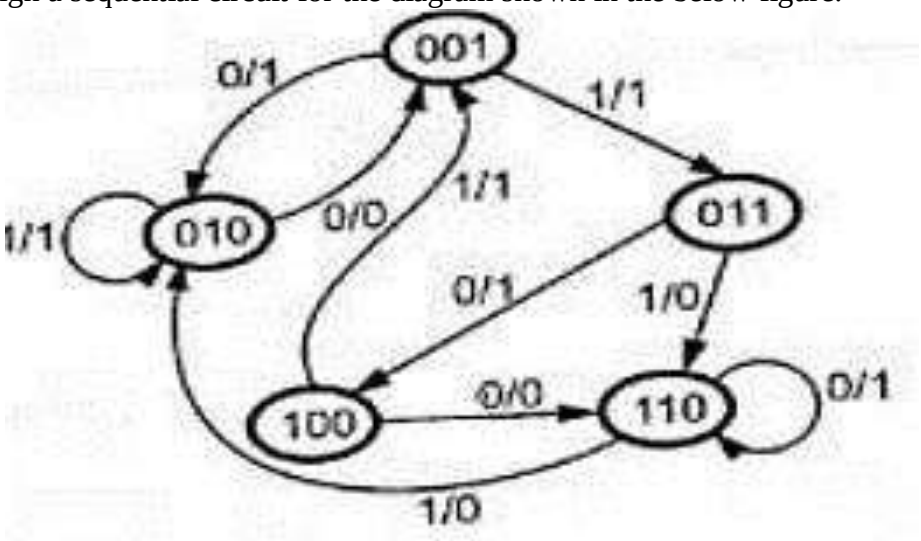
5.a) What is Encoder? Design an octal to binary Encoder.
b) Reduce the expression using Quine McCluskey's method F(x1, x2, x3, x4, x5) = ∑m (0, 2, 4, 5, 6, 7, 8, 10, 14, 17, 18, 21, 29, 31) + ∑d (11, 20, 22). [5+5]

6.a) With a neat diagram, explain the operation of bidirectional shift register.
b) Describe the conversion of SR-FlipFlop to JK-FlipFlop. [6+4]

OR

7.a) With a neat diagram, explain the operation of a 10-bit ring counter.
b) Explain the operation of synchronous and asynchronous counter. [5+5]

8.a) Design a sequential circuit for the diagram shown in the below figure.



b) Discuss about the capabilities of Finite State Machines. [6+4]

OR

9.a) Explain in detail about state equivalence and machine minimization.
b) With an example, describe state reduction in an incompletely specified machine. [5+5]

10.a) Draw the circuit of CMOS NOR gate and explain its operation. List some of the advantages of CMOS over other logic families.
b) Explain about Fan-In, Fan-Out, Tri-state gate. [5+5]

OR

11.a) Draw and explain the circuit of 2-input NAND and 2-input NOR gates using CMOS.
b) Draw the symbol of CMOS transmission gate and write its advantages and applications. [5+5]

---ooOoo---

Code No: 153AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, March - 2022
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Solve for x

i) $(257)_8 = (x)_2$ ii) $(21.625)_{10} = (x)_8$ iii) $(BC.2)_{16} = (x)_8$ iv) $(33)_{10} = (201)_x$

b) Obtain dual of the following Boolean expressions
(i) AB+A(B+C)+B′(B+D) (ii) A+B+A′B′C. [8+7]

2.a) Express the Decimal Digits 0-9 in BCD, 2421, 84-2-1 and Excess-3.
b) Using the tabular method, obtain the minimal expression for
$F = \sum m(6, 7, 8, 9) + \sum d(10, 11, 12, 13, 14. 15)$. [7+8]

3.a) Minimize the following expression using K-map and realize using NAND Gates.
$F(A,B,C,D) = \sum m(1,3,7,11,15) + \sum d(0,2,5)$.
b) Construct a full adder using only two half adders and one OR gate. [8+7]

4.a) With the aid of external logic, convert D type flip-flop to a JK flip-flop.
b) Design a synchronous modulo-12 counter using JK flip-flop. [5+10]

5.a) Find the characteristic equation for:
i) T flip-flop ii) D flip-flop
b) Draw and explain the operations of 4-bit universal shift register. [8+7]

6.a) Draw and explain the modulo N –counters.
b) Explain concept of minimal cover table. [10+5]

7.a) Discuss about the approaches of designing synchronous sequential finite state machines.
b) Design a 1101 sequence detector and draw its logic diagram. [5+10]

8. Write a short note on followings:
a) CMOS transmission gate
b) Tristate TTL
c) AND, OR gates using DTL. [5+5+5]

---ooOoo---

Code No: 153AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, March - 2021
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Convert the following to Decimal and then to octal.
i) $(125F)_{16}$
ii) $(10111111)_2$
iii) $(4234)_5$.
b) How do you convert a gray number to binary? Generate a 4-bit gray code directly using the mirror image property. [7+8]

2.a) Find all the prime implicants of the function using Quine McClusky method
$f(a,b,c,d) = \Sigma(7,9,12,13,14,15) + d(4,11)$.
b) Design a circuit that converts 8421 BCD code to XS-3 code. [8+7]

3.a) With a neat circuit diagram and waveforms explain the operation of Master Slave JK flip flop.
b) Explain the conversion of SR flip flop into JK and D flip flop with an excitation table. [8+7]

4.a) What are the capabilities and limitations of finite state machines? Explain.
b) Draw the diagram of Mealy type FSM for serial adder. [8+7]

5.a) Describe the operation of TTL logic circuit working as NAND gate.
b) Realize 2-input OR gates using CMOS logic and then explain its operation with the help of functional table. [7+8]

6.a) Convert the following expression into SOP and POS:
i) $(AB+C)(B+C'D)$
ii) $x'+(x+y')(y+z')$
b) Implement the switching function using $F = \Sigma m(0,1,3,4,12,14,15)$ using an 8 input MUX. [8+7]

7.a) Design a 3-bit synchronous counter with T-flip flop and draw the diagram.
b) Discuss the differences between combinational and sequential circuit. [9+6]

8.a) Mention the characteristics of different logic families. Also compare the performance of TTL, CMOS and ECL logic.
b) Design a synchronous sequential circuit which goes through the following states: 1, 3, 5, 3, 6, 1, 3, 5. [8+7]

---ooOoo---

Code No: 153AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, August/September -2022
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) State and prove Boolean Theorems:
i) Commutative ii) Associative iii) Distributive

b) Expand $A(\bar{A}+B)(\bar{A}+B+\bar{C})$ to maxterms and minterms.

c) i) Add $6E_{16}$ and $C5_{16}$ ii) Add $5D_{16}$ from $3A_{16}$ [6+5+4]

2.a) Reduce the following function using K-Map.
F(A,B,C,D,E) = Σm (1,4,8,10,11,20,22,24,25,26)+d(0,12,16,17)

b) Design and explain a 4-bit binary parallel Adder/Substractor. [8+7]

3.a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers.

b) Describe the operations performed by the following logic circuits with an example: (i) Comparator (ii) Decoder (iii) Encoder. [9+6]

4.a) With the block diagram, Truth table, describe the principle operation of edge triggered negative SR flip flop.

b) Explain the operation of 4-stage twisted ring counter with circuit diagram and timing diagram. [8+7]

5.a) Differentiate combinational and sequential circuits.

b) Write differences between Mealy and Moore machines.

c) Write the limitations of finite state machines? [5+5+5]

6.a) Design, draw and explain a 4-bit ring counter using D- flip flops with relevant timing diagrams.

b) Explain the operation J-K master slave flip flop. Explain its truth table. [8+7]

7.a) Draw a state diagram of a sequence detector which can detect 101.

b) How to interface TTL and CMOS and also CMOS to TTL. [10+5]

8.a) Discuss about RTL logic family in detail, with one example.

b) Realize 2-input NAND using TTL logic. [8+7]

---ooOoo---

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

I - Mid Examinations, JAN -2023

Set -I

Year & Branch: **II –ECE (A,B)** **Date: 23/01/23(FN)**

Subject: **DSD** Max. Marks: 10 Time: 60 mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

1.a) Write 12-bit hamming code,for a given 8 bit data 01011011 (C213.1) (3M) (Knowledge)

b)Locate and Correct if any errors,if the received hamming code is 101110110100 there are four parity bits and even parity is used. (C213.1) (2M)

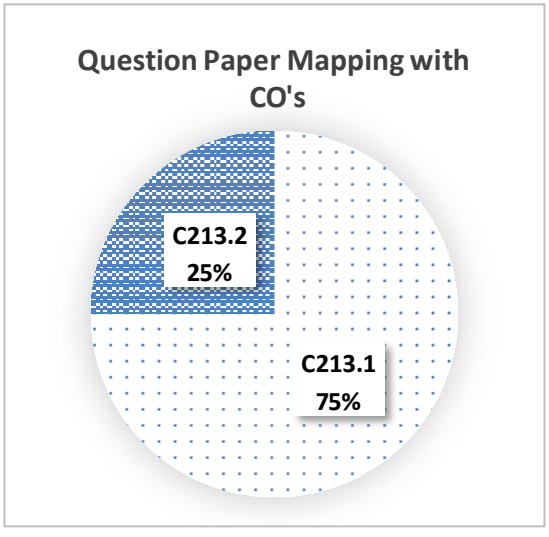
2. a)Define Universal gates and properties of X-OR Gates? (C213.1) (3M) (Knowledge)

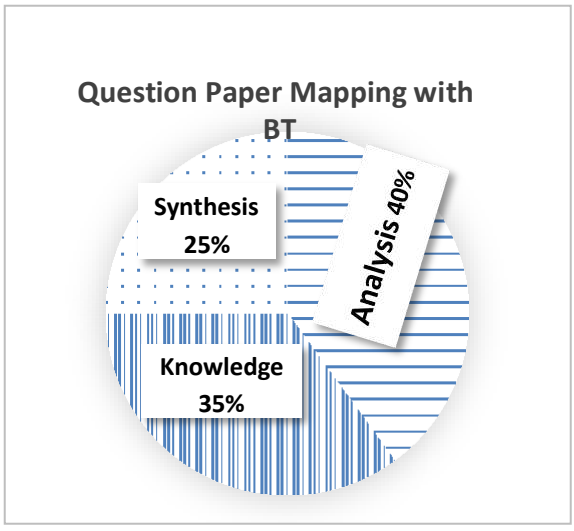
b)Change the Expression **X(X+Y')(Y+Z')** into sum of products and product of sums (C213.1) (Comorehension) (2M)

3. Apply the K-Map method to simplify the Boolean functions **Y=AB+C+ACD+ABCD+CD** ? (C213.1) (5M) (Application)

4a) State and proof the De-Morgan's Theoram (C213.2) (3M) (Knowledge)

b) Solve the given expression using De-Morgan's Theoram **((AB)'+A'+AB)'** (C213.2) (3M) (Evaluation)





Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

II - Mid Examinations, APRIL -2023

Set -I

Year & Branch: **II –ECE (A,B)** **Date: 31/03/23(FN)**

Subject: **DSD** Max. Marks: 10 Time: 60 mins

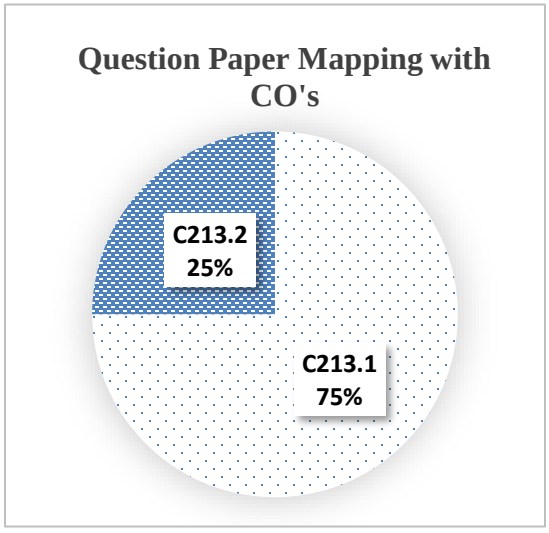
Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

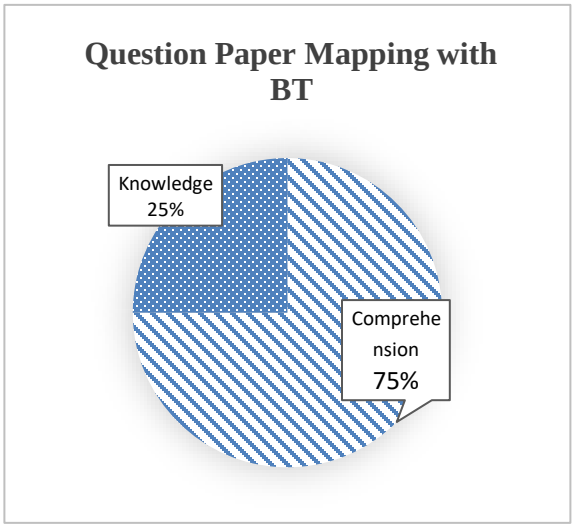
1. Explain in detail Universal Shift register (C213.1) (5M) (Knowledge)

2. Design a 3-bit up/down counter which counts up when the control signal M=1 & counts down when M=0 (C213.1) (5M) (Comprehension)

3. Define Sequence Detector? Design a Mealy type sequence detector to detect a serial input sequence of 101 ? (C213.1) (5M) (Knowledge)

4.Difference between logic families and Explain in detail TTL logic family (C213.2) (5M) (Knowledge)





SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ECE

B.Tech II Year I Sem I Mid –Term Examination,JAN-2023

DIGITAL SYSTEM DESIGN

(Objective Exam)

DATE: 23/01/2023(FN) **TIME: 20 Min** **MAX.MARKS: 10**

NAME : _____ **ROLL NO:** _____ **MARKS:** _____

I.Choose The Correct Answers

1. The value of binary 1111 is [ ]

a) 2^3 -1 b) 2^4-1 c) 2^4 d) none of these

2. The following code is not a BCD code. [ ]

a) Gray Code b) Xcess3 Code c) 8421 code d) All of these

3. A 15-bit hamming code requires [ ]

a) 4 parity bits b) 5 parity bits c) 15 parity bits d) 7 parity bits

4. Which of the following are called Universal gates [ ]

a) NAND, NOR b) AND, OR c) XOR XNOR d) OR, XOR

5. A gate is enabled when its enable input is at logic 0. The gate is [ ]

a) NOR b) AND c) NAND d) None of these '

6 Convert the hexadecimal number (1E2)16 to decimal [ ]

a)480 b)482 c) 481 d) 484

7. $(170)_{10}$ is equivalent to [ ]

a) $(FD)_{16}$ b) $(DF)_{16}$ c) $(AA)_{16}$ d) $(AF)_{16}$

8. In combinational circuits the o/p depends on _____i/p [ ]

a) Present b) Past c) A & B d) None

9. An overflow occurs in _____ [ ]

a) MSD position b) LSD position c) Middle position d) Signed Bit

10 The combinational circuits are_____ than sequential circuits [ ]

a) Slower b) Faster c) Same Speed d) None

II.Fill In The Blanks:

1. Cyclic codes are also called _____codes.
2. The basic two types of BCD codes are _____and_____ codes
3. The NOR gate can function as a NOT gate if _____
4. The NOR-NOR Realization is equivalent to ---------- gates
5. The 2's Complement of 10110000----------
6. Code is a symbolic representation of _____ information
7. In Boolean algebra A+AB= _____
8. The output of a logic gate is 1 , when all its inputs are at logic 0.The gate is either----------
9. Truth table is used to express ----------
10. The logical sum of two or more logical product terms is called _____

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ECE

B.Tech II Year I Sem II Mid –Term Examination,APRIL-2023

DIGITAL SYSTEM DESIGN

(Objective Exam)

DATE: 31/03/2023(FN) **TIME: 20 Min** **MAX.MARKS: 10**

NAME : _____ **ROLL NO:** _____ **MARKS:** _____

I.Choose The Correct Answers

1. How many Flipflops are Cascaded in Master Slave filpflop [ ]

a) 1 b) 2 c) 3 d) 4

2.Modulus of a counter having n-bit is given as [ ]

a) $2n \geq N$ b) $2^n \geq N$ c) $2/n=N$ d) $2+n=N$

3.How many states are required to detect 110 in moore circuit [ ]

a) 1 b) 4 c) 3 d) 6

4.Which of the following filpflop is used as a latch [ ]

a) J-K flipflop b) Master-Slave flipflop c) S-R flipflop d)T flipflop

5.The characteristic equation of a T- flipflop [ ]

a) $Q_{n+1}=Q_n'T+ Q_nT'$ b) $Q_{n+1}= Q_n'T'+ Q_nT$ c) $Q_{n+1}=Q_n R+S'$ d) $Q_{n+1}=Q_n'$

6.In general, a Sequential Logic Circuit consists of [ ]

a) only flip-flops b)only gates

c) flip-flops& Combinational Logic Circuits d) only Combinational Logic Circuits

7. A Sequential Circuit with 10 states will have [ ]

a)10 flip-flops b) 5 flip-flops c) 4 flip-flops d) 0 flip-flops

8.Mealy type of outputs are [ ]

a) Independent of the inputs b)dependent only on inputs

c) dependent only on present states d) dependent only on the present state and inputs

9. Which of the following is the fastest of all logic families [ ]

a)TTL b)ECL c)DTL d)CML

10.Which gate is used as an Inverter [ ]

a) AND b) NAND c) NOR d) EX-OR

II.Fill In The Blanks:

1. For a J-K flipflop, J=1,K=1 is the _____ mode.

2. Synchronous counters are _____ than Asynchronous counters.

3. _____ circuits require memory elements.

4. Moore type of outputs are dependent on _____

5.The Modulo-10 counter is also called as _____

6.The number of pins connected to a given output is known as _____

7.The operating speed of totem- pole output is _____

8.What is a figure of merit _____

9. Redundant states can be reduced using _____ technique.

10.A register capable of shifting the binary information in one or both directions is known as _____ register.

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

B-Tech I - Mid Examinations, JAN-2023

Year &Branch: II –ECE-A, B **Date: 23-01-2023(FN)**

Subject: DSD

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1sZJ07wK6cRaLrNuBzUn8pp5DS9RY3qKj/view?usp=sharing

Objective Key Paper

I.Choose The Correct Answers

1)B

2)B

3)A

4)A

5)A

6)B

7)C

8)C

9) A

10)B

II.Fill In The Blanks:

1) Block Code

2)unpacked and packed

3)one input is set to 0

4) OR ,AND Realization

5) 01010000

6) Discrete

7) AB

8) NOR

9) Boolean Expression

10) SOP

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

B-Tech II - Mid Examinations, APRIL-2023

Year &Branch: II –ECE-A, B **Date: 31-03-2023(FN)**

Subject: DSD

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1kaQU5UaJY9VavOiwCHPLPu6BKPcHqo0V/view?usp=sharing

Objective Key Paper

I.Choose The Correct Answers

1)B

2)B

3)B

4)C

5)A

6)C

7)C

8)D

9) D

10)B

II.Fill In The Blanks:

1) Toggle

2) Faster

3) Sequential circuits

4) Present state of the flipflop

5) Decade Counter

6) Fan-in

7) High

8) Power dissipation*Propagation delay

9) State Reduction

10) Shift Register

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

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(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

ASSIGNMENT- 1 **SUBJECT: DIGITAL SYSTEM DESIGN**

1.State and proof the De-Morgan's theorem. **C213.1 Knowledge**

2. Define Universal gates and Properties of X-OR gates. **C213.1 Knowledge**

3. A) Write 7-bit hamming code, for a given 4-bit data 1110 by using even parity.
B) Write 12-bit hamming code, for a given 8-bit data 01011011 by using even parity. **C213.1 Knowledge**

4. A) Solve the binary subtraction using 1's and 2's complement method. $(110011)_2$-$(1110011)_2$

B) Design all the basic gates using only NAND gates **C213.1 Evaluation**

5. A)Design and explain 3 to 8 decoder with necessary truth table and logic diagram

C213.1Synthesis

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Website: https://siiet.ac.in/

ASSIGNMENT- II **SUBJECT: DIGITAL SYSTEM DESIGN**

1	A)Write the characteristic equations and excitation tables of JK, SR, D and T flip-flops. B) Explain the Race around condition in flip-flops in detail.	C213.3	Comprehension Knowledge
2	Explain in detail Universal Shift Register.	C213.3	Comprehension
3	Design a 4-bit up/down ripple counter and explain its timing diagrams.	C213.3	Synthesis
4	Define sequence detector? Design a mealy type sequence detector to detect a serial input sequence of 101.	C213.4	Knowledge
5	Design and construct MOD-10 synchronous counter using JK flip flops.	C213.4	Synthesis
6	Design a serial adder for moore circuit	C213.4	Synthesis

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TUTORIAL TOPICS **SUBJECT: DIGITAL SYSTEM DESIGN**

S.NO	Unit	TOPIC	Number of Sessions Planned	Teaching method/Aids
1.	1	Write 12-bit hamming code,for a given 8 bit data 01011011	1	**BB**
2.		Change the Expression **X(X+Y')(Y+Z')** into sum of products and product of sums	1	BB
3.	2	Apply the K-Map method to simplify the Boolean functions **Y=AB+C+ACD+ABCD+CD**	1	BB
4.		Solve the given expression using De-Morgan's Theoram **((AB)'+A'+AB)'**	1	BB
5.	3	. Explain in detail Universal Shift register	1	BB
6.		Define Sequence Detector? Design a Mealy type sequence detector to detect a serial input sequence of 101	1	BB
7.	4	Difference between logic families and Explain in detail TTL logic family (C213.2) (5M) (Knowledge)	1	BB
8.		.	1	BB
9.	5	Explain about Read and Write cycles of a static RAM with neat timing waveforms	1	BB
10.		Convert an SR Flip-Flop into JK Flip-Flop.	1	BB

2.2.1: Assess Learning Levels, Special programs for advance& Slow learners

Result Analysis:

Course Title	DIGITAL SYSTEM DESIGN
Course Code	EC303PC
Programme	B.Tech
Year & Semester	IIyear I-semester.
Regulation	R18
Course Faculty	Mrs.G.Anusha ,Assistant Professor, ECE

Slow learners:

S No	Roll no	No of backlogs	Internal-I Status	Internal-II Status
1	21X31A0402	3S	16	16
2	21X31A0403	3S	16	17
3	21X31A0408	3S	18	18
4	21X31A0409	4S	14	15
5	21X31A0412	3S	21	14
6	21X31A0414	3S	21	16
7	21X31A0417	3S	18	18
8	21X31A0422	3S	17	18
9	21X31A0433	3S	22	19
10	21X31A0435	3S	19	19
11	21X31A0436	3S	14	17
12	21X31A0441	4S	15	19
13	21X31A0443	3S	25	17

14	21X31A0445	3S	22	14
15	21X31A0449	3S	19	19
16	21X31A0450	3S	19	14
17	21X31A0453	3S	21	20
18	21X31A0455	3S	16	18
19	21X31A0457	3S	20	18
20	21X31A0458	3S	19	18
21	21X31A0460	3S	22	17

Advanced learners:

S.NO	ROLL.NO.	Percentage	GATE MATERIAL
1	21X31A0401	71	Boolean algebra, minimization of functions using Boolean identities and Karnaugh map, logic gates and their static CMOS implementations, arithmetic circuits, code converters, multiplexers, decoders and PLAs; Sequential circuits: latches and flip-flops, counters, shift-registers and finite state machines
2	21X31A0413	72	
3	21X31A0415	70.875	
4	21X31A0418	73.755	
5	19X31A0420	82.625	
6	21X31A0423	72.255	
7	21X31A0426	78.755	
8	21X31A0442	71.62	
9	21X31A0444	70.625	
10	21X31A0446	74.12	
11	21X31A0447	71.12	

12	21X31A0451	73.75	
13	21X31A0452	73.75	
14	21X31A0459	74.62	
15	21X3A0464	73.375	
16	21X31A0465	75	
17	21X31A0466	72	
18	21X31A0467	71.25	
19	21X31A0468	68.875	
20	21X31A0469	76.5	
21	21X31A0470	72.75	
22	21X31A0471	78.375	
23	21X31A0472	86.125	

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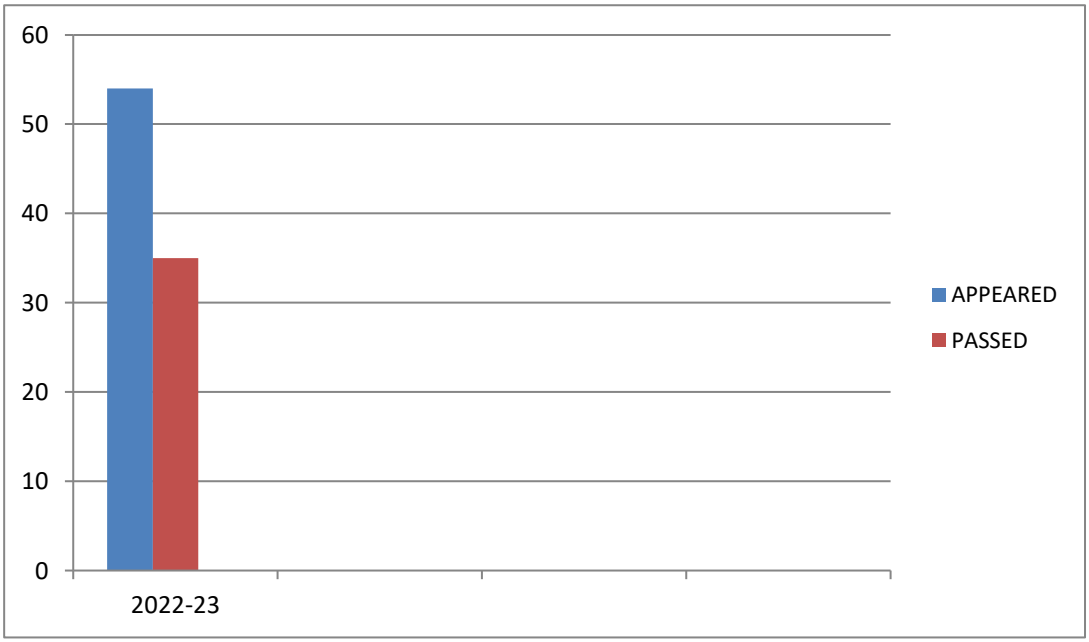
BATCH ECE-II BTECH I SEM ECE-A RESULT ANALYSIS

ACADAMIC YEAR	COURSE NAME	NUMBER OF STUDENTS		QUESTION PAPER SETTING		PASS%
		APPEARED	PASSED	INTERNAL	EXTERNAL	
2022-23	DIGITAL SYSTEM DESIGN	54	35	COURSE FACULTY	JNTUH	63.33

DIGITAL SYSTEM DESIGN (C213) RESULT ANALYSIS



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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

REMEDIAL CLASSES TIME TABLE

A.Y 2022-23 **SEMESTER-I**

BRANCH/ SEC	MON 4.00 PM-5.00 PM	TUE 4.00 PM-5.00 PM	WED 4.00 PM-5.00 PM	THUR 4.00 PM-5.00 PM	FRI 4.00 PM-5.00 PM
II ECE-A	EDC	NATL	DSD	PTSP	SS
II ECE-B	NATL	DSD	PTSP	SS	EDC
III ECE-A	MPMC	DCCN	CS	BEFA	EMI
III ECE-B	DCCN	CS	BEFA	EMI	MPMC
III ECE-C	CS	BEFA	EMI	MPMC	DCCN
IV ECE-A	MW&OC	DIP	PPLE	NS&C	JAVA
IV ECE-B	DIP	PPLE	NS&C	JAVA	MW&OC
IV ECE-C	PPLE	NS&C	JAVA	MW&OC	DIP

Head of the Department
Electronics and Communication Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH,
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510.

PRINCIPAL
Sri Indu Institute of Engineering & Tech.
Sheriguda(Vill), Ibrahimpatnam,
R.R. Dist. Telangana -501 510.

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty: G. Anusha — Academic Year: 2022-23

Branch & Section: ECE - A — Examination: I Internal

Course Name: DIGITAL SYSTEM DESIGN — Year: II — Semester: I

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj1	A1
Max. Marks ==>		5		5		5		5		10	5
1	21X31A0401	3				3				2	5
2	21X31A0402	3		2						6	5
3	21X31A0403		4	3						5	5
4	21X31A0404	3				3				5	5
5	21X31A0405	5		4						6	5
6	21X31A0406	3				2				6	5
7	21X31A0407	3		3						7	5
8	21X31A0408	3				3				6	5
9	21X31A0409	5								5	5
10	21X31A0410	3				3				7	5
11	21X31A0412	2		2			2			7	5
12	21X31A0413	4		2						7	5
13	21X31A0414			4		2				7	5
14	21X31A0415		3			3				8	5
15	21X31A0416	3								8	5
16	21X31A0417	2		2						9	5
17	21X31A0418	4								9	5
18	21X31A0420	5		4						9	5
19	21X31A0421	5				4				6	5
20	21X31A0422	5						3		6	5
21	21X31A0423		4			3				9	5
22	21X31A0424	5								10	5
23	21X31A0425	3		3						10	5
24	21X31A0426	4				1				10	5
25	21X31A0427	5								10	5
26	21X31A0428	5		2						8	5
27	21X31A0429	3				1				8	5
28	21X31A0431	2		2						10	5
29	21X31A0432	5								10	5
30	21X31A0433	4			2					10	5
31	21X31A0434	4		4						10	5
32	21X31A0435		4			3				7	5
33	21X31A0436	5			2					4	5
34	21X31A0437	4					2			4	5
35	22X35A0401	5		4						9	5
36	22X35A0402		5	4						9	5
37	22X35A0403	4					4			9	5
38	22X35A0404	3				4				6	5
39	22X35A0405	4		3						8	5
40	22X35A0406		5	2						8	5

41	22X35A0407	5					5			8	5
42	22X35A0408	3	2							10	5
43	22X35A0409	5		3						9	5
44	22X35A0410	4				3				10	5
45	22X35A0411	5		3						8	5
46	22X35A0412	4		4						9	5
47	22X35A0413	5				4				9	5
48	22X35A0414	4		3						10	5
49	22X35A0415	4		2						9	5
50	22X35A0416	5		4						10	5
51	22X35A0417	4				4				8	5
52	22X35A0418	4		5						9	5
53	22X35A0419	5				4				8	5
54	22X35A0420	5		4						9	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		44	7	18	2	13	4	1	0	48	54
Number of students attempted		47	7	26	2	17	4	1	0	54	54
Percentage of students scored more than target		94%	100%	69%	100%	76%	100%	100%		89%	100%

CO Mapping with Exam Questions:

CO - 1	**Y**		**Y**		**Y**				Y	Y
CO - 2							**Y**		Y	Y
CO - 3									Y	Y

CO - 4										
CO - 5										
CO - 6										

>Target %	94%	100%	69%	100%	76%	100%	100%		89%	100%

CO Attainment based on Exam Questions:

CO - 1	94%		69%		76%				89%	100%
CO - 2							100%		89%	100%
CO - 3									89%	100%
CO - 4										
CO - 5										
CO - 6										

CO	**Subj**	obj	Asgn	Overall	Level
CO-1	80%	89%	100%	90%	3.00
CO-2	100%	89%	100%	96%	3.00
CO-3		89%	100%	94%	3.00
CO-4					
CO-5					
CO-6					

Attainment Level	
1	40%
2	60%
3	>60%

Attainment (Internal 1 Examination) **3.00**

Faculty Signature

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-2)

Name of the faculty: G. Anusha — Academic Year: 2022-23
Branch & Section: ECE - A — Examination: II Internal
Course Name: DIGITAL SYSTEM DESIGN — Year: II — Semester: I

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj4	A4
Max. Marks ==>		3	2	5		5		5		10	5
1	21X31A0401	3				3				6	5
2	21X31A0402	3		2						8	5
3	21X31A0403		4	3						8	5
4	21X31A0404	3				3				8	5
5	21X31A0405	5		4						4	5
6	21X31A0406	3				2				8	5
7	21X31A0407	3		3						4	5
8	21X31A0408	3				3				7	5
9	21X31A0409	5								7	5
10	21X31A0410	3				3				7	5
11	21X31A0412	2		2			2			5	5
12	21X31A0413	4		2						8	5
13	21X31A0414			4		2				7	5
14	21X31A0415		3			3				8	5
15	21X31A0416	3								5	5
16	21X31A0417	2		2						8	5
17	21X31A0418	4								4	5
18	21X31A0420	5		4						9	5
19	21X31A0421	5				4				8	5
20	21X31A0422	5						3		8	5
21	21X31A0423		4			3				10	5
22	21X31A0424	5								10	5
23	21X31A0425	3		3						10	5
24	21X31A0426	4				1				10	5
25	21X31A0427	5								10	5
26	21X31A0428	5		2						9	5
27	21X31A0429	3				1				4	5
28	21X31A0431	2		2						5	5
29	21X31A0432	5								4	5
30	21X31A0433	4			2					9	5
31	21X31A0434	4		4						8	5
32	21X31A0435		4			3				9	5
33	21X31A0436	5			2					7	5
34	21X31A0437	4					2			8	5
35	22X35A040	5		4						10	5
36	22X35A040		5	4						10	5
37	22X35A040	4					4			10	5
38	22X35A040	3				4				10	5
39	22X35A040	4		3						10	5
40	22X35A040		5	2						9	5
41	22X35A040	5					5			9	5
42	22X35A040	3	2							9	5
43	22X35A040	5		3						9	5
44	22X35A041	4				3				9	5

45	22X35A041	5		3						10	5
46	22X35A041	4		4						10	5
47	22X35A041	5				4				9	5
48	22X35A041	4		3						9	5
49	22X35A041	4		2						6	5
50	22X35A041	5		4						9	5
51	22X35A041	4				4				10	5
52	22X35A041	4		5						10	5
53	22X35A041	5				4				10	5
54	22X35A042	5		4						10	5
Target set by the faculty / HoD		1.80	1.20	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		47	7	17	2	13	4	1	0	46	54
Number of students attempted		47	7	25	2	17	4	1	0	54	54
Percentage of students scored more than target		100%	100%	68%	100%	76%	100%	100%		85%	100%

CO Mapping with Exam Questions:

CO - 1										
CO - 2										
CO - 3		y								
CO - 4	**y**								y	y
CO - 5			**Y**						y	y
CO - 6					**y**		**y**		y	y

CO Attainment based on Exam Questions:

CO - 1										

CO - 2										
CO - 3										
CO - 4	100%								85%	100%
CO - 5			68%						85%	100%
CO - 6					76%		100%		85%	100%

CO	**Subj**	obj	Asgn	Overall	Level
CO-1					
CO-2					
CO-3					
CO-4	100%	85%	100%	95%	3.00
CO-5	68%	85%	100%	84%	3.00
CO-6	88%	85%	100%	91%	3.00

Attainment Level	
1	40%
2	60%
3	>60%

Attainment (Internal Examination-2) **3.00**

Faculty Signature

RI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty : G. Anusha | Academic Year: 2022-23

Branch & Section: ECE - A | Year / Semester: II / I

Course Name: DIGITAL SYSTEM DESIGN

S.No	Roll Number	Marks Secured
1	21X31A0401	36
2	21X31A0402	10
3	21X31A0403	19
4	21X31A0404	22
5	21X31A0405	23
6	21X31A0406	34
7	21X31A0407	5
8	21X31A0408	0
9	21X31A0409	4
10	21X31A0410	35
11	21X31A0412	8
12	21X31A0413	23
13	21X31A0414	8
14	21X31A0415	11
15	21X31A0416	6
16	21X31A0417	11
17	21X31A0418	17
18	21X31A0420	16
19	21X31A0421	8

S.No	Roll Number	Marks Secured
36	22X35A0402	40
37	22X35A0403	20
38	22X35A0404	30
39	22X35A0405	17
40	22X35A0406	13
41	22X35A0407	30
42	22X35A0408	17
43	22X35A0409	19
44	22X35A0410	29
45	22X35A0411	7
46	22X35A0412	39
47	22X35A0413	29
48	22X35A0414	40
49	22X35A0415	37
50	22X35A0416	53
51	22X35A0417	15
52	22X35A0418	23
53	22X35A0419	19
54	22X35A0420	23

20	21X31A0422	4
21	21X31A0423	23
22	21X31A0424	4
23	21X31A0425	16
24	21X31A0426	14
25	21X31A0427	52
26	21X31A0428	11
27	21X31A0429	29
28	21X31A0431	12
29	21X31A0432	21
30	21X31A0433	14
31	21X31A0434	40
32	21X31A0435	11
33	21X31A0436	11
34	21X31A0437	36
35	22X35A0401	35
Max Marks		75

Class Average mark	35
Number of students performed above the	1
Number of successful students	54
Percentage of students scored more than	2%
Attainment level	**1**

Attainment Level	**% students**
1	40%
2	60%
3	>60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment

Name of the faculty: G. Anusha
Branch & Section: ECE - A
Course Name: DIGITAL SYSTEM DESIGN

Academic Year: 2022-23
Examination: I Internal
Year: II
Semester: I

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00		3.00	1.00	2.40
CO2	3.00		3.00	1.00	2.40
CO3	3.00		3.00	1.00	2.40
CO4		3.00	3.00	1.00	2.40
CO5		3.00	3.00	1.00	2.40
CO6		3.00	3.00	1.00	2.40
Internal & University Attainment:			3.00	1.00	
Weightage			70%	30%	
ttainment for the course (Internal, Unive			2.10	0.30	
) Attainment for the course (Direct Meth			2.40		

Overall course attainment level **2.40**

Faculty Signature

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Program Outcome Attainment (from Course)

Name of Faculty:	G. Anusha	Academic Year:	2022-23
Branch & Section:	ECE - A	Year:	II
Course Name:	DIGITAL SYSTEM DESIGN	Semester:	I

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	-	2	3
CO2	3	3	3	-	-	-	-	-	-	-	2	3	3	3
CO3	3	2	3	-	-	-	-	-	-	-	-	-	2	3
CO4	3	1	3	-	-	-	-	-	-	-	3	-	3	3
CO5	3	-	3	-	-	-	-	-	-	-	-	2	3	3
CO6	2	-	3	-	-	-	-	-	-	-	-	-	3	3
Course	**3**	**2**	**3**								**2.5**	**2.5**	**2.5**	**2.5**

CO	**Course Outcome Attainment**
CO1	2.40
CO2	2.40
CO3	2.40
CO4	2.40
CO5	2.40
CO6	2.40
Overall course attainment level	**2.40**

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainment	**2.40**	**1.60**	**2.40**								**2.00**	**2.00**	**2.00**	**2.00**

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)

Faculty Signature

ASSIGNMENTS AND REGISTERS

Assignment 1 script link:

https://drive.google.com/file/d/1CPIgpbRpZ2wXd5y0iLHC35pyhJEcz2B-/view?usp=sharing

Assignment 2 script link:

https://drive.google.com/file/d/1M1kr-GYOMyYjZT4HLNprGp3PizAF260S/view?usp=sharing

Attendance register link:

https://drive.google.com/file/d/1VT_Gh6o_k9gfDsx-MfiEYJ82A8-1yjb5/view?usp=sharing