Sri Indu Institute of Engineering & Technology

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COURSE FILE

ON

DIGITAL SYSTEM DESIGN LAB

Course Code – EC307PC

II B.Tech I-SEMESTER

A.Y.: 2022-2023

Prepared by

Mrs. G.Anusha
Assistant Professor

Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year	2022-2023
Course Title	DIGITAL SYSTEM DESIGN LAB
Course Code	EC307PC
Programme	B. Tech
Year & Semester	II year I-semester
Room Number	A-313
Name of the lab in charge	Mrs. G. Anusha
Name of the faculty in charge	Mrs. G. Anusha.

Index of Course File

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INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To Continuous assess of teaching-learning process through institute-industry collaboration.

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.

IM4: To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

DM1: To facilitate an academic environment that enables student's centric learning.

DM2: To provide state-of-the-art hardware and software technologies to meet industry requirements.

DM3: To continuously update the Academic and Research infrastructure.

DM4: To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

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PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

PEO1: Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.

PEO2: Graduates with ability to execute innovative ideas for Research and Development with continuous learning.

PEO3: Graduates inculcated with industry based soft-skills to enable employability.

PEO4: Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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PROGRAM OUTCOMES

1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

6. **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING
COURSE STRUCTURE & SYLLABUS (R18)

Applicable From 2018-19 Admitted Batch

I YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	MA101BS	Mathematics - I	3	1	0	4
2	AP102BS	Applied Physics	3	1	0	4
3	CS103ES	Programming for Problem Solving	3	1	0	4
4	ME104ES	Engineering Graphics	1	0	4	3
5	AP105BS	Applied Physics Lab	0	0	3	1.5
6	CS106ES	Programming for Problem Solving Lab	0	0	3	1.5
7	*MC109ES	Environmental Science	3	0	0	0
		Induction Programme				
		Total Credits	**13**	**3**	**10**	**18**

I YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	MA201BS	Mathematics - II	3	1	0	4
2	CH202BS	Chemistry	3	1	0	4
3	EE203ES	Basic Electrical Engineering	3	0	0	3
4	ME205ES	Engineering Workshop	1	0	3	2.5
5	EN205HS	English	2	0	0	2
6	CH206BS	Engineering Chemistry Lab	0	0	3	1.5
7	EN207HS	English Language and Communication Skills Lab	0	0	2	1
8	EE208ES	Basic Electrical Engineering Lab	0	0	2	1
		Total Credits	**12**	**2**	**10**	**19**

II YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC301PC	Electronic Devices and Circuits	3	1	0	4
2	EC302PC	Network Analysis and Transmission Lines	3	0	0	3
3	EC303PC	Digital System Design	3	1	0	4
4	EC304PC	Signals and Systems	3	1	0	4
5	EC305ES	Probability Theory and Stochastic Processes	3	0	0	3
6	EC306PC	Electronic Devices and Circuits Lab	0	0	2	1
7	EC307PC	Digital System Design Lab	0	0	2	1
8	EC308ES	Basic Simulation Lab	0	0	2	1
9	*MC309	Constitution of India	3	0	0	0
		Total Credits	**18**	**3**	**6**	**21**

II YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	MA401BS	Laplace Transforms, Numerical Methods & Complex Variables	3	1	0	4
2	EC402PC	Electromagnetic Fields and Waves	3	0	0	3

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R18 B.Tech. ECE Syllabus JNTU HYDERABAD

EC307PC: DIGITAL SYSTEM DESIGN LAB

B.Tech. II Year I Sem. **L T P C**
0 0 2 1

Note: Implement using digital ICs, all experiments to be carried out.

List of Experiments

1. Realization of Boolean Expressions using Gates
2. Design and realization logic gates using universal gates
3. Generation of clock using NAND / NOR gates
4. Design a 4 – bit Adder / Subtractor
5. Design and realization of a 4 – bit gray to Binary and Binary to Gray Converter
6. Design and realization of an 8 bit parallel load and serial out shift register using flip-flops.
7. Design and realization of a Synchronous and Asynchronous counter using flip-flops
8. Design and realization of Asynchronous counters using flip-flops
9. Design and realization of 8x1 MUX using 2x1 MUX
10. Design and realization of 4 bit comparator
11. Design and Realization of a sequence detector-a finite state machine

Major Equipments required for Laboratories:

1. 5 V Fixed Regulated Power Supply/ 0-5V or more Regulated Power Supply.
2. 20 MHz Oscilloscope with Dual Channel.
3. Bread board and components/ Trainer Kit.
4. Multimeter.

TEXT BOOKS:

T1. Switching and Fininte Automata Theory-Zvi Kohavi & Niraj K.Jha,3rd Edition,Cambridge.
T2: Modern Digital Electronics – R. P. Jain, 3rd Edition, 2007- Tata McGraw-Hill

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Digital System Design Lab

CO's, PO's,PSO's MAPPING

A.Y: 2022-23 **SEMESTER: I** **CLASS: II ECE-A, B**

Course Outcomes:

After completing this course, the student will be able to:

C217.1: Identify the IC Configurations of Digital Circuits. (Knowledge)

C217.2: Verify and Compare the different types of gates and comparators. (Analysis)

C217.3: Develop the clock using universal gates. (Synthesis)

C217.4: Design and Realization of Sequential circuits. (Synthesis)

C217.5: Analyze and implementation of sequential circuits. (Analysis)

C217.6: Compare the combinational and Sequential circuits. (Evaluation)

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C217.1	3	2	-	-	3	2	2	-	2	-	-	3	3	3
C217.2	3	3	3	2	2	2	2	1	1	2	2	-	3	3
C217.3	3	2	3	3	2	2	2	1	1	2	-	2	3	3
C217.4	3	1	3	2	2	2	1	1	2	1	-	-	3	3
C217.5	3	-	3	2	2	1	1	-	1	2	-	2	3	3
C217.6	3	-	3	3	3	1	1	-	1	2	-	2	3	3
AVG	**3.00**	**2.00**	**2.50**	**2.50**	**2.50**	**2.00**	**2.00**	**1.50**	**2.00**	**2.00**	**2.00**	**2.33**	**3.00**	**3.00**

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Digital System Design Lab

LIST OF EXPERIMENTS AND THEIR CO, PO/PSO MAPPING

S.No	Name of The Experiment	CO	PO/PSO
1	Boolean Expressions	1	1,2,5,6,7,9,12/1,2
2	Logic Gates Using Universal Gates	2	1,2,3,4,5,6,7,8,9,10,11/1,2
3	Generation of Clock using NAND Gates	3	1,2,3,4,5,6,7,8,9,10,12/1,2
4	Design a 4-bit Binary Adder/Subtractor	2	1,2,3,4,5,6,7,8,9,10,12/1,2
5	Design a 4 bit Binary to Gray and Gray to Binary Converter	4	1,3,4,5,6,7,9,10,12/1,2
6	Parallel -load Serial-out Shift register using Flipflops	4	1,3,4,5,6,7,9,10,12/1,2
7	Synchronous Counter using Flipflops	4	1,3,4,5,6,7,9,10,12/1,2
8	Asynchronous Counter using Flipflops	4	1,3,4,5,6,7,9,10,12/1,2
9	Realization of 8*1 Mux using 2*1 Mux	4	1,3,4,5,6,7,9,10,12/1,2
10	Design a 4-bit Comparator	2	1,2,3,4,5,6,7,8,9,10,11/1,2
11	Sequence Detector as a Finite State Machine	5	1,3,4,5,6,7,9,10,12/1,2

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Class Timetable

CLASS: II-B.Tech ECE-A **A.Y:2022-23** **SEMESTER: I** **LH: C-101**

TIME/ DAY	I 9:40-10:30	II 10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00-1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON	EDC	COI	EDC LAB / DSD LAB		LUNCH	DSD	NATL	SPORTS
TUE	PTSP	NATL	DSD	COI		EDC	SS	DSD(T)/SS(T)
WED	SS	PTSP	DSD LAB / BS LAB			DSD	SS(T)/EDC(T)	EDC
THU	NATL	PTSP	COI	EDC(T)/DSD(T)		SS	DSD	COUN
FRI	SS	EDC	COI	PTSP		LIB	CO-CU/DAA	
SAT	EDC	DSD	SS	NATL		PTSP	BS LAB / EDC LAB	

*(T) – Tutorial Concern Faculty

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the Faculty
EC301PC	EDC-Electronic Devices and Circuits	K.Rajender	EC306PC	EDC LAB - Electronic Devices and Circuits Lab	K.Rajender/B.Ashwini/M.Srilatha
EC302PC	NATL-Network Analysis and Transmission Lines	M.Nagaraju	EC307PC	DSD LAB - Digital System Design Lab	G.Anusha/T.Divya/P.Krishna Rao
EC303PC	DSD-Digital System Design	G.Anusha	EC308ES	BS LAB - Basic Simulation Lab	P.Rajendra/T.Naresh
EC304PC	SS-Signals and Systems	P.Rajendra	LIB	Library	B.Ashwini/Dr.K.Srinivasa Reddy
EC305ES	PTSP-Probability Theory and Stochastic Processes	T.Naresh	COUN	Counseling	K.Rajender/G.Anusha/G.Anitha
*MC309	COI-Constitution of India	S.Swapna	CO-CU/DAA	Co-Curricular/Dept.Assc.Act.	K.Rajender/T.Naresh/D.Aruna
			SPORTS	Sports	G.Anitha/P.Sumana

Class Incharge

Head of The Department

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Lab External Question paper

Year & Semester: II-I Branch: ECE

Subject Name: Digital System Design Lab Faculty Name:G.Anusha

S. No.	QUESTIONS
1.	Design a 4-bit Binary Adder/Subtractor
2.	Design and Realization of Logic Gates using Universal Gates.
3.	Design and Realization of Boolean Expression using Ligic Gates.
4.	Design and implement 4-bit Parallel Adder/ Subtractor using IC 7483.
5.	Realize (i) Mod-N Asynchronous Counter using IC7490 and (ii) Mod-N Synchronous counter using IC74192
6.	Design and implement (a) Full Adder using (i) basic logic gates and (ii) NAND gates. (b) Full subtractor using (i) basic logic gates and (ii) NANAD gates.
7.	Design and Realization of 4-bit Comparator.
8.	Design and Realization of Parallel -load Serial-out Shift register using Flipflops.
9.	Design and Realization of Asynchronous Counter using flipflops.
10.	Design and Realization of 8*1 Mux using 2*1
11.	Design and Realization of Sequence Detector as a Finite State Machine.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

B.Tech II ECE Regular Lab External Exams Timetable

A.Y: 2022-23 **SEM: I**

S. No.	Name of the Lab & Lab Number	Year/ Branch Section	Date & Time of the Lab Exam	Lab Internal Examiners Details
1	Electronic Devices and Circuits Lab (A-113)	II ECE-A	11.04.2023 (10:00 AM – 01:00 PM)	Mr. Rajender & Mrs. Nirmala
		II ECE-B	12.04.2023 (10:00 AM – 01:00 PM)	
2	Digital System Design Lab (A-313)	II ECE-A	12.04.2023 (10:00 AM – 01:00 PM)	Mrs. Anusha & Mrs. Srilatha
		II ECE-B	13.04.2023 (10:00 AM – 01:00 PM)	
3	Basic Simulation Lab (C-002)	II ECE-A	13.04.2023 (10:00 AM – 01:00 PM)	Mr. Naresh & Mrs. Alekhya
		II ECE-B	11.04.2023 (10:00 AM – 01:00 PM)	

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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

B.Tech II ECE Regular Lab External Examiners from TKREC

A.Y: 2022-23 **SEM: I**

S. No.	Name of the Lab & Lab No.	Year/ Branch Section	Date & Time of the Lab Exam	Lab Internal Examiners Details	Lab External Examiners Details
1	Electronic Devices and Circuits Lab(A-113)	II ECE-A	11.04.2023 (10:00 AM – 01:00 PM)	Mr. Rajender 8897756066	B. Sunitha
		II ECE-B	12.04.2023 (10:00 AM – 01:00 PM)		Dr.G. Sirisha
2	Digital System Design Lab (A-313)	II ECE-A	12.04.2023 (10:00 AM – 01:00 PM)	Mrs. Anusha 8639937510	V.Nageshwar Reddy
		II ECE-B	13.04.2023 (10:00 AM – 01:00 PM)		Lavanya
3	Basic Simulation Lab(C-002)	II ECE-A	13.04.2023 (10:00 AM – 01:00 PM)	Mr. Naresh 8919911324	Amulya
		II ECE-B	11.04.2023 (10:00 AM – 01:00 PM)		Y. Prathyusha

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Digital System Design Lab

LAB OCCUPANCY CHART

A.Y: 2022-23 **Year/Semester: II/I** **W.E.F. 28-11-2022** **Lab No: A-313**

Period/Day	1 9:30-10:30	2 10:30-11:20	3 11:20-12:10	4 12:10-01:00	 1:00-1:30	5 1:30-2:20	6 2:20-3:10	7 3:10-4:00
Monday					L U N C H	**DSD LAB II ECE-A**		
Tuesday						**DSD LAB II ECE-B**		
Wednesday						**DSD LAB II ECE-A**		
Thursday						**DSD LAB II ECE-B**		
Friday	**MAINTANINANCE**							
Saturday								

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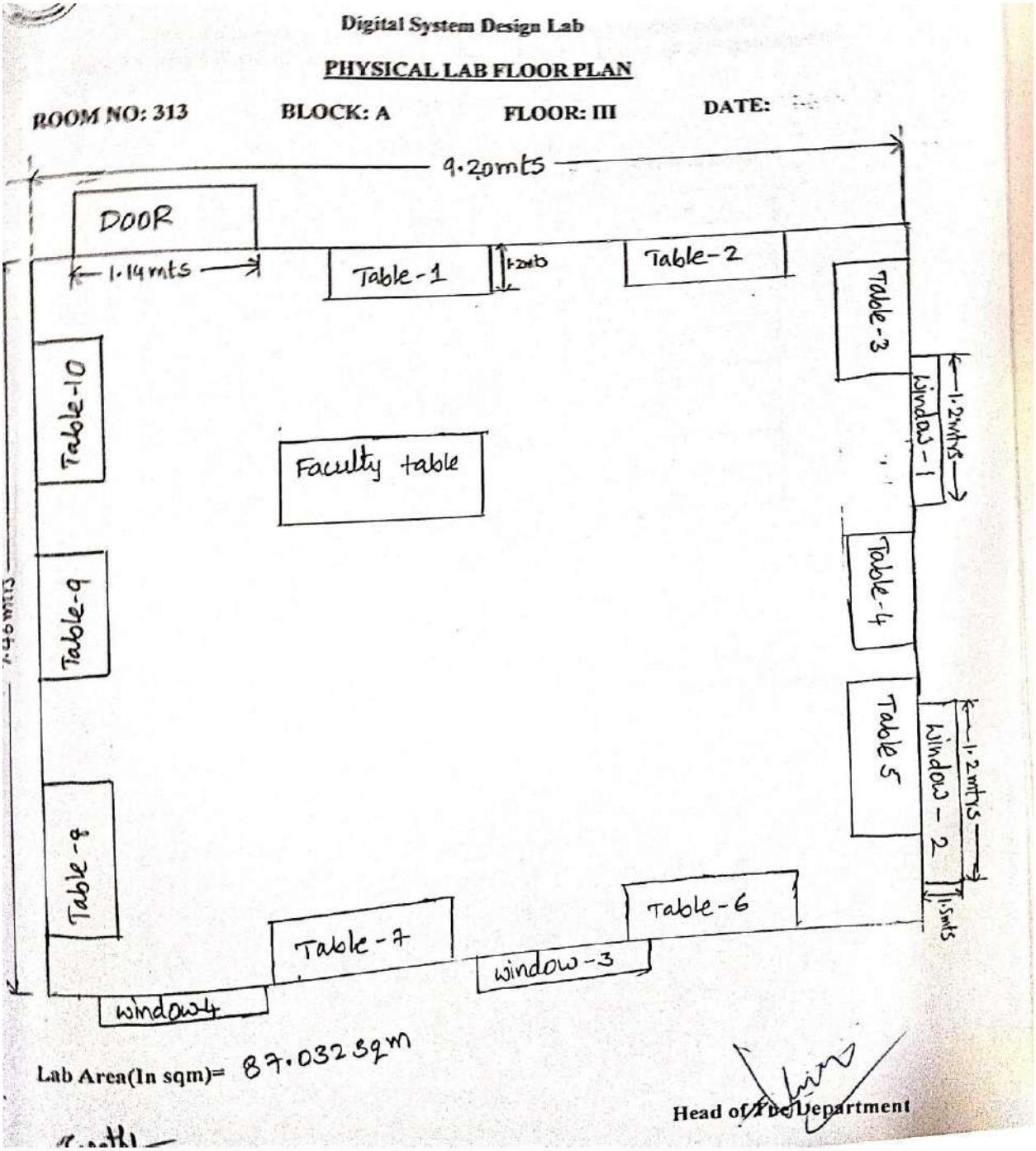
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Do's and Don'ts

- All students must observe the dress code while in the laboratory
- Foods, drinks and smoking are **NOT** allowed
- All bags must be left at the indicated place.
- The lab time table must be strictly followed.
- Be **PUNCTUAL** for your laboratory session.
- Experiment must be completed within the given time.
- Noise must be kept to minimum.
- Workspace must be kept clean and tidy at all time.
- Handle all apparatus with care.
- All students are liable for any damage to equipment due to their own negligence.
- All equipment, apparatus, tools and components must be **RETURNED** to their original place after use.
- Students are strictly **PROHIBITED** from taking out any items from the laboratory.
- Report immediately to the lab supervisor if any injury occurred.
- Report immediately to the lab supervisor if any damages to equipment.

BEFORE LIVING LAB

- Place the stools under the lab bench.
- Turn off the power to all instruments.
- Please check the laboratory notice board regularly for updates.



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DSD LAB MANUAL

CYCLE-1 LINKS

https://drive.google.com/file/d/1TXAlLfNi4G_k7b9ABRqsw00BOCpRQybc/view?usp=sharing

CYCLE-2 LINKS

https://drive.google.com/file/d/1nc337J3QIZQ4JOVgPl7xWdtyq5EGe1cb/view?usp=sharing

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty : G.Anusha
A.Y: 2022-23
Branch & Section: ECE - A
Examination I Internal
Course Name: DSD LAB
Year/Semester: II/I

S.No	HT No.	A+A+CD+MG	T+P+C+R	DDE
Max. Marks ==>		5	5	15
1	21X31A0401	3	3	14
2	21X31A0402	4	4	14
3	21X31A0403	2	2	14
4	21X31A0404	4	4	14
5	21X31A0405	4	3	14
6	21X31A0406	4	4	14
7	21X31A0407	3	4	13
8	21X31A0408	4	3	14
9	21X31A0409	4	3	13
10	21X31A0410	4	4	14
11	21X31A0412	4	3	14
12	21X31A0413	5	5	14
13	21X31A0414	3	3	14
14	21X31A0415	4	3	14
15	21X31A0416	2	2	13
16	21X31A0417	2	4	14
17	21X31A0418	4	4	14
19	21X31A0420	4	5	14
20	21X31A0421	3	4	13
21	21X31A0422	4	4	12
22	21X31A0423	4	3	14
23	21X31A0424	4	4	13
24	21X31A0425	4	3	14
25	21X31A0426	4	4	14
26	21X31A0427	4	5	14
27	21X31A0428	3	3	14
28	21X31A0429	4	3	14
29	21X31A0431	3	5	14
30	21X31A0432	4	5	14
31	21X31A0433	3	5	14
32	21X31A0434	5	5	14
33	21X31A0435	4	3	14
34	21X31A0436	1	2	10
35	21X31A0437	2	2	10
36	22X35A0401	4	4	14
37	22X35A0402	4	4	13
38	22X35A0403	4	4	14
39	22X35A0404	4	4	13
40	22X35A0405	4	4	14
41	22X35A0406	3	3	14

42	22X35A0407	4	4	13
43	22X35A0408	4	4	14
44	22X35A0409	3	3	14
45	22X35A0410	4	4	13
46	22X35A0411	4	4	14
47	22X35A0412	4	4	13
48	22X35A0413	3	3	12
49	22X35A0414	4	3	12
50	22X35A0415	4	4	14
51	22X35A0416	3	3	12
52	22X35A0417	4	4	14
53	22X35A0418	4	3	13
54	22X35A0419	4	3	14
55	22X35A0420	3	3	12
Target set by the faculty / HoD		3.00	3.00	9.00
Number of students performed above the target		49	50	54
Number of students attempted		54	54	54
Percentage of students scored more than target		91%	93%	100%

CO Mapping with Exam Questions:

CO - 1	Y	Y	Y
CO - 2	Y	Y	Y
CO - 3	Y	Y	Y
CO - 4	Y	Y	Y
CO - 5	Y	Y	Y
CO - 6	Y	Y	Y

% Students Scored >Target %	91%	93%	100%

CO Attainment based on Exam Questions:

CO - 1	91%	93%	100%
CO - 2	91%	93%	100%
CO - 3	91%	93%	100%
CO - 4	91%	93%	100%
CO - 5	91%	93%	100%
CO - 6	91%	93%	100%

CO	Intrnal practica	DDE	OveralI	Level
CO-1	92%	100%	96%	3.00
CO-2	92%	100%	96%	3.00
CO-3	92%	100%	96%	3.00
CO-4	92%	100%	96%	3.00
CO-5	92%	100%	96%	3.00
CO-6	92%	100%	96%	3.00

Attainment (Internal 1 Examination) = **3.00**

NOTE:

A+A+CD+MG : AIM+APPARATUS+CIRCUIT DIAGRAM+MODEL GRAPH

T+P+C+R : THEORY+PROCEDURE+CALCULATION+RESULT

DDE : Day to Day Evaluation

Attainment Level	
1	40%
2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-2)

Name of the faculty :	G.Anusha	A.Y:	2022-23
Branch & Section:	ECE - A	Examination	II Internal
Course Name:	DSD LAB	Year/Semester:	II/I

S.No	HT No.	A+A+CD+MG	T+P+C+R	DDE
Max. Marks ==>		5	5	15
1	21X31A0401	3	3	13
2	21X31A0402	4	4	13
3	21X31A0403	5	4	14
4	21X31A0404	4	4	14
5	21X31A0405	4	4	14
6	21X31A0406	4	4	13
7	21X31A0407	4	4	13
8	21X31A0408	4	4	14
9	21X31A0409	4	4	13
10	21X31A0410	4	4	14
11	21X31A0412	3	3	14
12	21X31A0413	4	4	14
13	21X31A0414	4	4	13
14	21X31A0415	3	3	14
15	21X31A0416	4	4	13
16	21X31A0417	4	4	14
17	21X31A0418	4	4	14
19	21X31A0420	4	4	14
20	21X31A0421	5	5	13
21	21X31A0422	4	4	13
22	21X31A0423	4	4	14
23	21X31A0424	5	5	13
24	21X31A0425	4	4	13
25	21X31A0426	3	3	14
26	21X31A0427	3	3	14
27	21X31A0428	3	3	14
28	21X31A0429	4	4	13
29	21X31A0431	3	3	14
30	21X31A0432	4	4	13
31	21X31A0433	3	3	14
32	21X31A0434	4	4	14
33	21X31A0435	4	4	14
34	21X31A0436	4	4	13
35	21X31A0437	4	4	14
36	22X35A0401	5	5	13
37	22X35A0402	4	4	13
38	22X35A0403	4	4	14
39	22X35A0404	4	4	13
40	22X35A0405	4	4	14
41	22X35A0406	3	3	14

42	22X35A0407	4	4	13
43	22X35A0408	4	4	14
44	22X35A0409	3	3	14
45	22X35A0410	4	4	13
46	22X35A0411	4	4	14
47	22X35A0412	3	4	14
48	22X35A0413	4	3	13
49	22X35A0414	4	3	14
50	22X35A0415	4	4	14
51	22X35A0416	3	3	14
52	22X35A0417	4	4	14
53	22X35A0418	4	4	13
54	22X35A0419	3	3	12
55	22X35A0420	3	3	12
Target set by the faculty / HoD		3.00	3.00	9.00
Number of students performed above the target		54	54	54
Number of students attempted		54	54	54
Percentage of students scored more than target		100%	100%	100%

CO Mapping with Exam Questions:

CO - 1	Y	Y	Y
CO - 2	Y	Y	Y
CO - 3	Y	Y	Y
CO - 4	Y	Y	Y
CO - 5	Y	Y	Y
CO - 6	Y	Y	Y

% Students Scored >Target %	100%	100%	100%

CO Attainment based on Exam Questions:

CO - 1	100%	100%	100%
CO - 2	100%	100%	100%
CO - 3	100%	100%	100%
CO - 4	100%	100%	100%
CO - 5	100%	100%	100%
CO - 6	100%	100%	100%

CO	Intrnal practica	DDE	OverallI	Level
CO-1	100%	100%	100%	3.00
CO-2	100%	100%	100%	3.00
CO-3	100%	100%	100%	3.00
CO-4	100%	100%	100%	3.00
CO-5	100%	100%	100%	3.00
CO-6	100%	100%	100%	3.00

Attainment (Internal 2 Examination) = **3.00**

NOTE:

A+A+CD+MG : AIM+APPARATUS+CIRCUIT DIAGRAM+MODEL GRAPH

T+P+C+R : THEORY+PROCEDURE+CALCULATION+RESULT

DDE : Day to Day Evaluation

Attainment Level	
1	40%
2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty : G.Anusha Academic Year: 2022-23

Branch & Section: ECE - A Year / Semester: II/I

Course Name: DSD LAB

S.No	Roll Number	Marks Secured
1	21X31A0401	60
2	21X31A0402	60
3	21X31A0403	61
4	21X31A0404	60
5	21X31A0405	60
6	21X31A0406	71
7	21X31A0407	65
8	21X31A0408	60
9	21X31A0409	63
10	21X31A0410	64
11	21X31A0412	62
12	21X31A0413	63
13	21X31A0414	60
14	21X31A0415	65
15	21X31A0416	63
16	21X31A0417	62
17	21X31A0418	65
19	21X31A0421	68
20	21X31A0422	60
21	21X31A0423	60
22	21X31A0424	68
23	21X31A0425	63
24	21X31A0426	64
25	21X31A0427	60
26	21X31A0428	70
27	21X31A0429	62
28	21X31A0431	71
29	21X31A0432	70
30	21X31A0433	65
31	21X31A0434	62
32	21X31A0435	71
33	21X31A0436	64
34	21X31A0437	63
35	22X35A0401	61
Max Marks		75

S.No	Roll Number	Marks Secured
36	22X35A0402	66
37	22X35A0403	62
38	22X35A0404	65
39	22X35A0405	65
40	22X35A0406	67
41	22X35A0407	71
42	22X35A0408	64
43	22X35A0409	63
44	22X35A0410	67
45	22X35A0411	71
46	22X35A0412	71
47	22X35A0413	70
48	22X35A0414	65
49	22X35A0415	70
50	22X35A0416	70
51	22X35A0417	68
52	22X35A0418	69
53	22X35A0419	66
54	22X35A0420	70

Class Average mark	64
Number of students performed above the	0

Attainment Level	% students
1	40%

Number of successful students	48
Percentage of students scored more than	0%
Attainment level	**1**

2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment

Name of the faculty: G.Anusha
Branch & Section: ECE - A
Course Name: DSD LAB

Academic Year: 2022-23
Examination: I Internal
Year: II
Semester: I

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00	3.00	3.00	3.00	3.00
CO2	3.00	3.00	3.00	3.00	3.00
CO3	3.00	3.00	3.00	3.00	3.00
CO4	3.00	3.00	3.00	3.00	3.00
CO5	3.00	3.00	3.00	3.00	3.00
CO6	3.00	3.00	3.00	3.00	3.00
Internal & University Attainment:			3.00	3.00	
Weightage			25%	75%	
Attainment for the course (Internal, Univers			0.75	2.25	
CO Attainment for the course (Direct Metho			3.00		

Overall course attainment level **3.00**

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Program Outcome Attainment (from Course)

Name of Faculty: G.Anusha
Academic Year: 2022-23
Branch & Section: ECE - A
Year: II
Course Name: DSD LAB
Semester: I

CO-PO mapping

PO /	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C217.1	3	2	-	-	3	2	2	-	2	-	-	3	3	3
C217.2	3	3	3	2	2	2	2	1	1	2	2	-	3	3
C217.3	3	2	3	3	2	2	2	1	1	2	-	2	3	3
C217.4	3	1	3	2	2	2	1	1	2	1	-	-	3	3
C217.5	3	-	3	2	2	1	1	-	1	2	-	2	3	3
C217.6	3	-	3	3	3	1	1	1	1	2	-	2	3	3
AVG	**3**	**2**	**2.5**	**2.5**	**2.5**	**2**	**2**	**1.5**	**2**	**2**	**2.00**	**2.33**	**3**	**3**

CO	**Course Outcome Attainment**
CO1	3.00
CO2	3.00
CO3	3.00
CO4	3.00
CO5	3.00
CO6	3.00
Overall course attainment level	**3.00**

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainment	**3**	**2**	**2**	**3.00**	**3.00**	**1.00**	**1.00**	**1.00**	**1.00**	**2.00**	**2.00**	**2.33**	**3**	**3.00**

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)