COURSE FILE

ON

e-CAD Lab

Course Code – EC605PC

III B.Tech II-SEMESTER

A.Y.: 2022-2023

Prepared by

Mrs. S. ALEKHYA
Assistant Professor

Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

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Sri Indu Institute of Engineering & Tech.
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Name of the Physical laboratory:	e-CAD LAB
Room No	C002
Name of the lab incharge	S.ALEKHYA
Name of the faculty incharge	S.ALEKHYA

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INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To Continuous assess of teaching-learning process through institute-industry collaboration.

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.

IM4: To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

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R.R. Dist. Telangana-501 510.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

DM1: To facilitate an academic environment that enables student's centric learning.

DM2: To provide state-of-the-art hardware and software technologies to meet industry requirements.

DM3: To continuously update the Academic and Research infrastructure.

DM4: To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

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PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

PEO1: Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.

PEO2: Graduates with ability to execute innovative ideas for Research and Development with continuous learning.

PEO3: Graduates inculcated with industry based soft-skills to enable employability.

PEO4: Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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PROGRAM OUTCOMES

1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

6. **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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Course Syllabus with Structure

R18 B.Tech. ECE Syllabus   **JNTU HYDERABAD**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech. IN ELECTRONICS AND COMMUNICATION ENGINEERING
COURSE STRUCTURE & SYLLABUS (R18)

Applicable From 2018-19 Admitted Batch

III YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC501PC	Microprocessors & Microcontrollers	3	1	0	4
2	EC502PC	Data Communications and Networks	3	1	0	4
3	EC503PC	Control Systems	3	1	0	4
4	SM504MS	Business Economics & Financial Analysis	3	0	0	3
5		Professional Elective - I	3	0	0	3
6	EC505PC	Microprocessors & Microcontrollers Lab	0	0	3	1.5
7	EC506PC	Data Communications and Networks Lab	0	0	3	1.5
8	EN508HS	Advanced Communication Skills Lab	0	0	2	1
9	*MC510	Intellectual Property Rights	3	0	0	0
		Total Credits	**18**	**3**	**8**	**22**

III YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC601PC	Antennas and Propagation	3	1	0	4
2	EC602PC	Digital Signal Processing	3	1	0	4
3	EC603PC	VLSI Design	3	1	0	4
4		Professional Elective - II	3	0	0	3
5		Open Elective - I	3	0	0	3
6	EC604PC	Digital Signal Processing Lab	0	0	3	1.5
7	EC605PC	e – CAD Lab	0	0	3	1.5
8	EC606PC	Scripting Languages Lab	0	0	2	1
9	*MC609	Environmental Science	3	0	0	0
		Total Credits	**18**	**3**	**8**	**22**

EC605PC: e- CADLAB

B.Tech. III Year II Semester
        L   T   P   C

        0   0   3   1.5

Note: Any **SIX of** the following experiments from each part are to be conducted (Total 12)

Part -I
All the following experiments have to be implemented using HDL

1. Realize all the logic gates
2. Design of 8-to-3encoder(without and with priority)and2-to-4decoder
3. Design of 8-to-1multiplexer and 1-to-8demultiplexer
4. Design of 4bit binary to gray code converter
5. Designof4bitcomparator
6. Design of Full adder using3modelingstyles
7. Design of flip flops :SR,D,JK,T
8. Designof4-bitbinary,BCDcounters(synchronous/asynchronousreset)oranysequencecounter
9. Finite State Machine Design

Part-II
Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and cross talk analysis for the following:

1. Basic logic gates
2. CMOS inverter
3. CMOS NOR/NAND gates
4. CMOS XOR and MUX gates
5. Static/Dynamic logic circuit(register cell)
6. Latch
7. Pass transistor
8. Layout of any combinational circuit (complex CMOS logic gate).

CO, PO,PSO'S MAPPING

A.Y: 2022-23   **SEMESTER: II**   **CLASS: III ECE-A**

Course Outcomes After completing this course, the student will be able to:
C327.1: To learn the HDL programming language. (Knowledge)
C327.2: To learn the simulation of basic gates using the HDL programming language.
    (Application)
C327.3: To learn the simulation of combinational circuits using programming language.
     (Application)
C327.4: To learn the simulation of sequential circuits using programming language.
    (Application)
C327.5: To learn the synthesis and layouts of analog and digital CMOS circuits.
     (Synthesis)
C327.6: To develop an ability to simulate and synthesize various digital circuits. (Synthesis)

Mapping of course outcomes with program outcomes:

High -3   Medium -2   Low-1

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C327.1	3	3	3	3	3	-	-	-	2	2	2	3	3	3
C327.2	3	3	3	3	3	-	-	-	2	2	2	3	3	3
C416.3	3	3	3	3	3	-	-	-	2	2	2	3	3	3
C327.4	3	3	3	3	3	-	-	-	2	2	2	3	3	3
C327.5	3	3	3	3	3	-	-	-	2	2	2	3	3	3
C327.6	3	3	3	3	3	-	-	-	2	2	2	3	3	3
C327	3	3	3	3	3	-	-	-	2	2	2	3	3	3

LIST OF EXPERIMENTS AND THEIR CO, PO, PSO MAPPING

S.No	Name of The Experiment	CO	PO	PSO
1	HDL code to realize all the logic gates.	2	12,3,4,5,9,10,11,12	1,2
2	Design of 2-to-4 decoder	3	12,3,4,5,9,10,11,12	1,2
3	Design of 8-to-3 encoder (without and with priority)	3	12,3,4,5,9,10,11,12	1,2
4	Design of 8-to-1 multiplexer and 1-to-8 de multiplexer	3	12,3,4,5,9,10,11,12	1,2
5	Design of 4 bit binary to gray code converter	3	12,3,4,5,9,10,11,12	1,2
6	Design of 4 bit comparator	3	12,3,4,5,9,10,11,12	1,2
7	Layout Design of Basic logic gates	2	12,3,4,5, 9,10,11,12	1,2
8	CMOS inverter	5	12,3,4,5,9,10,11,12	1,2
9	CMOS NOR gates	5	12,3,4,5,9,10,11,12	1,2
10	CMOS XOR and MUX gates	5	12,3,4,5,9,10,11,12	1,2
11	Complex CMOS Logic Gates	6	12,3,4,5,9,10,11,12	1,2
12	CMOS NAND gates	6	12,3,4,5,9,10,11,12	1,2

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Class Timetable

CLASS: III-B.Tech ECE-A   A.Y:2022-23   SEMESTER: II   LH: C-201

TIME/ DAY	I 9:40-10:30	II 10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00-1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON	A&P	DSP LAB / e-CAD LAB			L U N C H	VLSID	ESD	LIB
TUE	IM	DSP	FAI	ESD		DSP(T)/VLSID(T)	A&P	SPORTS
WED	ESD	IM	A&P	A&P(T)/DSP(T)		FAI	DSP	COUN
THU	IM	DSP	VLSID	VLSID(T)/A&P(T)		e-CAD LAB / DSP LAB		
FRI	FAI	DSP	A&P	VLSID		ESD		CO-CU/DAA
SAT	VLSID	ESD	VLSID(ADJUNCT)			SL LAB		A&P

*(T) – Tutorial Concern Faculty

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the Faculty
EC601PC	A&P-Antennas and Propagation	P.Krishna Rao	EC604PC	DSP LAB-Digital Signal Processing Lab	Y.Raju/Dr.T.Ramakrishna/ Dr.S.Anjaneyulu
EC602PC	DSP-Digital Signal Processing	Y.Raju	EC605PC	e-CAD LAB-e – CAD Lab	S.Alekhya/P.Rajendra/P.Krishna
EC603PC	VLSID-VLSI Design	S.Alekhya	EC606PC	SL LAB-Scripting Languages Lab	D.Nagaraju/.Krishna Rao/ K.Bhaskar Reddy
EC613PE	ESD-Embedded System Design(Professional Elective-II)	A.Vaani	-	FAI-Fundamentals of Artificaial Intelligence	P.Meena
VLSID (ADJUNCT)	VLSID(ADJUNCT)	G.Chandrasekhar	COUN	Counseling	Y.Raju/K.Padma/G.Swathi
MT600OE	IM-Industrial Management (Open Elective-I)	K.V.Nagamani	SPORTS	Sports	P.Srilatha/B.Ashwini
			CO-CU/DAA	Co-Curricular/Dept. Assoc.Activities	S.Alekhya/S.Naresh/K.Bhaskar Reddy
			LIB	Library	G.Nirmala/A.Swetha

Class Incharge

Head of The Department
Head of the Department
Electronics and Communication Engg. Dept
INSTITUTE OF ENGG & TECH..

Principal PRINCIPAL
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R.R. Dist. Telangana -501 510

MODEL PRACTICAL END EXAMINATION QUESTIONS

1. Write an HDL code to realize all the logic gates.

2. Draw Layout diagram for CMOS NOR gate.

3. Design of 2-to-4 decoder using Xilinx software.

4. Design Layout diagram for all the Basic logic gates using cadence tools.

5. Design of 8-to-3 encoder (without and with priority) using Xilinx software.

6. Draw Layout diagram for CMOS XOR gate.

7. Design of 8-to-1 multiplexer using Xilinx software.

8. Design 1-to-8 de multiplexer using Xilinx software.

9. Draw Layout diagram for CMOS inverter

10. Design of 4 bit binary to gray code converter using Xilinx software.

11. Draw Layout diagram for CMOS NAND gate.

12. Design of 4 bit comparator using Xilinx software.

13. Draw Layout diagram for MUX gates.

14. Draw Layout diagram for Pass transistor

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

III ECE Regular Lab External Exams Timetable

A.Y: 2022-23　　　　　　　　　　　　　　　　　　　　**SEM: II**

S.No.	Name of the Lab	Year/Sec	Date & Time of the Lab Exam	Name of the Lab Internal Examiners
1	Digital Signal Processing Lab	III ECE-A	03.07.2023(FN)	Mr.T.Naresh
		III ECE-B	04.07.2023(FN)	Mr.T.Naresh
		III ECE-C	05.07.2023(FN)	Mr.T.Naresh
2	e-CAD Lab	III ECE-A	04.07.2023(FN)	Mrs.S.Alekhya
		III ECE-B	05.07.2023(FN)	Mr.K.Srikanth
		III ECE-C	03.07.2023(FN)	Mrs.S.Alekhya
3	Scripting Languages Lab	III ECE-A	05.07.2023(FN)	Mr.M.Sagar
		III ECE-B	03.07.2023(FN)	Mr.K.Anup Kumar
		III ECE-C	04.07.2023(FN)	Mr.D.Nagaraju
4	Computer Vision Lab	III CSE(IOT)	03.07.2023(FN)	Mr.K.Srikanth
5	IoT Lab	III CSE(IOT)	04.07.2023(FN)	Mr.I.Venu

Timings: - FN: 10:00 AM To 01:00 PM

Head of the Department

HOD/ECE

Electronics and Communication Engg Dept

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

III ECE Regular Lab External Examiners from GNITC

A.Y: 2022-23   SEM: II

S.No.	Name of the Lab	Year/ Sec	Date & Time of the Lab Exam	Name of the Lab Internal Examiners	Name of the Lab External Examiner & Contact Details
1	Digital Signal Processing Lab	III ECE-A	03.07.2023	Mr.T.Naresh	Mr.M. Ravinder Asst Prof 9491108268
		III ECE-B	04.07.2023	Mr.T.Naresh	Mr.D Naresh Asst Prof 9885248584
		III ECE-C	05.07.2023	Mr.T.Naresh	Dr.Md.Rashid Mahmood Prof 9999254431
2	e-CAD Lab	III ECE-A	04.07.2023	Mrs.S.Alekhya	Prof.A Mohan Prof 9989298588
		III ECE-B	05.07.2023	Mr.K.Srikanth	Dr. B. Mythily Devi Asst Prof 8985858946
		III ECE-C	03.07.2023	Mrs.S.Alekhya	Mr.ChNarasimhulu Asst Prof 9849825884
3	Computer Vision Lab	III CSE (IOT)	03.07.2023	Mr.K.Srikanth	Mr NVS. Murthy Asst Prof 9701196375
4	IoT Lab	III CSE (IOT)	04.07.2023	Mr.I.Venu	Mr D .Surendra Rao Assoc Prof 9849935889

HOD

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LAB OCUPANCY CHART

CLASS: III-II B.Tech ECE-A, B,C   **A.Y:2022-23**

TIME/ DAY	I 9:30-10:30	II 10:30 - 11:20	III 11:20-12:10	IV 12:10-1:00	1:00-1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON		e-CAD LAB-A SEC				e-CAD LAB-C SEC		
TUE						e-CAD LAB-B SEC		
WED					LUNCH			
THU						e-CAD LAB-A SEC		
FRI						e-CAD LAB-B SEC		
SAT						e-CAD LAB-C SEC		

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DOS AND DON'TS

- All students must observe the dress code while in the laboratory
- Foods, drinks and smoking are NOT allowed
- All bags must be left at the indicated place.
- The lab time table must be strictly followed.
- Be PUNCTUAL for your laboratory session.
- Experiment must be completed within the given time.
- Noise must be kept to minimum.
- Workspace must be kept clean and tidy at all time.
- Handle all apparatus with care.
- All students are liable for any damage to equipment due to their own negligence.
- All equipment,apparatus,tools and components must be RETURNED to their original place after use.
- Students are strictly PROHIBITED from taking out any items from the laboratory.
- Report immediately to the lab supervisor if any injury occurred.
- Report immediately to the lab supervisor if any damages to equipment.

BEFORE LEAVING LAB
- Place the stools under the lab bench.
- Turn off the power to all instruments.
- Please check the laboratory notice board regularly for updates.

PHYSICAL LAB FLOOR PLAN WITH AREA IN SQ.M

ROOM NO: C002   A.Y-2022-23   YEAR/SEM-III-II

Lab Area(In sqm)= 16 × 9.6 = 153.6

Lab In-charge

Head of The Department
Electronics and Communication Engg. Dept.
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e-CAD LAB

Lab Manual Link

https://drive.google.com/file/d/1a1ywX1qBlpiwv8uYH_l6DOR74VsrOGY0/view?usp=sharing

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty : S.ALEKHYA   A.Y: 2022-23

Branch & Section: ECE - A   Examination I Internal

Course Name: E-CAD LAB   Year/Sem III/II

S.No	HT No.	A+A+CD+MC	T+P+C+R	DDE
Max. Marks ==>		**5**	**5**	**15**
1	20X31A0401	4	4	13
2	20X31A0402	4	5	14
3	20X31A0403	2	2	10
4	20X31A0404	4	4	14
5	20X31A0405	4	4	14
6	20X31A0406	4	4	10
7	20X31A0407	4	4	12
8	20X31A0408	4	4	10
9	20X31A0409	5	5	14
10	20X31A0410	4	3	12
11	20X31A0411	5	4	11
12	20X31A0412	4	4	10
13	20X31A0413	4	4	10
14	20X31A0414	4	5	11
15	20X31A0415	5	4	15
16	20X31A0416	5	4	11
17	20X31A0417	4	4	14
19	20X31A0418	2	2	10
20	20X31A0419	4	4	10
21	20X31A0420	4	4	10
22	20X31A0421	5	5	12
23	20X31A0422	4	5	12
24	20X31A0423	4	4	10
25	20X31A0424	4	4	11
26	20X31A0425	4	4	10
27	20X31A0426	5	4	12
28	20X31A0427	4	4	10
29	20X31A0428	4	4	10
30	20X31A0429	4	4	12
31	20X31A0430	4	4	14
32	20X31A0431	4	4	10
33	20X31A0432	4	4	14
34	20X31A0433	4	4	12
35	20X31A0434	4	4	14
36	20X31A0435	4	4	10
37	20X31A0436	4	4	9
38	20X31A0437	4	4	14
39	20X31A0438	4	4	14
40	20X31A0439	4	5	11
41	20X31A0440	4	4	10
42	20X31A0441	4	4	10
43	20X31A0442	4	4	14

44	20X31A0444	4	4	14
45	20X31A0445	4	5	11
46	20X31A0446	5	4	12
47	20X31A0447	4	4	14
48	20X31A0448	4	5	10
49	20X31A0449	4	5	15
50	20X31A0450	2	3	13
51	20X31A0451	4	4	14
52	20X31A0452	5	4	15
53	20X31A0453	5	4	12
54	20X31A0454	2	2	10
55	20X31A0455	4	4	10
56	20X31A0456	4	4	10
57	20X31A0458	4	4	12
58	20X31A0459	5	4	15
59	20X31A0460	4	4	10
60	20X31A0461	5	4	13
61	20X31A0462	4	4	10
Target set by the faculty / HoD		3.00	3.00	9.00
Number of students performed above the target		56	57	60
Number of students attempted		60	60	60
Percentage of students scored more than target		93%	95%	100%

CO Mapping with Exam Questions:

CO - 1	Y	Y	Y
CO - 2	Y	Y	Y
CO - 3	Y	Y	Y
CO - 4			
CO - 5			
CO - 6			

% Students Scored >Target %	93%	95%	100%

CO Attainment based on Exam Questions:

CO - 1	93%	95%	100%
CO - 2	93%	95%	100%
CO - 3	93%	95%	100%
CO - 4			
CO - 5			
CO - 6			

CO	Intrnal prac	DDE	OveralI	Level
CO-1	94%	100%	97%	3.00
CO-2	94%	100%	97%	3.00
CO-3	94%	100%	97%	3.00
CO-4				
CO-5				
CO-6				

Attainment L	
1	40%
2	50%
3	60%

Attainment (Internal 1 Examination) =   **3.00**

NOTE:

A+A+CD+MG : AIM+APPARATUS+CIRCUIT DIAGRAM+MODEL GRAPH

T+P+C+R : THEORY+PROCEDURE+CALCULATION+RESULT

DDE : Day to Day Evaluation

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-2)

Name of the faculty : S.ALEKHYA A.Y: 2022-23

Branch & Section: ECE - A Examination II Internal

Course Name: E-CAD LAB Year/Semeste III/II

S.No	HT No.	A+A+CD+MG	T+P+C+R	DDE
Max. Marks ==>		5	5	15
1	20X31A0401	4	4	13
2	20X31A0402	4	5	14
3	20X31A0403	2	2	10
4	20X31A0404	4	4	14
5	20X31A0405	4	4	14
6	20X31A0406	4	4	10
7	20X31A0407	4	4	12
8	20X31A0408	4	4	10
9	20X31A0409	5	5	14
10	20X31A0410	4	3	12
11	20X31A0411	5	4	11
12	20X31A0412	4	4	10
13	20X31A0413	4	4	10
14	20X31A0414	4	5	11
15	20X31A0415	5	4	15
16	20X31A0416	5	4	11
17	20X31A0417	4	4	14
19	20X31A0418	2	2	10
20	20X31A0419	4	4	10
21	20X31A0420	4	4	10
22	20X31A0421	5	5	12
23	20X31A0422	4	5	12
24	20X31A0423	4	4	10
25	20X31A0424	4	4	11
26	20X31A0425	4	4	10
27	20X31A0426	5	4	12
28	20X31A0427	4	4	10
29	20X31A0428	4	4	10
30	20X31A0429	4	4	12
31	20X31A0430	4	4	14
32	20X31A0431	4	4	10
33	20X31A0432	4	4	14
34	20X31A0433	4	4	12
35	20X31A0434	4	4	14
36	20X31A0435	4	4	10
37	20X31A0436	4	4	9
38	20X31A0437	4	4	14
39	20X31A0438	4	4	14
40	20X31A0439	4	5	11
41	20X31A0440	4	4	10
42	20X31A0441	4	4	10
43	20X31A0442	4	4	14

44	20X31A0444	4	4	14
45	20X31A0445	4	5	11
46	20X31A0446	5	4	12
47	20X31A0447	4	4	14
48	20X31A0448	4	5	10
49	20X31A0449	4	5	15
50	20X31A0450	2	3	13
51	20X31A0451	4	4	14
52	20X31A0452	5	4	15
53	20X31A0453	5	4	12
54	20X31A0454	2	2	10
55	20X31A0455	4	4	10
56	20X31A0456	4	4	10
57	20X31A0458	4	4	12
58	20X31A0459	5	4	15
59	20X31A0460	4	4	10
60	20X31A0461	5	4	13
61	20X31A0462	4	4	10
Target set by the faculty / HoD		3.00	3.00	9.00
Number of students performed above the target		56	57	60
Number of students attempted		60	60	60
Percentage of students scored more than target		93%	95%	100%

CO Mapping with Exam Questions:

CO - 1			
CO - 2			
CO - 3			
CO - 4	Y	Y	Y
CO - 5	Y	Y	Y
CO - 6	Y	Y	Y

% Students Scored >Target %	93%	95%	100%

CO Attainment based on Exam Questions:

CO - 1			
CO - 2			
CO - 3			
CO - 4	93%	95%	100%
CO - 5	93%	95%	100%
CO - 6	93%	95%	100%

CO	Intrnal practica	DDE	OveralI	Level
CO-1				
CO-2				
CO-3				
CO-4	94%	100%	97%	3.00
CO-5	94%	100%	97%	3.00

Attainment Le	
1	40%
2	50%
3	60%

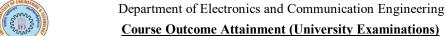| CO-6	94%	100%	97%	3.00

Attainment (Internal 2 Examination) = **3.00**

NOTE:

A+A+CD+MG : AIM+APPARATUS+CIRCUIT DIAGRAM+MODEL GRAPH

T+P+C+R : THEORY+PROCEDURE+CALCULATION+RESULT

DDE : Day to Day Evaluation

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty :	S.ALEKHYA	Academic Year:	2022-23
Branch & Section:	ECE - A	Year / Semester:	III/II
Course Name:	E-CAD LAB		

S.No	Roll Number	Marks Secured	S.No	Roll Number	Marks Secured
1	20X31A0401	63	36	20X31A0435	64
2	20X31A0402	68	37	20X31A0436	63
3	20X31A0403	-1	38	20X31A0437	67
4	20X31A0404	67	39	20X31A0438	73
5	20X31A0405	70	40	20X31A0439	70
6	20X31A0406	64	41	20X31A0440	64
7	20X31A0407	66	42	20X31A0441	64
8	20X31A0408	64	43	20X31A0442	71
9	20X31A0409	73	44	20X31A0444	70
10	20X31A0410	65	45	20X31A0445	65
11	20X31A0411	66	46	20X31A0446	66
12	20X31A0412	64	47	20X31A0447	67
13	20X31A0413	64	48	20X31A0448	62
14	20X31A0414	66	49	20X31A0449	73
15	20X31A0415	73	50	20X31A0450	64
16	20X31A0416	65	51	20X31A0451	68
17	20X31A0417	68	52	20X31A0452	73
19	20X31A0418	-1	53	20X31A0453	68
20	20X31A0419	64	54	20X31A0454	-1
21	20X31A0420	64	55	20X31A0455	64
22	20X31A0421	68	56	20X31A0456	64
23	20X31A0422	71	57	20X31A0458	66
24	20X31A0423	64	58	20X31A0459	73
25	20X31A0424	65	59	20X31A0460	64
26	20X31A0425	64	60	20X31A0461	68
27	20X31A0426	71	61	20X31A0462	64
28	20X31A0427	64			
29	20X31A0428	64			
30	20X31A0429	66			
31	20X31A0430	67			
32	20X31A0431	64			
33	20X31A0432	69			
34	20X31A0433	66			
35	20X31A0434	71			

Max Marks	75	
Class Average mark	64	
Number of students performed above the target	43	
Number of successful students	48	

Attainment Level	% students
1	40%
2	50%

Percentage of students scored more than target	90%		3	60%
Attainment level	**3**			

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment

Name of the faculty : S.ALEKHYA   Academic Year: 2022-23

Branch & Section: ECE - A   Examination: I Internal

Course Name: E-CAD lab   Year: III

     Semester: II

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00	3.00	3.00	3.00	3.00
CO2	3.00	3.00	3.00	3.00	3.00
CO3	3.00	3.00	3.00	3.00	3.00
CO4		3.00	3.00	3.00	3.00
CO5		3.00	3.00	3.00	3.00
CO6		3.00	3.00	3.00	3.00
Internal & University Attainment:			3.00	3.00	
Weightage			25%	75%	
CO Attainment for the course (Internal, University			0.75	2.25	
CO Attainment for the course (Direct Method)			3.00		

Overall course attainment level   **3.00**

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering
Program Outcome Attainment (from Course)

Name of Faculty: S.ALEKHYA   Academic Year: 2022-23

Branch & Section: ECE - A   Year: III

Course Name: E-CAD LAB   Semester: II

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	3	-	-	-	2	2	2	3	3	3
CO2	3	3	3	3	3	-	-	-	2	2	2	3	3	3
CO3	3	3	3	3	3	-	-	-	2	2	2	3	3	3
CO4	3	3	3	3	3	-	-	-	2	2	2	3	3	3
CO5	3	3	3	3	3	-	-	-	2	2	2	3	3	3
CO6	3	3	3	3	3	-	-	-	2	2	2	3	3	3
Course	3.00	3.00	3.00	3.00	3.00	-	-	-	2.00	2.00	2.00	3.00	3.00	3.00

CO	Course Outcome Attainment
CO1	3.00
CO2	3.00
CO3	3.00
CO4	3.00
CO5	3.00
CO6	3.00
Overall course attainment level	**3.00**

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainment	3.00	3.00	3.00	3.00	3.00	-	-	-	2.00	2.00	2.00	3.00	3.00	3.00

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)