



**Sri Indu Institute of  
Engineering & Technology**

Recognized Under 2(f) of UGC Act 1956  
Approved by AICTE, New Delhi  
Affiliated to JNTUH, Hyderabad.

# **COURSE FILE**

**ON**

## **ELECTRONIC CIRCUIT ANALYSIS LAB**

**Course Code- EC408PC**

**II B.Tech II-SEMESTER**

**A.Y.:2022-2023**

**Prepared by**

**Mrs.G.Nirmala**  
**Assistant Professor**

**Head of the Department**  
Electronics and Communication Engg. Dept  
SRI INDU INSTITUTE OF ENGG & TECH  
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

**PRINCIPAL**  
Sri Indu Institute of Engineering & Tech.  
Sheriguda(VIII), Ibrahimpatnam  
R.R. Dist. Telangana-501 510.



## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year	2022-2023
Course Title	ELECTRONIC CIRCUIT ANALYSIS LAB
Course Code	EC408PC
Programme	B.Tech
Year & Semester	II year II-semester
Room Number	A-114
Name of the lab incharge	Mr.K.Rajender
Name of the faculty incharge	Mrs.G.Nirmala

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# Sri Indu Institute of Engineering & Technology

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## INSTITUTE VISION AND MISSION

### Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

### Mission:

- IM1:** To offer outcome-based education and enhancement of technical and practical skills.
- IM2:** To Continuous assess of teaching-learning process through institute-industry collaboration.
- IM3:** To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.
- IM4:** To Create an enterprising environment to ensure culture, ethics and social responsibility among the stake holders.

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### DEPARTMENT VISION AND MISSION

#### Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

#### Mission:

- DM1 :** To facilitate an academic environment that enables student's centric learning.
- DM2 :** To provide state-of-the-art hardware and software technologies to meet industry requirements.
- DM3 :** To continuously update the Academic and Research infrastructure.
- DM4 :** To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

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## PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

- PEO1:** Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.
- PEO2:** Graduates with ability to execute innovative ideas for Research and Development with continuous learning.
- PEO3:** Graduates inculcated with industry based soft-skills to enable employability.
- PEO4:** Graduates demonstrate with ability to work in inter disciplinary teams and ethical professional behavior.

## PROGRAM SPECIFIC OUTCOMES

- PSO 1: Design Skills:** Design, analysis and development a economical system in the area of Embedded system & VLSI design.
- PSO2: Software Usage:** Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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## PROGRAM OUTCOMES

1. **ENGINEERING KNOWLEDGE:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **PROBLEM ANALYSIS:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **DESIGN/DEVELOPMENT OF SOLUTIONS:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **MODERN TOOL USAGE:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6. **THE ENGINEER AND SOCIETY:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **ENVIRONMENT AND SUSTAINABILITY:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **ETHICS:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **INDIVIDUAL AND TEAM WORK:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **COMMUNICATION:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.
11. **PROJECT MANAGEMENT AND FINANCE:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **LIFE-LONG LEARNING:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**B.tech. in ELECTRONICS AND COMMUNICATION ENGINEERING**  
**II YEAR COURSE STRUCTURE AND SYLLABUS (R18)**  
 Applicable From 2018-19Admitted Batch

**II YEAR I SEMESTER**

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC301PC	Electronic Devices and Circuits	3	1	0	4
2	EC302PC	Network Analysis and Transmission Lines	3	0	0	3
3	EC303PC	Digital System Design	3	1	0	4
4	EC304PC	Signals and Systems	3	1	0	4
5	EC305PC	Probability Theory and Stochastic Processes	3	0	0	3
6	EC306PC	Electronic Devices and Circuits Lab	0	0	2	1
7	EC307PC	Digital System Design lab	0	0	2	1
8	EC308PC	Basic simulation Lab	0	0	2	1
9	*MC309	Constitution of India	3	0	0	0
		<b>Total Credits</b>	<b>18</b>	<b>3</b>	<b>6</b>	<b>21</b>

**II YEAR II SEMESTER**

S. No.	Course Code	Course Title	L	T	P	Credits
1	MA401BS	Laplace Transforms, Numerical Methods & Complex Variables	3	1	0	4
2	EC402PC	Electromagnetic Fields and Waves	3	0	0	3
3	EC403PC	Analog and Digital Communications	3	1	0	4
4	EC404PC	Linear IC Applications	3	0	0	3
5	EC405PC	Electronic Circuit Analysis	3	0	0	3
6	EC406PC	Analog and Digital Communications Lab	0	0	3	1.5
7	EC407PC	IC Applications Lab	0	0	3	1.5
8	EC408PC	Electronic Circuit Analysis Lab	0	0	2	1
9	*MC409	Gender Sensitization Lab	0	0	2	0
		<b>Total Credits</b>	<b>15</b>	<b>2</b>	<b>10</b>	<b>21</b>

\*MC-Satisfactory/Unsatisfactory

## EC408PC: ELECTRONIC CIRCUIT ANALYSIS LAB

B.Tech. II Year II Sem.

<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>0</b>	<b>0</b>	<b>2</b>	<b>1</b>

**Note:**

- Experiments marked with \* has to be designed, simulated and verified in hardware.
- Minimum of 9 experiments to be done in hardware.

**Hardware Testing in Laboratory:**

1. Common Emitter Amplifier (\*)
2. Two Stage RC Coupled Amplifier
3. Cascode amplifier Circuit (\*)
4. Darlington Pair Circuit
5. Current Shunt Feedback amplifier Circuit
6. Voltage Series Feedback amplifier Circuit (\*)
7. RC Phase shift Oscillator Circuit (\*)
8. Hartley and Colpitt's Oscillators Circuit
9. Class A power amplifier
10. Class B Complementary symmetry amplifier (\*)
11. Design a Mono stable Multivibrator
12. The output voltage waveform of Miller Sweep Circuit

**Major Equipments required for Laboratories:**

1. Computer System with latest specifications connected
2. Window XP or equivalent
3. Simulation software-Multisim or any equivalent simulation software
4. Regulated Power Suppliers, 0-30V
5. 20 MHz, Dual Channel Cathode Ray Oscilloscopes.
6. Functions Generators-Sine and Square wave signals
7. Multimeters
8. Electronic Components





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Course: Electronic Circuit Analysis Lab (C228)

Class: II ECE-A Course Outcomes

After completing this course the student will be able to:

CO Number	Course Outcomes	Bloom's Taxonomy
C228.1	Design and simulate different BJT amplifiers: CE amplifier, Two stage RC coupled amplifier, Cascode, Darlington pair.	Comprehensive, Understand
C228.2	Design and simulate feedback amplifiers: Current shunt feedback amplifier, Voltage series feedback amplifiers.	Creative , comprehensive
C228.3	Design and simulate different oscillators: RC phase shift oscillator, Hartley and colpitt's oscillators.	Creative
C228.4	Design and simulate power amplifiers: Class A power amplifier, Class B complementary symmetry amplifier.	Comprehensive
C228.5	Design Monostable Multivibrator.	Comprehensive, Understand
C228.6	Design Miller sweep circuit.	Applying , Analyzing

### Mapping of course outcomes with program outcomes:

High-3      Medium-2      Low-1

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C228.1	3	3	2	2	-	-	-	-	-	-	-	-	3	3
C228.2	2	3	2	2	-	-	-	-	-	-	2	-	2	2
C228.3	2	3	2	2	-	-	-	-	-	-	-	3	3	3
C228.4	1	3	2	2	-	-	-	-	-	-	2	-	3	3
C228.5	3	2	1	2	-	-	-	-	-	-	-	3	2	2
C228.6	2	3	2	-	-	-	-	-	-	-	-	-	1	1
AVG	2.17	2.83	1.83	2.00	-	-	-	-	-	-	2	3	2.33	2.33



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## LIST OF EXPERIMENTS AND THEIR CO, PO/PSO MAPPING

S.No	Name of The Experiment	CO	PO/PSO
1	Common Emitter Amplifier.	1	PO1,PO2,PO3,PO4, PSO1,PSO2
2	Two Stage RC Coupled Amplifier.	1	PO1,PO2,PO3,PO4, PSO1,PSO2
3	Cascode amplifier Circuit.	1	PO1,PO2,PO3,PO4, PSO1,PSO2
4	Darlington Pair Circuit.	1	PO1,PO2,PO3,PO4, PSO1,PSO2
5	Current Shunt Feedback amplifier Circuit	2	PO1,PO2,PO3,PO4,PO11, PSO1,PSO2
6	Voltage Series Feedback amplifier Circuit.	2	PO1,PO2,PO3,PO4,PO11, PSO1,PSO2
7	RC Phase shift Oscillator Circuit.	3	PO1,PO2,PO3,PO4,PO12, PSO1,PSO2
8	Hartley and Colpitt's Oscillators Circuit	3	PO1,PO2,PO3,PO4,PO12, PSO1,PSO2
9	Class A power amplifier.	4	PO1,PO2,PO3,PO4,PO11, PSO1,PSO2
10	Class B Complementary symmetry amplifier.	4	PO1,PO2,PO3,PO4,PO11, PSO1,PSO2
11	Design a Monostable Multivibrator.	5	PO1,PO2,PO3,PO4,PO12, PSO1,PSO2
12	The output voltage waveform of Miller Sweep Circuit.	6	PO1,PO2,PO3, PSO1,PSO2



**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**  
**Class Timetable**

CLASS: II-B.Tech ECE-A

A.Y:2022-23

SEMESTER: II

LH: C-101

TIME/ DAY	I 9:40-10:30	II 10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00- 1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON	LTNM	LICA	EMF&W	A&DC	<b>L U N C H</b>	ECA	EMF&W	A&DC(T)/LTNM(T)
TUE	A&DC	LICA	COUN	ECA		LTNM	CO-CU/DAA	
WED	LICA	A&DC	EMF&W	LTNM		ICA LAB / A&DC LAB		
THU	ECA	EMF&W	A&DC	LICA		A&DC LAB / ICA LAB		
FRI	LTNM	ECA	ECA LAB / GS LAB			LTNM(T)/A&DC(T)	LICA	SPORTS
SAT	EMF&W	ECA	LIB	A&DC		LTNM	GS LAB / ECA LAB	

\*(T) – Tutorial Concern Faculty

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the Faculty
MA401BS	LTNM-Laplace Transforms, Numerical Methods & Complex Variables	T.Thirupathi Reddy	EC406PC	A&DC LAB-Analog and Digital Communications Lab	B.Jyothirmai/K.Rajender/T.Ehavani
			EC407PC	ICA LAB-IC Applications Lab	A.M.../S.../T.../V...
EC402PC	EMF&W-Electromagnetic Fields and Waves	K.Rajender	EC408PC	ECA LAB-Electronic Circuit Analysis Lab	G.Nirmala/G.Anusha/Y.Rajani
EC403PC	A&DC-Analog and Digital Communications	B.Jyothirmai	*MC409	GS LAB-Gender Sensitization Lab	G.Ananda Rao
EC404PC	LICA-Linear IC Applications	G.Anitha	COUN	Counseling	I.Venu/G.Nirmala/A.Swetha
EC405PC	ECA-Electronic Circuit Analysis	G.Nirmala	SPORTS	Sports	Dr.S.Suresh/I.Venu
			CO-CU/DAA	Co-Curricular/Dept. Assoc.Activities	G.Nirmala/D.Aruna Kumari/K.Bhaskar Reddy
			LIB	Library	S.Alekhyia/M.Srilatha

*K.P.*  
Class in charge

**Head of the Department**  
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 Ibrahimpatnam, R.R.Dist-501 510

**Principal**  
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## **Lab External Question Paper**

**Subject Name : Electronic Circuit Analysis Lab**

**Year & Semester : II-II**

**A.Y:2022-2023**

1. Find out the bandwidth of Common Emitter Amplifier.
2. Find out the bandwidth of Two Stage RC Coupled Amplifier.
3. Find out the bandwidth of Cascode amplifier Circuit.
4. Find out the bandwidth of Darlington Pair Circuit.
5. Find out the bandwidth of Current Shunt Feedback amplifier Circuit.
6. Find out the bandwidth of Voltage Series Feedback amplifier Circuit.
7. Calculate the frequency of RC Phase shift Oscillator Circuit.
8. Calculate the frequency of Hartley Oscillators Circuit.
9. Calculate the frequency of Colpitt's Oscillators Circuit.
10. Calculate the efficiency of Class A power amplifier.
11. Calculate the efficiency of Class B Complementary symmetry amplifier.
12. Design a Monostable Multivibrator.
13. The output voltage waveform of Miller Sweep Circuit.



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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### II ECE REGULAR LAB EXTERNAL EXAMS TIMETABLE

A.Y: 2022-23

SEM: II

S.No.	Name of the Lab	Year/ Section	Name of the Lab Internal Examiner	Date & Time
1	Analog and Digital Communications Lab	II ECE-A	Mrs.B.Jyothirmai	21.09.2023(FN)
		II ECE-B	Mr.M.Ganesh	20.09.2023(AN)
2	Electronic Circuit Analysis Lab	II ECE-A	Mrs.G.Nirmala	19.09.2023(FN)
		II ECE-B	Mrs.G.Nirmala	19.09.2023(AN)
3	IC Applications Lab	II ECE-A	Mrs.D.Aruna Kumari	20.09.2023(FN)
		II ECE-B	Mrs.P.Kavitha	21.09.2023(AN)

Timings:- FN: 09:40 AM - 12:40 PM

AN: 01:00 PM - 04:00 PM

  
HOD/ECE

Head of the Department

Electronics and Communication Engg. Dept  
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PRINCIPAL

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**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**II ECE REGULAR LAB EXTERNAL EXAMINERS FROM TKRCET**

**A.Y: 2022-23**

**SEM: II**

S.No.	Name of the Lab	Year/ Section	Name of the Lab Internal Examiner	Date & Time	Name of the Lab External Examiner & Designation	Lab External Examiner Contact No.
1	Analog and Digital Communications Lab	II ECE-A	Mrs.B.Jyothirmal	21.09.2023(FN)	Dr. K. Sukanya Assoc. Prof	9951018558
		II ECE-B	Mr.M.Ganesh	20.09.2023(AN)	Mrs. M. Jagruthi Asst. Prof	9703263741
2	Electronic Circuit Analysis Lab	II ECE-A	Mrs.G.Nirmala	19.09.2023(FN)	Dr. J.Sunitha Kumari Assoc. Prof	9849727103
		II ECE-B	Mrs.G.Nirmala	19.09.2023(AN)	Dr. P. Gayathri Assoc. Prof	9440337355
3	IC Applications Lab	II ECE-A	Mrs.D.Aruna Kumari	20.09.2023(FN)	Dr. Mahesh Assoc. Prof	9491457702
		II ECE-B	Mrs.P.Kavitha	21.09.2023(AN)	Dr. B. Swapna Rani Assoc. Prof	9866104554

  
**HOD/ECE**  
Head of the Department  
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 Website: <https://siiet.ac.in/>

## LAB OCCUPANCY CHART

### ELECTRONIC CIRCUIT ANALYSIS LAB

	I 9:40-10:30	II 10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00-1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON					L U N C H		ECA Lab II ECE-B	
TUE	MAINTENANCE							
WED								
THU			ECA Lab II ECE-B					
FRI			ECA Lab II ECE-A					
SAT							ECA Lab II ECE-A	

  
 LAB INCHARGE

  
 HOD  
**Head of the Department**  
 Electronics and Communication Engg. Dept.  
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## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

### Do's and Don'ts

- All students must observe the **Dress code** while in the laboratory
- Foods, drinks and smoking are **NOT** allowed
- All bags must be left at the indicated place
- The lab time table must be strictly followed
- Be **PUNCTUAL** for your laboratory session
- Experiment must be completed within the given time
- Noise must be kept to a minimum
- Workspace must be kept clean and tidy at all time
- Handle all apparatus with care
- All students are liable for any damage to equipment due to their own negligence
- All equipment, apparatus, tools and components must be **RETURNED** to their original place after use
- Students are strictly **PROHIBITED** from taking out any items from the laboratory
- Students are **NOT** allowed to work alone in the laboratory without the lab supervisor
- Report immediately to the lab supervisor if any damages to equipment.

### BEFORE LEAVING LAB

- Place the stools under the lab bench
- Turn off the power to all instruments
- Please check the laboratory notice board regularly for updates.





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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### PHYSICAL LAB FLOOR PLAN

Lab Name: Electronic circuit Analysis Lab

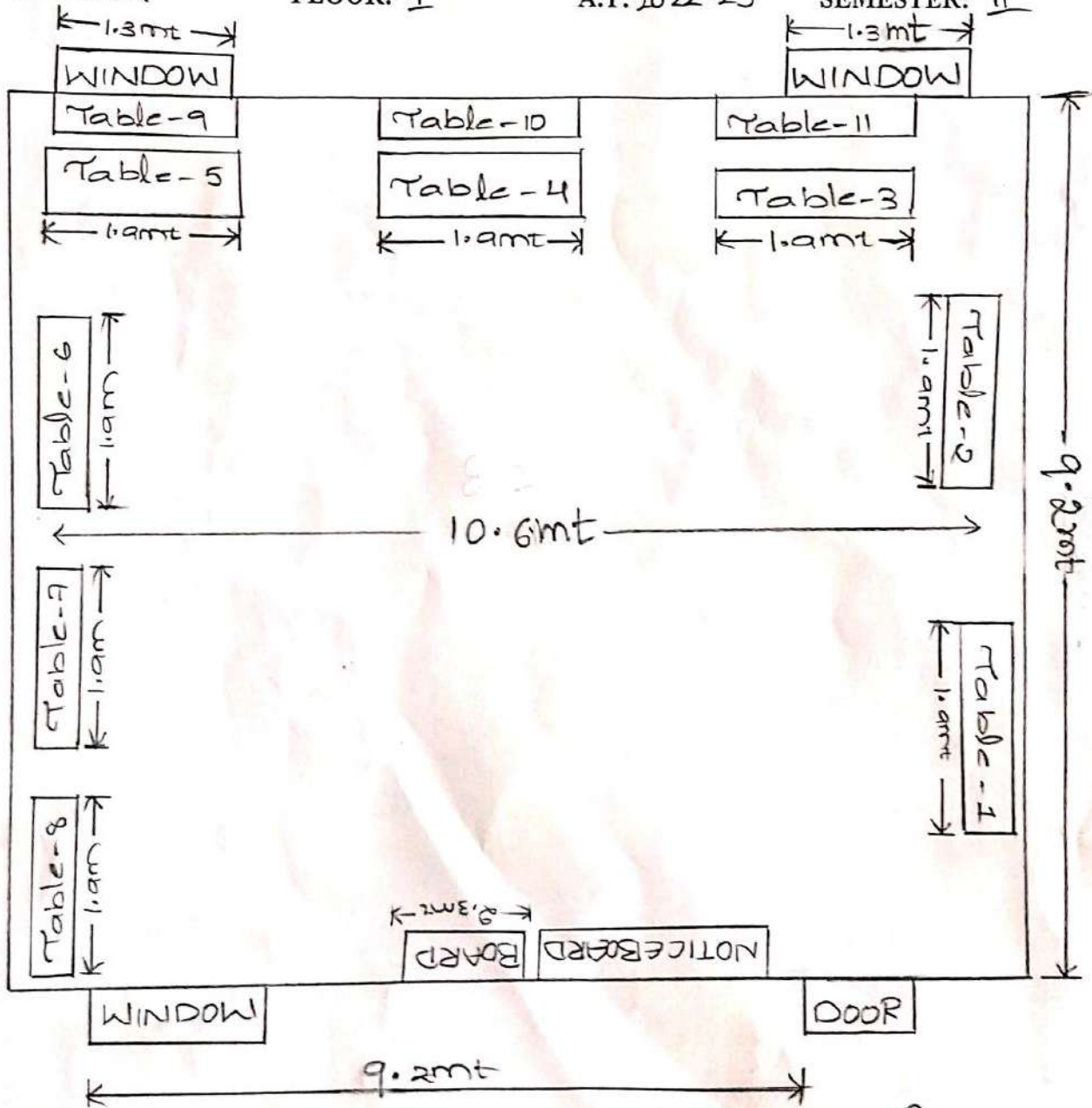
ROOM NO: A-114

BLOCK: A

FLOOR: I

A.Y: 2022-23

SEMESTER: II



Lab Area (In sqm) = 97.5259m

*K.P.*  
LAB IN CHARGE

*[Signature]*  
Head of the Department  
Electronics and Communication Engg. Dept  
SRI INDU INSTITUTE OF ENGG & TECH  
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

*[Signature]*  
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## **Lab manual link:**

<https://drive.google.com/file/d/1FRTdhj9ke7S2jUQu9HA-R0TUoY432OwA/view?usp=sharing>

# SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY



Department of Electronics and Communication Engineering

## Course Outcome Attainment (Internal Examination-1)

Name of the faculty :	G.Nirmala	A.Y:	2022-23
Branch & Section:	ECE - A	Examination	I Internal
Course Name:	ECA LAB	Year/Semester:	II/II

S.No Max. Marks ==>	HT No.	A+A+CD+MG	T+P+C+R	DDE
		5	5	15
1	21X31A0401	4	5	14
2	21X31A0402	4	3	10
3	21X31A0403	4	4	10
4	21X31A0404	4	5	11
5	21X31A0405	4	5	10
6	21X31A0406	5	5	14
7	21X31A0407	5	4	10
8	21X31A0408	5	4	11
9	21X31A0409	3	4	10
10	21X31A0410	4	5	13
12	21X31A0412	3	3	10
13	21X31A0413	4	5	14
14	21X31A0414	4	5	10
15	21X31A0415	5	5	10
16	21X31A0416	4	4	10
17	21X31A0417	4	3	11
19	21X31A0418	5	5	11
21	21X31A0420	5	5	15
22	21X31A0421	4	5	12
23	21X31A0422	4	5	10
24	21X31A0423	5	4	15
25	21X31A0424	4	4	10
26	21X31A0425	5	5	14
27	21X31A0426	5	5	10
28	21X31A0427	5	5	14
29	21X31A0428	5	4	10
30	21X31A0429	5	4	14
32	21X31A0431	5	5	12
33	21X31A0432	5	4	12
34	21X31A0433	5	5	14
35	21X31A0434	5	5	11
36	21X31A0435	4	4	10
37	21X31A0436	4	3	11
38	21X31A0437	4	4	10
39	22X35A0401	5	5	14
40	22X35A0402	5	5	13

41	22X35A0403	5	4	13
42	22X35A0404	4	5	10
43	22X35A0405	5	5	10
44	22X35A0406	5	5	13
45	22X35A0407	5	5	14
46	22X35A0408	4	5	15
47	22X35A0409	5	5	11
48	22X35A0410	5	5	13
49	22X35A0411	5	5	12
50	22X35A0412	5	4	13
51	22X35A0413	5	5	13
52	22X35A0414	5	5	11
53	22X35A0415	5	5	10
54	22X35A0416	4	5	11
55	22X35A0417	5	4	11
56	22X35A0418	5	5	13
57	22X35A0419	4	5	13
58	22X35A0420	5	5	10
Target set by the faculty / HoD		3.00	3.00	9.00
Number of students performed above the target		54	54	54
Number of students attempted		54	54	54
Percentage of students scored more than target		100%	100%	100%

**CO Mapping with Exam Questions:**

CO - 1	Y	Y	Y
CO - 2	Y	Y	Y
CO - 3	Y	Y	Y
CO - 4	Y	Y	Y
CO - 5	Y	Y	Y
CO - 6	Y	Y	Y

% Students Scored >Target %	100%	100%	100%
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**CO Attainment based on Exam Questions:**

CO - 1	100%	100%	100%
CO - 2	100%	100%	100%
CO - 3	100%	100%	100%
CO - 4	100%	100%	100%
CO - 5	100%	100%	100%
CO - 6	100%	100%	100%

CO	Intrnal practical	DDE	OverallI	Level
CO-1	100%	100%	100%	3.00
CO-2	100%	100%	100%	3.00
CO-3	100%	100%	100%	3.00
CO-4	100%	100%	100%	3.00
CO-5	100%	100%	100%	3.00
CO-6	100%	100%	100%	3.00

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal 1 Examination) =

**3.00**

**NOTE:**

**A+A+CD+MG : AIM+APPARATUS+CIRCUIT DIAGRAM+MODEL GRAPH**

**T+P+C+R : THEORY+PROCEDURE+CALCULATION+RESULT**

**DDE : Day to Day Evaluation**

# SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY



Department of Electronics and Communication Engineering

## Course Outcome Attainment (Internal Examination-2)

Name of the faculty :	G.Nirmala	A.Y:	2022-23
Branch & Section:	ECE - A	Examination	II Internal
Course Name:	ECA LAB	Year/Semester:	II/II

S.No Max. Marks ==>	HT No.	A+A+CD+MG	T+P+C+R	DDE
		5	5	15
1	21X31A0401	4	3	10
2	21X31A0402	3	4	10
3	21X31A0403	4	3	10
4	21X31A0404	4	5	10
5	21X31A0405	4	3	10
6	21X31A0406	5	5	14
7	21X31A0407	4	5	10
8	21X31A0408	5	5	11
9	21X31A0409	4	3	10
10	21X31A0410	5	5	12
12	21X31A0412	3	3	10
13	21X31A0413	5	5	11
14	21X31A0414	5	5	10
15	21X31A0415	3	4	10
16	21X31A0416	4	3	10
17	21X31A0417	5	5	13
19	21X31A0418	4	3	10
21	21X31A0420	5	5	14
22	21X31A0421	5	5	10
23	21X31A0422	5	5	11
24	21X31A0423	4	4	10
25	21X31A0424	3	4	10
26	21X31A0425	5	5	13
27	21X31A0426	4	5	10
28	21X31A0427	5	5	15
29	21X31A0428	5	5	10
30	21X31A0429	5	5	10
32	21X31A0431	4	5	11
33	21X31A0432	5	5	13
34	21X31A0433	4	5	10
35	21X31A0434	5	5	14
36	21X31A0435	4	4	10
37	21X31A0436	4	3	10
38	21X31A0437	3	4	10
39	22X35A0401	5	5	13
40	22X35A0402	5	5	11
41	22X35A0403	4	4	10

42	22X35A0404	3	4	10
43	22X35A0405	4	3	10
44	22X35A0406	3	4	10
45	22X35A0407	4	3	10
46	22X35A0408	4	4	10
47	22X35A0409	3	3	10
48	22X35A0410	4	5	10
49	22X35A0411	4	4	11
50	22X35A0412	4	4	10
51	22X35A0413	5	5	13
52	22X35A0414	4	3	10
53	22X35A0415	3	4	10
54	22X35A0416	5	5	11
55	22X35A0417	4	5	12
56	22X35A0418	5	5	14
57	22X35A0419	5	5	13
58	22X35A0420	4	4	10
Target set by the faculty / HOD		3.00	3.00	9.00
Number of students performed above the target		36	36	36
Number of students attempted		36	36	36
Percentage of students scored more than target		100%	100%	100%

**CO Mapping with Exam Questions:**

CO - 1	Y	Y	Y
CO - 2	Y	Y	Y
CO - 3	Y	Y	Y
CO - 4	Y	Y	Y
CO - 5	Y	Y	Y
CO - 6	Y	Y	Y

% Students Scored >Target %	100%	100%	100%
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**CO Attainment based on Exam Questions:**

CO - 1	100%	100%	100%
CO - 2	100%	100%	100%
CO - 3	100%	100%	100%
CO - 4	100%	100%	100%
CO - 5	100%	100%	100%
CO - 6	100%	100%	100%

CO	Intrnal practical	DDE	Overall	Level
CO-1	100%	100%	100%	3.00
CO-2	100%	100%	100%	3.00
CO-3	100%	100%	100%	3.00
CO-4	100%	100%	100%	3.00
CO-5	100%	100%	100%	3.00
CO-6	100%	100%	100%	3.00

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal 2 Examination) =

**3.00**

**NOTE:**

**A+A+CD+MG : AIM+APPARATUS+CIRCUIT DIAGRAM+MODEL GRAPH**

**T+P+C+R : THEORY+PROCEDURE+CALCULATION+RESULT**

**DDE : Day to Day Evaluation**



# SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY



Department of Electronics and Communication Engineering

## Course Outcome Attainment (University Examinations)

Name of the faculty: G.Nirmala

Branch & Section: ECE - A

Course Name: ECA LAB

Academic Year: 2022-23

Year / Semester: II/II

S.No	Roll Number	Marks Secured
1	21X31A0401	63
2	21X31A0402	55
3	21X31A0403	57
4	21X31A0404	71
5	21X31A0405	69
6	21X31A0406	72
7	21X31A0407	59
8	21X31A0408	69
9	21X31A0409	55
10	21X31A0410	68
12	21X31A0412	56
13	21X31A0413	70
14	21X31A0414	68
15	21X31A0415	60
16	21X31A0416	55
17	21X31A0417	69
19	21X31A0418	71
21	21X31A0420	72
22	21X31A0421	69
23	21X31A0422	70
24	21X31A0423	70
25	21X31A0424	55
26	21X31A0425	71
27	21X31A0426	68
28	21X31A0427	72
29	21X31A0428	65
30	21X31A0429	69
32	21X31A0431	55
33	21X31A0432	66
34	21X31A0433	72
35	21X31A0434	72
Max Marks		75

S.No	Roll Number	Marks Secured
36	21X31A0435	58
37	21X31A0436	60
38	21X31A0437	56
39	22X35A0401	70
40	22X35A0402	71
41	22X35A0403	65
42	22X35A0404	56
43	22X35A0405	60
44	22X35A0406	64
45	22X35A0407	72
47	22X35A0409	62
48	22X35A0410	69
49	22X35A0411	69
50	22X35A0412	57
51	22X35A0413	71
52	22X35A0414	68
53	22X35A0415	66
55	22X35A0417	71
56	22X35A0418	65
57	22X35A0419	66
58	22X35A0420	72

Attainment Level	% students
1	40%
2	50%
3	60%

Class Average mark	64
Number of students performed above the target	28
Number of successful students	44
Percentage of students scored more than target	64%
<b>Attainment level</b>	<b>3</b>

# SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY



Department of Electronics and Communication Engineering

## Course Outcome Attainment

Name of the faculty: G.Nirmala  
Branch & Section: ECE - A  
Course Name: ECA LAB

Academic Year: 2022-23  
Examination: I Internal  
Year: II  
Semester: II

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00	3.00	3.00	3.00	3.00
CO2	3.00	3.00	3.00	3.00	3.00
CO3	3.00	3.00	3.00	3.00	3.00
CO4	3.00	3.00	3.00	3.00	3.00
CO5	3.00	3.00	3.00	3.00	3.00
CO6	3.00	3.00	3.00	3.00	3.00
<b>Internal &amp; University Attainment:</b>			3.00	3.00	
<b>Weightage</b>			25%	75%	
<b>CO Attainment for the course (Internal, University)</b>			0.75	2.25	
<b>CO Attainment for the course (Direct Method)</b>			3.00		

Overall course attainment level

**3.00**



# SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering  
Program Outcome Attainment (from Course)

Name of	G.Nirmal		
Faculty:	a	Academic Year:	2022-23
Branch &		Year:	II
Section:	ECE - A		
	ECA		
Course Name:	LAB	Semester:	II

### CO-PO mapping

Course	PO 1	PO2	PO 3	PO 4	PO 5	PO6	PO7	PO 8	PO9	PO 10	PO 11	PO 12	PS O1	PS O2
<b>C228.1</b>	3	3	2	2	-	-	-	-	-	-	-	-	3	3
<b>C228.2</b>	2	3	2	2	-	-	-	-	-	-	2	-	2	2
<b>C228.3</b>	2	3	2	2	-	-	-	-	-	-	-	3	3	3
<b>C228.4</b>	1	3	2	2	-	-	-	-	-	-	2	-	3	3
<b>C228.5</b>	3	2	1	2	-	-	-	-	-	-	-	3	2	2
<b>C228.6</b>	2	3	2	-	-	-	-	-	-	-	-	-	1	1
<b>AVG</b>	<b>2.17</b>	<b>2.83</b>	<b>1.83</b>	<b>2.00</b>	-	-	-	-	-	-	<b>2</b>	<b>3</b>	<b>2.33</b>	<b>2.33</b>

CO	Course Outcome Attainment
	3.00
<b>CO1</b>	
	3.00
<b>CO2</b>	
	3.00
<b>CO3</b>	
	3.00
<b>CO4</b>	
	3.00
<b>CO5</b>	
	3.00
<b>CO6</b>	
	3.00
<b>Overall course attainment level</b>	<b>3.00</b>

**PO-  
ATTAIN  
MENT**

	PO 1	P O 2	PO 3	P O 4	PO 5	PO6	PO7	PO 8	PO9	PO10	PO 11	PO 12	PS O1	PS O2
<b>CO Attainme nt</b>	<b>2.1 7</b>	<b>2. 83</b>	<b>1.8 3</b>	<b>2. 00</b>	-	-	-	-	-	-	<b>2</b>	<b>3</b>	<b>2.3 3</b>	<b>2.3 3</b>

**CO contribution to PO - 33%, 67%, 100% (Level  
1/2/3)**