

Recognized Under 2(f) of UGC Act 1956 Approved by AICTE, New Delhi Affiliated to JNTUH, Hyderabad.

COURSE FILE

ON

LINEAR IC APPLICATIONS

CourseCode-EC404PC

II-B.Tech II-SEMESTER A.Y.:2022-2023

Prepared by

Mrs. P.KAVITHA Assistant Professor

Head of the Department Electronics and Communication Engg. Dept SRI INDU INSTITUTE OF ENGG & TECH Sherguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL Sri Indu Institute of Engineering & Tect. Sheriguda(Vill), Ibrahimpatnam

R.R. Dist. Telangana-501 510.

Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510. Campus Ph:9640590999, 9347187999, 8096951507.



Recognized Under 2(f) of UGC Act 1956 Approved by AICTE, New Delhi Affiliated to JNTUH, Hyderabad.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year	2022-2023
Course Title	LINEAR IC APPLICATIONS
Course Code	EC404PC
Programme	B. Tech
Year & Semester	II year II-semester
Branch & Section	ECE- B
Regulation	R18
Course Faculty	Mrs. P. KAVITHA, Assistant Professor

Index of Course File

S. No.	Name of the content
1	Institute vision and mission
2	Department vision and mission
3	Program Educational Objectives /Program Specific Outcomes
4	Program Outcomes
5	Course Syllabus with Structure
6	Course Outcomes(CO)
7	Mapping CO with PO/PSO and Justification
8	Academic Calendar
9	Timetable-highlighting your course periods including tutorial
10	Lesson plan with number of hours/periods, TA/TM, Text/ Reference book
11	Web references
12	Lecture notes
13	List of Power point presentations
14	University Question papers
15	Internal Question papers, Key with CO and BT
16	Assignment Question papers mapped with CO and BT
17	Tutorial topics
18	Result Analysistoidentifyweakandadvancedlearners-3timesinasemester
19	Result Analysis at the end of the course
20	Remedial class for weak students -schedule and evidences
21	CO,PO/PSO attainment sheets
22	Attendance register
23	Course file (Digital form)

Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510. Campus Ph:9640590999, 9347187999, 8096951507.



Recognized Under 2(f) of UGC Act 1956 Approved by AICTE, New Delhi Affiliated to JNTUH, Hyderabad.

INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

- **IM1:** To offer outcome-basededucationandenhancementoftechnicalandpracticalskills.
- **IM2:** To Continuous assess of teaching-learning process through institute-industry collaboration.
- **IM3:** To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.
- **IM4:** To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

Head of the Department Electronics and Communication Engg. Dept SRI INDV INSTITUTE OF ENGG & TECH Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL

Sri Indu Institute of Engineering & Tech Sheriguda(Vill), Ibrahimpatnam R.R. Dist. Telangana-501 510.

Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510. Campus Ph:9640590999, 9347187999, 8096951507.



Recognized Under 2(f) of UGC Act 1956 Approved by AICTE, New Delhi Affiliated to JNTUH, Hyderabad.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

- **DM1:** To facilitate an academic environment that enables student's centric learning.
- **DM2:** To providestate-of-the-arthardwareandsoftwaretechnologiestomeetindustry requirements.
- DM3: To continuously update the Academic and Research infrastructure.
- **DM4:** To ConductTechnicalDevelopmentProgramsforoverallprofessionalcaliberofStake Holders.

Head of the Department Electronics and Communication Engg. Dept SRI INDU INSTITUTE OF ENGG & TECH Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL

Sri Indu Institute of Engineering & Tech Sheriguda(Vill), Ibrahimpatnam R.R. Dist. Telangana-501 510.

Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510. Campus Ph:9640590999, 9347187999, 8096951507.



Recognized Under 2(f) of UGC Act 1956 Approved by AICTE, New Delhi Affiliated to JNTUH, Hyderabad.

PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

- **PEO1:** Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.
- **PEO2:** Graduates with ability to execute innovative ideas for Research and Development with continuous learning.
- PEO3: Graduates inculcated with industry based soft-skills to enable employability.
- **PEO4:** Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

Head of the Department Electronics and Communication Engg. Dept SRI INDU INSTITUTE OF ENGG & TECH Sherguda(V), Ibrahimpatham(M), R.R.Dist-501 510

PRINCIPAL Sri Indu Institute of Engineering & Tech Sheriguda(Vill), Ibrahimpatnam

R.R. Dist. Telangana-501 510.

Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510. Campus Ph:9640590999, 9347187999, 8096951507.



Recognized Under 2(f) of UGC Act 1956 Approved by AICTE, New Delhi Affiliated to JNTUH, Hyderabad.

PROGRAM OUTCOMES

1.**ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2.**PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problemsreachingsubstantiatedconclusionsusingfirstprinciplesofmathematics, natural sciences, and engineering sciences.

3.**DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4.**CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5.**MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6.**THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7.**ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8.**ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9.**INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **LIFE-LONGLEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510. Campus Ph: 9640590999, 9347187999, 8096951507.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING II YEAR COURSE STRUCTURE AND SYLLABUS (R18)

IIYEAR I SEMESTER

S. No.	Course Code	Course Title	L	Т	Р	Credits
1	EC301PC	Electronic Devices and Circuits	3	1	0	4
2	EC302PC	Network Analysis and Transmission Lines	3	0	0	3
3	EC303PC	Digital System Design	3	1	0	4
4	EC304PC	Signals and Systems	3	1	0	4
5	EC305ES	Probability Theory and Stochastic Processes	3	0	0	3
6	EC306PC	Electronic Devices and Circuits Lab	0	0	2	1
7	EC307PC	Digital System Design Lab	0	0	2	1
8	EC308ES	Basic Simulation Lab	0	0	2	1
9	*MC309	Constitution of India	3	0	0	0
		Total Credits	18	3	6	21

II YEAR II SEMESTER

S. No.	Course Code	Course Title	L	Т	Р	Credits
1	MA401BS	Laplace Transforms, Numerical Methods& Complex Variables	3	1	0	4
2	EC402PC	Electromagnetic Fields and Waves	3	0	0	3
3	EC403PC	Analog and Digital Communications	3	1	0	4
<mark>4</mark>	EC404PC	Linear IC Applications	<mark>3</mark>	<mark>0</mark>	<mark>0</mark>	<mark>3</mark>
5	EC405PC	Electronic Circuit Analysis	3	0	0	3
6	EC406PC	Analog and Digital Communications Lab	0	0	3	1.5
7	EC407PC	IC Applications Lab	0	0	3	1.5
8	EC408PC	Electronic Circuit Analysis Lab	0	0	2	1
9	*MC409	Gender Sensitization Lab	0	0	2	0
		Total Credits	15	2	10	21

EC404PC: LINEAR IC APPLICATIONS

B. Tech. II Year II Sem.

Pre-requisite: Electronic Devices & Circuits

Course Objectives: The main objectives of the course are:

- To introduce the basic building blocks of linear integrated circuits.
- To introduce the theory and applications of analog multipliers and PLL.
- To introduce the concepts of wave form generation and introduce some special function ICs.

Course Outcomes: Upon completing this course, the student will be able to

- Thorough understanding operational amplifiers with linear integrated circuits.
- Attain the knowledge of functional diagrams and applications of IC555 and IC 565
- Acquire the knowledge about the Data converters.

UNIT-I

Integrated Circuits: Classification, chip size and circuit complexity, basic information of Op-amp, ideal and practical Op-amp, internal circuits, Op-amp characteristics, DC and AC Characteristics, 741 op- amp and its features, modes of operation-inverting, non-inverting, differential.

UNIT-II

Op-amp and Applications: Basic information of Op-amp, instrumentation amplifier, ac amplifier, V to I and I to V converters, Sample & hold circuits, multipliers and dividers, differentiators and integrators, comparators, Schmitt trigger, Multivibrators, introduction to voltage regulators, features of 723

UNIT-III

Active Filters &Oscillators: Introduction, 1st order LPF, HPF filters, Band pass, Band reject and all pass filters. Oscillator types and principle of operation - RC, Wien and quadrature type, waveform generators - triangular, saw tooth, square wave and VCO.

UNIT-IV

Timers & Phase Locked Loops: Introduction to 555 timer, functional diagram, monostable and astable operations and applications, Schmitt Trigger. PLL - introduction, block schematic, principles and description of individual blocks of 565.

UNIT-V

D-A and A-D Converters: Introduction, basic DAC techniques, weighted resistor DAC, R-2R ladder DAC, inverted R-2R DAC, slope integration type ADC, DAC and ADC specifications.

TEXT BOOKS:

- 1. Linear Integrated Circuits, D. Roy Chowdhury, New Age International (p) Ltd.
- 2. Op-Amps & Linear ICs, Ramakanth A. Gayakwad, PHI

REFERENCESBOOKS:

- 1. Operational Amplifiers & Linear Integrated Circuits, R.F. Coughlin & Fredrick F. Driscoll, PHI.
- 2. Operational Amplifiers & Linear Integrated Circuits: Theory & Applications, Denton J. Daibey, TMH.
- 3. Design with Operational Amplifiers & Analog Integrated Circuits, Sergio Franco, Mc Graw Hill.
- 4. Digital Fundamentals-Floydan dJain, Pearson Education.

L T P C 3 0 0 3



Accredited by NAAC with A+ Grade, Recognized under2 (f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), RangaReddy Dist.,Telangana–501510 Website: https://siiet.ac.in/

COs and Mapping with PO/PSO

Course: LINEAR IC APPLICATIONS (C224)

Course Outcomes

After completing this course, the student will be able to:

C224.1: Understand the internal operation of Op-Amp and its specifications.

[Knowledge, Understand]

Class: II ECE- B

C224.2: Analyze and design linear applications like adder, subs tractor, instrumentation amplifier and etc. using Op-Amp. [Application, Analysis]

C224.3: Analyze and design non linear applications like multiplier, comparator and etc, using Op-Amp. [Analysis, Evaluation]

C224.4: Classify various active filter configurations based on frequency response and construct using 741 Op Amp. [Analysis]

C224.5: Operate 555 timers in different modes like bistable, monostable and astable operations and study their applications. [Application, Analysis]

C224.6: Determine the lock range and capture range of PLL and use in various applications of communications. [Knowledge, Understand]

Mapping of course outcomes with program outcomes:

High-3 Medium-2 Low-1

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO	PSO
													1	2
C224.1	3	2	-	3	-	-	-	-	-	-	-	3	1	2
C224.2	3	3	2	-	-	-	-	-	-	-	-	2	1	2
C224.3	3	3	2	-	-	-	-	-	-	-	2	2	1	1
C224.4	3	2	1	-	-	-	-	-	-	-	-	-	1	2
C224.5	3	3	3	-	2	-	2	-	-	-	2	2	2	2
C224.6	3	2	2	-	-	-	-	-	-	2	-	-	2	2
Averag	3	2.5	2	3	2	-	2	-	-	2	2	2.3	1.33	1.83
e														



Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956 (Approved by AICTE ,New Delhi and Affiliated to J NTUH, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), RangaReddy Dist., Telangana –501510 Website: https://siiet.ac.in/

CO-PO/PSO Mapping-Justification

Course: LINEAR IC APPLICATIONS (C224)

Class: II ECE- B

PO1: ENGINEERING KNOWLEDGE: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: PROBLEM ANALYSIS: Identify, formulate, research literature, and analyze complex engineering problemsreachingsubstantiatedconclusionsusingfirstprinciplesofmathematics, natural sciences, and engineering sciences.

PO3: DESIGN/DEVELOPMENT OF SOLUTIONS: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: MODERN TOOL USAGE: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO7: ENVIRONMENT AND SUSTAINABILITY: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO10: COMMUNICATION: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

PO11: PROJECT MANAGEMENT AND FINANCE: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: LIFE-LONGLEARNING: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

<u>CO-PO mapping Justification</u>

C224.1: Understand the internal operation of Op-Amp and its specifications. [Knowledge, Understand]

	Justification
PO1	Students get the knowledge of characteristics of the operational amplifier
PO2	Students able to understand the modes of operation.
PO4	Students can analyse the applications of op-amp
PO12	Students can use this application in the future
PSO1	Students will be able to understand about ICS
PSO2	Students will be able to understand about op-amps

C224.2: Analyze and design linear applications like adder, subs tractor, instrumentation amplifier and etc. using Op-Amp. [Application, Analysis]

	Justification
PO1	Students get the knowledge of non linear applications
PO2	This approach fosters a deep understanding of circuits, facilitating the creation of reliable and efficient designs.
PO3	Students can understand the knowledge of adder and Subtractor circuit.
PO12	This concept can use in the future
PSO1	Students will be able to understand about adder circuit
PSO2	Students will be able to understand about instrumentation amplifier

C224.3: Analyze and design non linear applications like multiplier, comparator and etc, using Op-Amp. [Analysis, Evaluation]

	Justification
PO1	Students get the knowledge on Filters and Oscillators.
PO2	Students can solve problems on Filters and Oscillators.
PO3	Students able to design the different types of filters.
PO11	This concepts can use in the their projects

PO12	This concept can use in the projects
PSO1	Students will be able to understand about comparator
PSO2	Students will be able to understand about multiplier

C224.4: Classify various active filter configurations based on frequency response and construct using 741 Op Amp. [Analysis]

	Justification
PO1	Students can acquire the knowledge on timers and voltage controlled oscillator.
PO2	Students can solve problems on timers.
PO3	Students able to design the applications of IC 555 & IC 565.
PSO1	Students will be able to understand about the filters
PSO2	Students will be able to understand about timing applications

C224.5: Operate 555 timers in different modes like bistable, monostable and astable operations and study their applications. [Application, Analysis]

	Justification
PO1	Students get the knowledge on A/D and D/A Converters.
PO2	Students can solve problems on Specifications of A/D and D/A Converters.
PO3	Students able to design the different types of converters.
PO5	Students can use applications of timers
PO7	Students will be able to use in future applications
PO11	Students can get the knowledge about conversion
PO12	Students can use in project applications
PSO1	Students will be able to understand about the converters
PSO2	Students will be able to understand about timing applications

C224.6: Determine the lock range and capture range of PLL and use in various applications of communications.

[Knowledge, Understand]

	Justification
PO1	Students get the knowledge on PLL.
PO2	Students can solve problems on applications of PLL.
PO3	Students able to get knowledge of lock range.
PO10	Students can get knowledge of capture range.
PSO1	Students will be able to understand about the converters
PSO2	Students will be able to understand about applications of communications.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

ACADEMIC CALENDAR 2022-23

B. Tech./B.Pharm. II YEAR I & II SEMESTERS

I SEM

S. No	Description	Duration		
		From	То	
1	Commencement of I Semester classwork		28.11.2022	
2	1 st Spell of Instructions	28.11.2022	21.01.2023 (8 Weeks)	
3	First Mid Term Examinations	23.01.2023	30.01.2023 (1 Week)	
4	Submission of First Mid Term Exam Marks to the University on or before	04.02.2023		
5	2 nd Spell of Instructions	31.01.2023	29.03.2023 (8 Weeks)	
6	Second Mid Term Examinations	31.03.2023	08.04.2023 (1 Week)	
7	Preparation Holidays and Practical Examinations	10.04.2023	15.04.2023 (1 Week)	
8	Submission of Second Mid Term Exam Marks to the University on or before	15.04.2023		
9	End Semester Examinations	17.04.2023	29.04.2023 (2 Weeks)	

Note: No. of Working / Instructional Days: 93

II SEM

S. No	Description	Duration			
	Description	From	То		
1	Commencement of II Semester classwork	01.05.2023			
2	1 st Spell of Instructions (including Summer Vacation)	01.05.2023	08.07.2023 (10 Weeks)		
3	Summer Vacation	15.05.2023	27.05.2023 (2 Weeks)		
4	First Mid Term Examinations	10.07.2023	15.07.2023 (1 Week)		
5	Submission of First Mid Term Exam Marks to the University on or before		22.07.2023		
6	2 nd Spell of Instructions	18.07.2023	11.09.2023 (8 Weeks)		
7	Second Mid Term Examinations	12.09.2023	16.09.2023 (1 Week)		
8	Preparation Holidays and Practical Examinations	19.09.2023	23.09.2023 (1 Week)		
9	Submission of Second Mid Term Exam Marks to the University on or before		23.09.2023		
10	End Semester Examinations	25.09.2023	07.10.2023 (2 Weeks)		

Note: No. of Working / Instructional Days: 92

REGISTRAR



UGC Autonomous, Accredited by NAAC A+ Grade, Recognized under 2(f) of UGC Act 1956. (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana - 501 510 https://siiet.ac.in/

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING **Class Timetable**

TIME/	ISS: II-B. Tech EC	CE-B	A.Y:2022-	23	SI	EMESTE	ER: II		LH:	C-102
DAY	9:40-10:30	10:30 -11:2	III 0 11:20-12:10	0 12	IV :10-1:00	1:00-	1.20	2:20	VI	VII
MON	EMF&W	ECA	A&DC		LTNM	1.50	1:50-	2:20	2:20-3:10	3:10-4:0
TUE	LICA	A&DC	EMERW			-	LICA		ECA LAB/GS LA	
WED	LTNM	Et many	LIVIPOCW	_	ECA L A&DC LA		A&DC LA	AB / ICA LAB		
TED	LINM	EMF&W	LICA	1	ECA	U	A&DC(T)/	LTNM(T)/	0.0	
THU	A&DC	COUN	GS LA	B/ECALA	В	N	LTN	n/	0.0	UDAA
FRI	ECA	EMF&W	LTNM(T)/A&D	COT	LICA	H	LIN	IM	EMF&W	SPORTS
SAT	LICA	LTNM	ECI	(1)	LICA		A&I	DC	LTNM	LIB
*(T) - Tutorial Conc	ern Faculty	ECA	I	\&DC			ICA LAB/	A&DC LAB	
Course Code	Course	Name	Name of the Faculty	Course Code		Course	e		Name of th	e
AA401BS	LTNM-Laplace Numerical Meth Complex Variat	Transforms, ods & oles	Dr.B.Mahesh	EC406PC	A&DC LAB-Analog and Digital Communications Lab		A&DC LAB-Analog and Digital Communications Lab M.Ganesh/S.Nares		S.Naresh/K.R	ajender
C402PC	EMF&W-Electr Fields and Wave	romagnetic	Dr.S.Suresh	EC40/PC EC408PC	ICA LAB-IC Applications Lab ECA LAB-Electronic Circuit		ICA LAB-IC Applications Lab P.Kavitha/A.Vaani/T ECA LAB-Electronic Circuit Dr.D.Lakshmaiah/Dr		A.Vaani/T.Div hmaiah/Dr.S.S	vya Suresh/
C403PC	A&DC-Analog Communications	and Digital	S.Naresh	*MC409	GS LAB-Gender Sensitization		GS LAB-Gender Sensitization Lab G.Ananda Rap		Rao	19.5
C404PC	LICA-Linear IC	Applications	P.Kavitha	COUN	Counseling D.A.L.		DUN Counseling		T.D. 10 1	-
	POL PLAN	o:		SPORTS	Sports			G.Nirmala/	1.Divya/G.Ar	lusna
405PC	Analysis	Circuit	Dr.D.Lakshmaiah	CO- CU/DAA	DAA Dept. Assoc		es	S.Alekhya/	I.Venu/K.Bhas	skar Reddy
	SBB			LIB	Library			A.Sindhuja	0,Swathi /	

Head of The Department Electronics and Communication Engg. Dept

BAINCIPAL Rrincipal Sn Indu Institute of Engineering & Teci Sheriguda(Vill), Ibrahimpatnam p. Diet Telangana -501 510



Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam(M),RangaReddy Dist.,Telangana–501510 Website: https://siiet.ac.in/

LESSON PLAN

Programme: B. Tech	Academic Year: 2022-23
Year: II	Semester: II
Course Title: LINEAR IC APPLICATIONS	Course Code:EC404PC
Name of Faculty: P.KAVITHA	

UNIT - I

Integrated Circuits: Classification, chip size and circuit complexity, basic information of Op-amp, Ideal and practical Op-amp, internal circuits, Op-amp characteristics, DC and AC Characteristics, 741 op-amp and its features, modes of operation-inverting, non-inverting, differential

No. of	Topics	Reference	Teaching
Sessions			Method/
Planned			Aids
1	Introduction to Integrated Circuits	T1,R1	Black
			board
1	Classification of Integrated Circuits	T1,R1	Black
			board
1	Chip size and circuit complexity	T1,R1	Black
			board
1	Basic information of Op-amp	T1,R1,W1	Black
			board
1	Ideal and practical Op-amp	T1,R1	Black
			board
1	Internal circuit of Op-amp	T1,R1	Black
			board
1	AC Characteristics of Op-amp	T1,R1,R2	Black
			board
1	DC Characteristics of Op-amp	T1,R1,R2	Black
			board
1	IC 741 op-amp and its features	T1,R1	Black
			board
2	Inverting mode of operation	T2,R1,	Black
			board
1	Non-Inverting mode of operation	T2,R1,	Black
			board
1	Differential mode of operation	T2,R1,	Black
			board
Gap bey	ond syllabus(if any):		
Gap with	ı in the syllabus(if any)		
CourseO	utcome1: Understand the internal operation of Op-A	np and its specifications. [k	Knowledge,
Understan	d]		6.1
*Session	Duration: 50minutes		

Session Duration. Joininutes



Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), RangaReddy Dist., Telangana –501510 Website: https://siiet.ac.in/

Unit-II Syllabus

Op-amp and Applications: Basic information of Op-amp, instrumentation amplifier, ac amplifier, V to I and I to V converters, Sample & hold circuits, multipliers and dividers, differentiators and Integrators, comparators, Schmitt trigger, Multivibrators, introduction to voltage regulators, Features of 723

No. of	Topics	Reference	Teaching
Sessions			Method/
Planned			Aids
1	Basic information of Op-amp	R2	Black board
1	Instrumentation amplifier using Op-amp	R2	Black board
1	AC amplifier using Op-amp	R2	Black board
1	V to I and I to V converters using Op-amp	R2,W2	Black board
1	Sample & hold circuits using Op-amp	R2	Black board
1	Multipliers and Dividers using Op-amp	R2	Black board
1	Differentiators using Op-amp	R2	Black board
1	Integrators using Op-amp	R2	Black board
1	Comparator using Op-amp	R2	Black board
1	Schmitt trigger using Op-amp	R2	Black board
1	Multivibrators using Op-amp	R2	Black board
1	Introduction to voltage regulators	R2	Black board
2	Features of 723	R2	Black board
Gap beyo	ond syllabus(if any):		
Gap with	in the syllabus(if any)		

CourseOutcome1: Analyze and design linear applications like adder, substractor, instrumentation amplifier and etc. using Op-Amp. [Application, Analysis]

*Session Duration: 50 minutes

*Total Number of Hours/Unit: 14



Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda (V),Ibrahimpatnam(M),Ranga Reddy Dist., Telangana –501510 Website: https://siiet.ac.in/

Unit-III Syllabus

Active Filters & Oscillators: Introduction, 1st order LPF, HPF filters, Band pass, Band reject and All pass filters. Oscillator types and principle of operation - RC, Wien and quadrature type, waveform Generators - triangular, saw tooth, square wave and VCO.

No. of	Topics	Reference	Teaching
Sessions			Method/
Planned			Aids
1	Introduction to Filters & Oscillators	R1,R4	Black board
1	1st order LPF filter	R1,R4,W3	Black board
1	1st order HPF filter	R1,R4	Black board
1	Band pass, Band reject filters	R2,R4	Black board
1	All Pass filters	R2,R4	Black board
1	Introduction to Oscillators	T1,R2	Black board
1	Principle of operation on Oscillators	T1,R2	Black board
1	RC Phase Shift Oscillators	T1,R2	Black board
1	Wien Bridge Oscillators	T1,R2	Black board
1	Quadrature type Oscillators	T1,R2	Black board
1	Triangular waveform generators	R4	Black board
1	Saw tooth waveform generators	R4	Black board
1	Square waveform generators	R4	Black board
1	VCO	T1,R4	Black board
Gap beyo	ond syllabus(if any):		

Gap with in the syllabus(if any)

CourseOutcome1: Classify various active filter configurations based on frequency response and construct using 741 Op Amp.

*Session Duration: 50minutes

*Total Number of Hours/Unit:14



Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTU H, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), RangaReddy Dist., Telangana –501510 Website: https://siiet.ac.in/

Unit-IV Syllabus

Timers & Phase Locked Loops: Introduction to 555 timer, functional diagram, monostable and Astable operations and applications, Schmitt Trigger. PLL - introduction, block schematic, Principles and description of individual blocks of 565.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids	
1	Introduction to 555 timer	R3,R4,W4	Black board	
1	Functional diagram of 555 timer	R3,R4,W4	Black board	
1	Monostable multivibrator using 555 timer	R3,R4	Black board	
1	Astable multivibrator using 555 timer	R3,R4,W4	Black board	
1	Applications of Monostable multivibrator	R2,R4,W4	Black board	
1	Applications of Astable multivibrator	R2,R4	Black board	
1	Schmitt Trigger	R2,R4	Black board	
1	Introduction to PLL	R2,R4	Black board	
1	Block schematic operation of PLL	T2, R4	Black board	
1	Description of individual blocks of 565	T2, R4	Black board	
1	Applications of PLL	T2, R4	Black board	
Gap beyond syllabus(if any):				
Gap with in the syllabus(if any)				
CourseO astable op	utcome1: Operate 555 timers in different modes literations and study their applications	ke bistable, monost	able and	

*Session Duration: 50minutes

*Total Number of Hours/Unit: 11



Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956 (Approved by AICTE ,New Delhi and Affiliated to JNTUH, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam(M),RangaReddyDist., Telangana–501510 Website: https://siiet.ac.in/

Unit-V Syllabus

D-A and A-D Converters: Introduction, basic DAC techniques, weighted resistor DAC, R-2R ladder DAC, inverted R-2R DAC, and IC 1408 DAC, Different types of ADCs - parallel comparator type ADC, counter type ADC, successive approximation ADC dual slope integration type ADC, DAC and ADC specifications.

No. of	Topics	Reference	Teaching	
Sessions			Method/	
Planned			Aids	
1	Introduction to D-A and A-D Converters	T1	Black board	
2	Weighted resistor DAC	T1	Black board	
1	R-2R ladder DAC	T1	Black board	
2	Inverted R-2R DAC	T1	Black board	
1	IC 1408 DAC	T1	Black board	
2	Parallel Comparator type ADC	T1	Black board	
1	Counter type ADC	T1	Black board	
2	Successive Approximation ADC	T1	Black board	
2	Dual Slope Integration type ADC	T1	Black board	
1	DAC and ADC specifications.	T1	Black board	
Gap beyond syllabus (if any):				
Gap with in the syllabus(if any)				
CourseO	utcome1			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 15 **TEXT BOOKS:**

T1: Linear Integrated Circuits, D. Roy Chowdhury, New Age International (p) Ltd.

T2: Op-Amps & Linear ICs, Ramakanth A. Gayakwad, PHI

REFERENCES BOOKS:

R1: Operational Amplifiers & Linear Integrated Circuits, R.F. Coughlin & Fredrick F. Driscoll, PHI.

R2: Operational Amplifiers & Linear Integrated Circuits: Theory & Applications, Denton J. Daibey, And TMH.

R3: Design with Operational Amplifiers & Analog Integrated Circuits, Sergio Franco, McGraw Hill.

R4: Operational Amplifiers with Linear Integrated Circuits by K.Lal Kishore-Pearson, 2009.

WEBREFERENCES:

<u>+</u>	
S. No.	Web Link
1	https://www.electronics-tutorials.ws/opamp/opamp_1.html
2	https://www.youtube.com/watch?v=GugPxYOscg4
3	https://kobita1234.files.wordpress.com/2016/11/ch-68.pdf
4	https://www.electricaltechnology.org/2014/12/555-timer.html



Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), RangaReddy Dist.,Telangana–501510 Website: https://siiet.ac.in/

Lecture notes

Unit1link:

https://drive.google.com/file/d/1dA3H76w0uFN3uZkxWOrv_5Ffl7mHX_CU/view?usp=sharing

Unit 2 link:

https://drive.google.com/file/d/1ECYXlkF15n_l2KsMOTUB2ZSJMI6doqCD/vi

ew?usp=sharing

Unit 3 link: https://drive.google.com/file/d/1y9NTts5iAfO

G_V5WFcA9TqZZg1tAVIUE/view?usp=sha

<u>ring</u>

Unit 4 link:

https://drive.google.com/file/d/113KvDQASle9tgzATOTKLOtIGa2_u8A_B/view?usp=drive_link

Unit5link:

https://drive.google.com/file/d/132Ovh44E9E_sb4QD5agUA2F9UpzBYO1B/view?usp=drive_link



Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956

(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), RangaReddy Dist., Telangana–501510 Website: https://siiet.ac.in/

Power point presentation

PPT link:

https://docs.google.com/presentation/d/18OkUb6NIO8IH5M3l4L_a6zy83VdN57kd/edit?usp=sh aring&ouid=115911641205636277165&rtpof=true&sd=true

Code No: 154BH JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech II Year II Semester Examinations, April/May - 2023 LINEAR IC APPLICATIONS (Common to ECE, EIE)

Time: 3 Hours

Max. Marks: 75

Note: i) Question paper consists of Part A, Part B.

- ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
- iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

De	fine slew rate and PSRR.	[2]
b)	What are the properties of dual input unbalanced output differential amplifier?	[3]
c)	What is a voltage regulator? Mention types of voltage regulators.	[2]
d)	Explain how comparator is used as level detector.	[3]
e)	What are the characteristics of all pass filters?	[2]
f)	The resonant frequency f_0 of a band pass filter is 1 kHz and its bandwidth is 3 kHz	Iz. Find
	the value of Q.	[3]
g)	Why control terminal of IC 555 timer is connected to ground through a 0.01μ F	bypass bypass
	capacitor?	[2]
h)	Define capture range and Lock range in PLL.	[3]
i)	Which is the fastest ADC and why it is so?	[2]
j)	The LSB of a 10-bit DAC is 20 mV. Calculate the output voltage for an input,	
	1011001101.	[3]

PART – B

(50 Marks)

- 2.a) Explain about DC coupling and cascaded differential amplifier stages.
- b) What is an Op-amp? Briefly explain the function of different stages of an Op-amp with respect to its block schematic. [5+5]

OR

- 3.a) The two input terminals of an op-amp are connected to voltage signals of strength 745 μ V and 740 μ V respectively. The gain of the OP-AMP in differential mode is 5 ×10⁵ and its CMRR is 80dB. Calculate the output voltage and percentage error due to common mode.
 - b) Draw the circuit diagram of non-inverting amplifier and explain its working. [5+5]
- 4.a) Design an instrumentation amplifier to have a variable differential gain in the range 5-200. Use a 50 kilo-ohm potentiometer.
 - b) Draw the circuit diagram of an integrator and explain its working. [5+5]

5.a)	Describe the working of practical differentiator circuit. Derive the expression for output voltage.
b)	Explain the monostable multivibrator operation by using op amp. [5+5]
6.a)	Discuss in detail about band pass filter with neat sketch.
b)	Explain the operation of the second order low pass Butterworth filter. [5+5] OR
7.a)	Explain, how to obtain triangular wave using a square wave generator.
b)	What is VCO, draw and explain the functional block diagram of VCO.[5+5]
8.a)	Explain the monostable operation of 555 IC timer with neat sketch.
b)	Draw and explain the circuit of an astable multivibrator using 555 timer. [5+5] OR
9.a)	Draw and explain the principles and description of individual blocks of PLL in detail.
b)	Compute the free running frequency f _o , lock in range and capture range of PLL 565.
	Assume $R_T=20$ k-ohm, $C_T=0.01\mu$ F, $C=1\mu$ F and supply voltage is $\pm 6v$. [5+5]
10.a)	What are the draw backs of weighted resistor DAC? How they can be overcome by using
	R-2R ladder DAC.
b)	Find out step size and analog output for 4-bit R-2R ladder DAC, when input is 0 1 1 1
	and 1 1 1 1, assume $V_{ref} = +5V$. [5+5]
	<u>OD</u>

OR

11.a) With neat sketch explain the principle and operation of successive approximation ADC.b) Enlist the advantages and disadvantages of dual slope ADC. [5+5]

Code No: 154BH JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech II Year II Semester Examinations, August/September - 2021 LINEAR IC APPLICATIONS (Common to ECE, EIE)

Time: 3 Hours

Answer any five questions All questions carry equal marks

- 1.a) Derive closed loop voltage gain, input resistance, output resistance and band width for inverting amplifier with feedback arrangement.
 - b) Differentiate the functional classification of the differential amplifiers used in the first two stages of Op-amp. [8+7]
- 2.a) List and explain DC characteristics of op-Amp.
 - b) Brief out the classification of ICs.
- 3.a) Discuss the necessity of negative feedback in amplifier applications. How does negative feedback affect the performance of an inverting amplifier?
- b) Write about the sampling process and its requirement and explain the basic circuit for sample and hold circuit. [8+7]
- 4.a) Discuss the design of differentiators and integrators in brief.
- b) Design a practical integrator circuit to process input sinusoidal wave forms up to 1 kHz with given input amplitude is 10mV. [7+8]
- 5.a) Explain the classification and operation of all types of filters with their characteristics.
- b) Design square waveform generator circuit using op-Amp and then explain the same.

[6+9]

- 6.a) Design Band pass circuit using op-Amp.
- b) Design Wein-bridge oscillator using op-Amp and then derive its expression for frequency of oscillations. [5+10]
- 7.a) Draw the circuit of Schmitt trigger using 555 timer and explain its operation.
- b) Design a 555 Astable multivibrator to operate at 10 KHz with 40% duty cycle. [7+8]
- 8.a) Mention about the weighted resistor DAC and R-2R ladder DAC design.
- b) Draw the schematic circuit diagram of a counter type A/D converter and explain the operations of the system. [8+7]

---00000----

Max. Marks: 75

[10+5]



Code No: 154BH JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech II Year II Semester Examinations, August/September – 2022 LINEAR IC APPLICATIONS (Common to ECE, EIE)

Time: 3 Hours

Answer any five questions All questions carry equal marks

Draw and explain the equivalent circuit of an operational amplifier.

- b) An input of 3V is fed to the non-inverting terminal of an op-amp. The amplifier has a R_i of 10 K Ω and R_f of 10 K Ω . Find the output voltage.
- c) Write all the DC and AC characteristics of an ideal OP-AMP with relevant expressions. [7+4+4]
- 2.a) Sketch an instrumentation amplifier using 3 Op-Amp and derive its output voltage equation.
- b) What is a comparator? With neat circuit diagram, explain its characteristics. [8+7]
- 3.a) Discuss a sample and hold circuit and explain its operation.
- b) Explain the op-amp multiplier in detail. [8+7]
- 4.a) What is VCO? Explain its operation with neat diagram.
- b) Design and draw the square wave generator using op-amp and explain its operation.

[7+8]

Max. Marks: 75

- 5.a) Design a second order Butterworth LPF operating at a frequency of 4KHz.
 - b) Design RC phase shift oscillator using op-amp and derive the necessary expression.

[7+8]

- 6.a) Explain the operation of a monostable multivibrator using 555 timer? Also derive pulse Width.
- b) Draw the circuit of Schmitt trigger using IC555 timer and explain its operation. [7+8]
- 7.a) With neat block diagram, explain successive approximation type A/D converter in detail.b) Draw and explain the operation of counter type ADC. [7+8]
- 8.a) Draw and explain the operation of weighted resistor DAC.
- b) Discuss the specifications of DAC's. [8+7]

Code No: 154BH JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech II Year II Semester (Special) Examinations, January/February - 2021 LINEAR IC APPLICATIONS (Electronics and Communication Engineering)

Time: 2 Hours

Answer any Five Questions All Questions Carry Equal Marks

Max. Marks: 75

- 1.a) Explain different modes of operation of op-Amp.
 - b) What is level translator? Explain the necessity of level translator stage in cascading differential amplifiers. [8+7]
- 2.a) Explain the term slew rate and write its importance in op-amp circuits.
- b) For the given dual-input, balanced-output differential amplifier $R_C = 2.2 \text{ k}\Omega$, $R_E = 4.7 \text{ k}\Omega$, $R_{in1} = R_{in2} = 50 \Omega$, $V_{CC} = +10 \text{ V}$, $V_{EE} = -10 \text{ V}$, $\beta_{DC} = \beta_{AC} = 100$ and $V_{BE} = 0.71 \text{ V}$, determine I_{CQ} , V_{CEQ} , r_e , voltage gain, input and output resistances. [7+8]
- 3. What is the necessity of Instrumentation amplifier? Design Instrumentation amplifier using op-amp. Also, explain the advantages of it. [15]
- 4. Design the following using OP-Amps:
 a) V-to-I converter
 b) I to V converters.
 Also, give their applications.
- 5. Draw and explain the operation of Wein bridge oscillator and derive its frequency of oscillation. [15]
- 6. Write the design steps of the second order low pass filter and design it using OP-Amp. [15]
- 7. Draw and explain the Manostable mode of operation of 555IC timer and also derive its pulse with expression. [15]
- 8.a) Draw and explain the successive approximation ADC.b) List and explain specifications of ADC. [8+7]

Code No: 154BH JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech II Year II Semester Examinations, November/December - 2020 LINEAR IC APPLICATIONS (Common to ECE, EIE)

Time: 2 Hours

Answer any Five Questions All Questions Carry Equal Marks

Max. Marks: 75

1.a) b)	Perform AC analysis of single input dual output differential amplifier Configu List out the features of ideal OP-Amp.	ration. [10+5]
2.a)	What are the differences between the inverting and non inverting terminals? you mean by the term "virtual ground"?	What do
b)	List out AC and DC characteristics of OP-AMP.	[7+8]
3.a)	Draw the circuit diagram of instrumentation amplifier using 741 op-amp and e operation.	explain its
b)	How OP-AMP is used as integrator? Explain its working.	[9+6]
4.a) b)	How OP-AMP is used as Comparator? Explain its working. How OP-AMP is used as Arithmetic circuits? Explain its working.	[6+9]
5.a) b)	Design a active high pass filter with cutoff frequency of 4 KHz. Explain the working principle of Wein Oscillator.	[7+8]
6.a)	How to generate a Saw tooth waveform? Explain the working of such a circuit neat circuit diagram	t with a
b)	Discuss in detail about band pass and band reject filters.	[8+7]
De	escribe the 555 timer monostable multivibrator applications in: i) Frequency divider ii) Pulse width modulation.	
b)	Explain the terms frequency multiplication, frequency translation of PLL.	[8+7]
8.a)	What is the conversion time of a 10 bit successive approximation ADC if its in is 5 MHz?	nput clock
b)	List and explain the specifications of DAC.	[6+9]

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 Mid Examinations IIII V 2022 т

	Sheriguda (V), Ibrahimpatnar I - Mid Examination	n (M), R.R.I ns, JULY - 2	Dist-501 510 2 023	Set -I			
Year a Subjec	&Branch: II –ECE (A&B) et: LINEAR IC APPLICATIONS Max. Ma	urks: 10		Date:11/07/23(AN) Time: 60 mins			
Aı	Answer any TWO Questions. All Question Carry Equal Marks 2*5=10 marks						
1.	Explain practical inverting amplifier?	5	(C224.1)	(COMPREHENSION)			
2	Explain in detail DC and AC Characteristics of an op-amp?	5	(C224.1)	(COMPREHENSION)			
3	Derive the output voltage and frequency response of the practical Differentiator?	5	(C224.2)	(ANALYSIS)			
4	Define active filters? Derive the equation for first order low pass Filter?	5	(C224.3)	(KNOWLEDGE)			



Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

II - Mid Examinations, SEP -2023

Set -II

Yea Subj	* &Branch: II –ECE(A&B) ect: LINEAR IC APPLICATIONS Max. Ma	rks: 10		Date: 13 /09/23(AN) Time: 60 mins				
	Answer any TWO Questions. All Question Carry Equal Marks2*5=10 marks							
1.	Draw the basic circuit of RC-Phase Shift Oscillator and explain its operation. Also derive the expression for frequency of oscillations.	5	(C224.3)	(Application)				
2.	Describe the working of an Astable multivibrator using IC555 with circuit diagram.	5	(C224.4)	(Knowledge)				
3.	Draw the circuit diagram of Weighted Resistor DAC and explain the operation in detail.	5	(C224.5)	(Comprehension)				
4.	Explain in detail specifications of ADC/DAC Converter.	5	(C224.5)	(Comprehension)				



DEPARTMENT OF ECE

B.Tech II Year II Sem I Mid –Term Examination, JULY-2023

<u>LINEAR IC APPLICATIONS</u> (Objective Exam)

DATE:11/07/2023(AN)	TIME: 20 Min	МАХ	K.MARKS: 10
NAME:	ROLL NO:	MARKS:	
I. CHOOSE THE CORREC	Γ ALTERNATIVE:	<u>10X0.5</u>	<u>=5M</u>
 In IC's all the active as Along with inter connections are i a) Hybrid b) Thick and Thin 	s well as passive elements co integrated on a single crysta c) Monolithic d) None	omponents l	[]
2. If input to the integrator is Unit sta) Positive going rampb) Neg	tep signal. Output is gative going ramp c) U	Unit step only d) Impu	[] lse signal
3. How many gates can design on M a) 3 to 30 b) 30 to 300 c)	1SI 300 to 3000 d) All c	of the above	[]
4. Open loop gain of an Ideal OP-A a) 0 b) 1 c) -1	Amp. d) infinite		[]
5. Choose the limitation of an Integrala) Less weightb) Less heat of	rated Circuit. dissipation c) Less co	st d) Less Power consu	[] Imption
6. Which is not the internal circuit of a) Differential Amplifier b) Lev	of Operational Amplifier vel Translator c) Output	Driver d) Clamper	[]
7. The Output of the Inverting amplea) 180 degree out of phasec) -180 degree out of phase	ifier with respect input is b) 180 degree in phase d) -180 degrees out of phase	se	[]
8. The Overall voltage gain of an In	verting amplifier, If R1=10	kohms, Rf= 100Kohms	
 a) -1 b) -10. c 9. What are the applications of com a) Zero crossing detectors. b) A 	adder c) Subtractor	d) Multiplexer	[]
10. The output of Comparatora) Sine waveb) Square Wa	ave c) Triangular Wav	e d) Sawtooth Wave	[]

II. Fill in the Blanks:

10X0.5=5M

1. The difference between the two input bias currents when the output voltage is Zero is called 2. The Output equation of differentiator is _____ 3. What is CMRR _____ 4. The Gain of Non-Inverting Amplifier _____ 5. The Output equation of Integrator is _____ 6. The output of Voltage follower _____ 7. The Output voltage of inverting summer _____ 8. What is the functions of op-amp pin number 2, 5, 7 _____ 9. Instrumentation amplifier is also called as _____ 10. What are the types of V to I Converter _____

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY DEPARTMENT OF ECE

B. Tech II Year II Sem II Mid – Term Examination, SEP-2023

LICA

DATE: 13/09/2023 (AN)	(Objective E TIME: 20 Min	xam) MAX.MARKS: 10
NAME:	ROLL NO:	
I. CHOOSE THE CORRECT A	LTERNATIVE:	<u>10X0.5=5M</u>
 Filters are classified as a) Analog or digital c) Audio or radio frequency 	b) Passive or actived) All of the above	[]
2.Given the lower and higher cut-obandwidth.a) 750 Hzc) 75000 Hz	off frequency of a band-pas b) 7500 Hz d) None of the above	ss filter are 2.5kHz and 10kHz. Determine its []
3. IC 555 Timer is used for generala) Accurate time delay from micc)Only days	ting ro sec to hrs b) Accur d)Only h	[] rate time delay from hrs to days nours
4. The time period for Monostable a) 0.69RC b) 1.1 RC	c) .45RC	[] d) 0.405RC
5is defined as the ratio a) Duty cycle b) Timer	o of ON time to the total tin c) oscillations	ne period. [] d) Multivibrator
6. Which A/D converter is considerablea) Servo Converterc) Counter type	ered to be simplest, fastest a b) flash type converter d) All of the above	and most expensive []
7. The Phase locked loop principlea) Motor speed controlsc) FM Demodulation	e has been used in application b) tracking filters d)All of the above	on such as []
8is defined as the range frequency fina) Capture range b) lock ran	e of frequency over which t ge c) pull in time	the PLL system follows the change in the input [] d) none of the above
9circuit uses a su trial and errora) Successive approximationc) Counter type	ccessive approximation reg b) flash type d) tracking s	gister to find the required value of each bit by [] converter ervo type
10. Applications of IC-555 timer aa) FSK generatorb) 1	estable multivibrator are PPM c) A&B	[] d) None of the above

II. Fill in the Blanks:

<u>10X0.5=5M</u>

1. Write the voltage gain formula of Low Pass Filter_____

2. A first order low pass Butterworth filter is realized by RC network and _____

3. A monostable 555 timer has the _____ no of stable states

4. Monostable multivibrator needs _____

5. Square wave generator is an application of _____

6. Example of ADC technique is _____

7 .VCO is also called as _____

8. Astable multivibrator is also called as _____

10. Write the IC555 pin description of Pins 2,3 &6------.

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501510 B-Tech I-Mid Examinations, JULY-2023

Year& Branch: II–ECE-A & B Date: 11-07-2023(AN) Subject : LICA

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1-zu1OuYhTfUFOno291-0nlV8_32LvwsI/view?usp=drive_linkObjective Key Paper

I. CHOOSE THE CORRECT ALTERNATIVE:

- 1. c
- 2. a
- 3. b
- 4. d
- 5.b
- 6. d
- 7. a
- 8. b
- 9.a
- 10. b

II. FILL IN THE BLANKS:

- 1. Input offset current
- 2. $V0= -C1 \text{ RF } \frac{d}{dt} \text{ Vin}$ 3. $\frac{Ad}{Ac}$ 4. $(1 + \frac{Rf}{R1})$ 5. $\frac{-1}{Cf Rf} \text{ Vin}$ 6. V0 = Vin7. V0 = -(V1 + V2)8. Inverting, offset null, positive supply voltage 9. Data amplifier
- 10. floating load & grounded load

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501510 B-Tech II-Mid Examinations, SEP-2023

Year& Branch: II–ECE-A & B Date: 13-09-2023(AN) Subject: LICA

ANSWERKEY

Descriptive paper key link:

https://drive.google.com/file/d/1L9oZqCXGiEzrnf7g3Uf79w4TFrTN_dEU/view?usp=sharingObjective/Q uiz

uiz

Key Paper

I.CHOOSE THE CORRECT ANSWERS

- 1. b
- 2. b
- 3. a
- 4. b
- 5. a
- 6. b
- 7. d
- 8. b
- 9. a

10. b

II. FILL IN THE BLANKS

 $1. \frac{AF}{}$ $\sqrt{1+(\frac{f)^2}{fc}^2}$

2. op-amp

3. Single (1)

4. External trigger pulse

5. Astable multi vibrator

6. Mobile phone

7. Voltage to frequency converter

8. Free running

9. Lock in range, capture range ,pull in time

10. Trigger input, output, threshold



Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956

(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510

Website: https://siiet.ac.in/

ASSIGNMENT-1

SUBJECT: Linear IC Applications

- 1. Explain the AC & DC characteristics of op-amp and its features? (C224.1) (COMPREHENSION)
- 2. Derive the gain expression for practical inverting amplifier? (C224.1) (COMPREHENSION)
- 3. What is op-amp? Explain its ideal characteristics of op-amp and its features?

(C224.2) (ANALYSIS)

4. Derive the output voltage and frequency of practical Differentiator?

(C224.2) (ANALYSIS)

5. What is instrumentation amplifier? And explain three op-amp instrumentation amplifiers?

(C224.3) (ANALYSIS)



Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), RangaReddy Dist., Telangana–501510 Website: https://siiet.ac.in/

ASSIGNMENT-2

SUBJECT: Linear IC Applications

1. Draw the basic circuit of RC-Phase Shift Oscillator and explain its operation. Also derive the expression for frequency of oscillations. (C224.3) (APPLICATION)

2. Describe the working and Operation of IC555 Timer and also its PIN diagram in detail? (C224.4) (ANALYSIS)

3. Explain the working of each block in PLL in detail? (C224.4) (COMPREHENSION)

4. Explain the working of R-2R ladder DAC with neat circuit diagram?

(C224.5) (COMPREHENSION)

5. Explain the working of weighted Resistor DAC with neat circuit diagram? (C224.5) (COMPREHENSION)



Accredited by NAAC with A+ Grade, Recognized under2 (f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510 Website: https://siiet.ac.in/

RESULT ANALYSIS TO IDENTIFY SLOW AND ADVANCED LEARNERS

Course Title	Linear IC Applications
Course Code	EC404PC
Programme	B. Tech
Year & Semester	II year I-semester, B sec
Regulation	R18
Course Faculty	P.KAVITHA, Assistant Professor, ECE

Slow Learners:

S. No	Roll Number	No. of Backlogs	MID-I Marks	MID-2 Marks
1	21X31A0440	58	17	20
2	21X31A0441	4S	14	18
3	21X31A0443	58	18	22
4	21X31A0445	58	14	18
5	21X31A0448	58	21	23
6	21X31A0450	58	14	18
7	21X31A0453	58	17	22
8	21X31A0455	4S	20	22
9	21X31A0456	58	21	21
10	21X31A0457	38	14	18
11	21X31A0458	58	15	20
12	21X31A0460	58	18	22
13	21X31A0470	4S	23	23
14	22X35A0424	4S	20	22
15	22X35A0427	58	17	20
16	22X35A0428	4S	18	22
17	22X35A0433	58	16	18

18	22X35A0435	4S	19	22
19	22X35A0436	4S	24	23
20	22X35A0439	38	20	22
21	22X35A0441	58	16	18

Advanced Learners (From II-I Result Analysis having <=2 backlogs):

Total 34 advanced learners are identified.

S .No	Roll Number	GATE Material Provided
1	21X31A0438	
2	21X31A0442	
3	21X31A0444	
4	21X31A0446	
5	21X31A0447	complexity, basic information of Op-
6	21X31A0449	AC Characteristics, 741 op- amp and
7	21X31A0451	its features, modes of operation- inverting, non-inverting, differential,
8	21X31A0452	differentiators and integrators, Schmitt
9	21X31A0454	- trigger, Multivibrators, 1st order LPF, HPF filters, waveform generators -
10	21X31A0459	- triangular, saw tooth, square wave and VCO. Introduction to 555 timer,
11	21X31A0461	functional diagram, monostable and astable, PLL - introduction, block
12	21X31A0462	schematic, principles, basic DAC techniques, weighted resistor DAC, R-
13	21X31A0463	2R ladder DAC
14	21X31A0464	
15	21X31A0465	
16	21X31A0466	
17	21X31A0467	
18	21X31A0468	
19	21X31A0469	
20	21X31A0471	
21	21X31A0472	
22	22X35A0421	

23	22X35A0422
24	22X35A0423
25	22X35A0425
26	22X35A0426
27	22X35A0429
28	22X35A0430
29	22X35A0431
30	22X35A0432
31	22X35A0434
32	22X35A0437
33	22X35A0438
34	22X35A0440
1	



Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956

(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga ReddyDist., Telangana–501510

Website: https://siiet.ac.in/

BATCH ECE-II BTECH II SEM ECE-A RESULT ANALYSIS

ACADAMIC	COURSE	NUMBE STUDE	CROF ENTS	QUESTIO SETT	NPAPER 'ING	
YEAR	NAME	APPEARED	PASSED	INTERNAL	EXTERNAL	PASS%
2022-23	Linear IC Applications	57	37	COURSE FACULTY	JNTUH	64.9



Linear IC APPLICATIONS (C224) RESULT ANALYSIS



(An Autonomous Institution under UGC) Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad) Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510 Website: https://siiet.ac.in/

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

REMEDIAL CLASSES TIME TABLE

A.Y 2022-23

SEMESTER-II

BRANCH/ SEC	MON 4.00 PM- 5.00 PM	TUE 4.00 PM- 5.00 PM	WED 4.00 PM- 5.00 PM	THUR 4.00 PM- 5.00 PM	FRI 4.00 PM- 5.00 PM
II ECE-A	EMF&W	LTNM	A&DC	LICA	ECA
II ECE-B	LICA	A&DC	EMF&W	ECA	LTNM
III ECE-A	DSP	VLSID	A&P	ESD	IM
III ECE-B	A&P	ESD	DSP	IM	VLSID
III ECE-C	IM	A&P	ESD	VLSID	DSP
IV ECE-A	WSN	ML	LPVLSID	-	-
IV ECE-B	ML	LPVLSID	WSN	-	-
IV ECE-C	LPVLSID	WSN	ML	-	-

TIEBOLOT THE LIPPAFTMENT Electronics and Communication Engg. Depi SRI INDV INSTITUTE OF ENGG & TECH SNAMMARIN BANK MARKAN DEPARTMENT Ski INUV INSTITUTE UF ENGU & TEUN Shenguda(V), brehimpetham(M), R.R.Dist-501 514

PRIN CIPAL. PRINCIPAL Sn Indu Institute of Engineering & Tech Sheriguda(Vill), Ibrahimpa R Dist Telangana -501 510



Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty :FBranch & Section:FCourse Name:F

P.KAVITHA ECE - B LINEAR IC APPLICATIONS Academic Year: 2022-2023 Examination: I Internal Year: II Semester: II

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj1	A1
Max	. Marks ==>	5		5		5		5		10	5
1	21X31A0438	5		5						5	5
2	21X31A0439							4		5	5
3	21X31A0440	5		2						5	5
4	21X31A0441	5		5							5
5	21X31A0442	5		5						5	5
6	21X31A0443	3		5						5	5
7	21X31A0444	5		5						4	5
8	21X31A0445					4				5	5
9	21X31A0446	5				5					5
10	21X31A0447	5		5						5	5
11	21X31A0448	5		2						5	5
12	21X31A0449	4		2						5	5
13	21X31A0450	4		2						3	5
14	21X31A0451	5		5						5	5
15	21X31A0452	5		5						4	5
16	21X31A0453	1		5						5	5
17	21X31A0454			5						2	5
18	21X31A0455	2		4						3	5
19	21X31A0456	3		3						3	5
20	21X31A0457					4				5	5
21	21X31A0458			3						5	5
22	21X31A0459			5		5				6	5
23	21X31A0460			5						5	5
24	21X31A0461	3		1						3	5
25	21X31A0462	5		2						4	5
26	21X31A0463	5		2						3	5
27	21X31A0464	4		5						5	5
28	21X31A0465	5		5						5	5
29	21X31A0466	3		5						5	5
30	21X31A0467	3						4		4	5
31	21X31A0468	2				3				4	5
32	21X31A0469	5		5						5	5
33	21X31A0470	3		5						5	5
34	21X31A0471	5		1						6	5
35	21X31A0472	5		5						7	5
36	22X35A0421	5		5						7	5
37	22X35AU422	4				5				2	5
38	22X35AU423	5		5						4	5
39	22X35AU424	5		4						4	5
40	22X35AU425	5		5						3	5
41	22X35AU426	5		5						3	5
42	22X35A0427	4				5				4	5

10 0000510100		1			_			r 1	-	Τ
43 22X35A0428	4				5				3	5
44 22X35A0429	5		4						4	5
45 22X35A0430	5		3						5	5
46 22X35A0431			5		5				9	5
47 22X35A0432	5		5						9	5
48 22X35A0433					4				9	5
49 22X35A0434	5		5						4	5
50 22X35A0435			2						4	5
51 22X35A0436					4				5	5
52 22X35A0437	3								8	5
53 22X35A0438			5		5				7	5
54 22X35A0439	3		1						6	5
55 22X35A0440	2				3				2	5
56 22X35A0441			2						2	5
arget set by the faculty HoD	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Sumber of students										
erformed above the	39	0	32	0	13	0	2	0	10	56
arget							<u> </u>			
Sumber of students	42	0	12	0	12	0	2	0	51	56
ttempted	43	U	43	U	13	U	2	0	54	30
ercentage of students	010/		7 40 /		10001		10001		100/	1000/
cored more than target	91%		74%		100%		100%		19%	100%
O Monning with Evon	n Ouesti	onsi								4
O Wrapping with Exam	l Questi	<u>0115:</u>								T
CO - 1									Y	Y
CO - 2									Y	Y
CO - 3									Y	Y
CO - 4										
CO - 5										
CO - 6										
	-									
% Students Scored										
>Target %	91%		74%		100%		100%		19%	100%
CO Attainment based of	n Exam	Ouestio	ns:							
CO - 1									10%	100%
CO 2									1970	10070
0 - 2									19%	100%
CO - 3									19%	100%
CO - 4									ļ	
CO - 5									ļ	
CO - 6									<u> </u>	
	•									
СО	Subj	obj	Asgn	Ove	erall	Le	evel		Attain	ment Le
CO-1		19%	100%	59	%	2	.00		1	40%
CO-2		19%	100%	59	%	2	.00		2	50%
CO-3	1	19%	100%	59	%	2	.00	1	3	609
	1						-	1 1		1 207
CO-4										
CO-4										
CO-4 CO-5										



Department of Electronics and Communication Engineering Course Outcome Attainment (Internal Examination-2)

Name of the faculty : P.KAVITHAAcademic Year:Branch & Section:ECE - BExamination:

Course Name:

ECE - BExamination:LINEAR IC APPLICATIONSYear: II

on: II Internal Semester: II

2022-2023

47 22X35A0432					5		5		10	5	
48 22X35A0433			4						10	5	
49 22X35A0434			5		4				10	5	
50 22X35A0435			5		4				10	5	
51 22X35A0436			5		4				10	5	
52 22X35A0437			5		5				9	5	
53 22X35A0438					5				10	5	
54 22X35A0439			4		3				10	5	
55 22X35A0440			5		3				10	5	
56 22X35A0441			3		1				9	5	
Target set by the	2.00	0.00	2.00	0.00	2.00	0.00	3 00	0.00	6.00	2.00	
faculty / HoD	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	0.00	5.00	
Number of students											
performed above the	5	0	39	0	37	0	16	0	51	56	
target											
Number of students	7	0	42	0	40	0	16	0	56	56	
attempted	/	0	42	0	40	0	10	0	50	50	
Percentage of students										7	
scored more than	71%		93%		93%		100%		91%	100%	
target											
CO Mapping with Exa	am Ques	tions:	-								
CO - 1											
CO - 2											
CO - 3											
CO - 4	Y								Y	Y	
CO - 5	-		Y		Y				Y	Y	
CO - 6							Y		Y	Y	
	1	I	1			I	r				
% Students Scored	710/		0.20/		020/		1000/		010/	1000/	
>1 arget %	/1%		93%		93%		100%		91%	100%	
CO Attainment based	on Exai	n Ques	<u>stions:</u>		1	<u>r</u>	1				
CO - 1											
CO - 2											
CO - 3											
CO - 4	71%								91%	100%	
CO - 5			93%		93%				91%	100%	
CO - 6							100%		91%	100%	
CO	Subj	obj	Asgn	0	verall	Le	evel		Attain	ment Level	1
CO-1									1	40%	1
CO-2									2	50%	,
CO-3	1								3	60%	,
CO-4	71%	91%	100%	S.	8%	3	00		-		
	020/	010/	10070		50/	2	00				
CO-5	93%	91%	100%	9	5%0	3	.00				
CO-6	100%	91%	100%	9	7%	3	.00				

Attainment (Internal Examination-2 3.00



Department of Electronics and Communication Engineering
 Course Outcome Attainment (University Examinations)

 Name of the faculty : P.KAVITHA
 Academic Year:
 20

Name o	of the faculty :	P.KAVITHA		Academic Y	ear:	
Branch	& Section:	ECE - B		Year / Seme	ester:	
Course	Name:	LINEAR IC APPLICAT	IONS			
S.No	Roll Number	Marks Secured		S.No	R	
1	21X31A0438	26		36	22	
2	21X31A0440	9		37	22	
3	21X31A0441	6		38	22	
4	21X31A0442	26		39	22	
5	21X31A0443	0		40	22	
6	21X31A0444	32		41	22	
7	21X31A0445	1		42	22	
8	21X31A0446	29		43	22	
9	21X31A0447	35		44	22	
10	21X31A0448	4		45	22	
11	21X31A0449	13		46	22	
12	21X31A0450	0		47	22	
13	21X31A0451	31		48	22	
14	21X31A0452	27		49	22	
15	21X31A0453	11		50	22	
16	21X31A0454	31		51	22	
17	21X31A0455	7		52	22	
18	21X31A0456	1		53	22	
19	21X31A0457	8		54	22	
20	21X31A0458	2		55	22	
21	21X31A0459	34				
22	21X31A0460	1				
23	21X31A0461	40				
24	21X31A0462	26				
25	21X31A0463	35				
26	21X31A0464	28				
27	21X31A0465	27				
28	21X31A0466	26				
29	21X31A0467	32				
30	21X31A0468	28				
31	21X31A0469	26				
32	21X31A0470	36				
33	21X31A0471	26				
34	21X31A0472	35				
35	22X35A0421	27				
Max Ma	arks	75		F	-	
Class A	verage mark		26]	Atta	
Number of students performed above the target 37						
Number	r of successful st	tudents	55]		
				-		

S.No	Roll Number	Marks Secured				
36	22X35A0422	32				
37	22X35A0423	29				
38	22X35A0424	26				
39	22X35A0425	26				
40	22X35A0426	26				
41	22X35A0427	1				
42	22X35A0428	14				
43	22X35A0429	26				
44	22X35A0430	26				
45	22X35A0431	37				
46	22X35A0432	54				
47	22X35A0433	0				
48	22X35A0434	46				
49	22X35A0435	26				
50	22X35A0436	35				
51	22X35A0437	5				
52	22X35A0438	49				
53	22X35A0439	7				
54	22X35A0440	39				
55	22X35A0441	26				

2022-2023

II / II

Attainment Level	% students
1	40%
2	50%

Percentage of students scored more than target	67%
Attainment level	3



Department of Electronics and Communication Engineering Course Outcome Attainment

Name of the faculty :	P.KAVITI	HA		Academic Year:	2022-2023
Branch & Section:	ECE - B		Examination:	I Internal	
Course Name:	LINEAR IO	C APPLICATIONS		Year:	II
				Semester:	II
Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	2.00		2.00	3.00	2.75
CO2	2.00		2.00	3.00	2.75
CO3	2.00		2.00	3.00	2.75
CO4		3.00	3.00	3.00	3.00
CO5		3.00	3.00	3.00	3.00
CO6		3.00	3.00	3.00	3.00
Inter	nal & Unive	ersity Attainment:	2.50	3.00	
		Weightage	25%	75%	
CO Attainment for the	e course (In	ternal, University)	0.63	2.25	
CO Attainment for	the course (Direct Method)		2.88	

Overall course attainment level

2.88



Department of Electronics and Communication Engineering <u>Program Outcome Attainment (from Course)</u>

Name of Faculty:	P.KAVITHA	Academic Year:	2022-2023
Branch & Section:	ECE - B	Year:	II
Course Name:	LINEAR IC APPLICATIONS	Semester:	II

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	3	1	-	-	-	-	-	-	3	1	2
CO2	3	3	2	-	-	-	-	-	-	-	-	2	1	2
CO3	3	3	2	-	-	-	-	-	-	-	2	2	1	1
CO4	3	2	1	-	-	-	-	-	-	-	-	-	1	2
CO5	3	3	3	-	2	-	2	-	-	-	2	2	2	2
CO6	3	2	2	-	-	-	-	-	-	2	-	-	2	2
Course	3	2.5	2	3	2	-	2	-	-	2	2	2.3	1.333	1.83

со	Course Outcome Attainment
CO1	2.75
CO2	2.75
CO3	2.75
CO4	3.00
CO5	3.00
CO6	3.00
Overall course at	tainment level 2.88

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainme nt	2.88	2.40	1.92	2.88	1.92		1.92			1.92	1.92	2.24	1.28	1.76

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)



Accredited by NAAC with A+ Grade, Recognized under2(f) of UGC Act 1956 (Approved by AICTE, NewDelhi and Affiliated to JNTUH, Hyderabad) Khalsa Ibrahimpatnam , Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana–501510

Website: https://siiet.ac.in/

ASSIGNMENTS AND ATTENDANCE REGISTER

Assignment1 script link:

https://drive.google.com/file/d/1jk7qokJN_kQxBFLUju3qHBBjslLXe4l2/view?usp=sharing

Assignment2 script link:

https://drive.google.com/file/d/1GIV0cMm3yRTaGkLKnCMtrGHJUBuO7kTy/view?usp=sha ring

Attendance register link:

https://drive.google.com/file/d/12m5qQBIRrLszrRlpt37ejrqTEJnKCzNy/view?usp=sharing