Sri Indu Institute of Engineering & Technology

Recognized Under 2(f) of UGC Act 1956
Approved by AICTE, New Delhi
Affiliated to JNTUH, Hyderabad.

COURSE FILE

ON

VLSI DESIGN

Course Code – EC603PC

III B.Tech II-SEMESTER

A.Y.: 2022-2023

Prepared by

Mr. K. SRIKANTH
Assistant Professor

Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year	2022-2023
Course Title	VLSI DESIGN
Course Code	EC603PC
Programme	B.Tech
Year & Semester	III year II-semester
Branch & Section	ECE-B
Regulation	R18
Course Faculty	Mr. K. SRIKANTH, Assistant Professor

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INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To Continuous assess of teaching-learning process through institute-industry collaboration.

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.

IM4: To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

DM1: To facilitate an academic environment that enables student's centric learning.

DM2: To provide state-of-the-art hardware and software technologies to meet industry requirements.

DM3: To continuously update the Academic and Research infrastructure.

DM4: To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

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PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

PEO1: Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.

PEO2: Graduates with ability to execute innovative ideas for Research and Development with continuous learning.

PEO3: Graduates inculcated with industry based soft-skills to enable employability.

PEO4: Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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PROGRAM OUTCOMES

1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

6. **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING
III YEAR COURSE STRUCTURE AND SYLLABUS (R18)
Applicable From 2018-19 Admitted Batch

III YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC501PC	Microprocessors & Microcontrollers	3	1	0	4
2	EC502PC	Data Communications and Networks	3	1	0	4
3	EC503PC	Control Systems	3	1	0	4
4	SM504MS	Business Economics & Financial Analysis	3	0	0	3
5		Professional Elective - I	3	0	0	3
6	EC505PC	Microprocessors & Microcontrollers Lab	0	0	3	1.5
7	EC506PC	Data Communications and Networks Lab	0	0	3	1.5
8	EN508HS	Advanced Communication Skills Lab	0	0	2	1
9	*MC510	Intellectual Property Rights	3	0	0	0
		Total Credits	18	3	8	22

III YEAR II SEMESTER

S. No.	**Course Code**	**Course Title**	**L**	**T**	**P**	**Credits**
1	EC601PC	Antennas and Propagation	3	1	0	4
2	EC602PC	Digital Signal Processing	3	1	0	4
3	EC603PC	VLSI Design	3	1	0	4
4		Professional Elective - II	3	0	0	3
5		Open Elective - I	3	0	0	3
6	EC604PC	Digital Signal Processing Lab	0	0	3	1.5
7	EC605PC	e – CAD Lab	0	0	3	1.5
8	EC606PC	Scripting Languages Lab	0	0	2	1
9	*MC609	Environmental Science	3	0	0	0
		Total Credits	**18**	**3**	**8**	**22**

***MC - Environmental Science – Should be Registered by Lateral Entry Students Only.**

Note: Industrial Oriented Mini Project/ Summer Internship is to be carried out during the summer vacation between 6th and 7th semesters. Students should submit report of Industrial Oriented Mini Project/ Summer Internship for evaluation.

Professional Elective – I

EC511PE	Computer Organization & Operating Systems
EC512PE	Error Correcting Codes
EC513PE	Electronic Measurements and Instrumentation

Professional Elective – II

EC611PE	Object Oriented Programming through Java
EC612PE	Mobile Communications and Networks
EC613PE	Embedded System Design

EC603PC: VLSI DESIGN

B.Tech. III Year II Semester **L T P C**

3 1 0 4

Prerequisite: Electronic Circuit Analysis; Switching Theory and Logic Design

Course Objectives: The objectives of the course are to:

1. Give exposure to different steps involved in the fabrication of ICs.
2. Explain electrical properties of MOS and BiCMOS devices to analyze the behavior of inverters designed with various loads.
3. Give exposure to the design rules to be followed to draw the layout of any logic circuit.
4. Provide design concepts to design building blocks of data path of any system using gates.
5. Understand basic programmable logic devices and testing of CMOS circuits.

Course Outcomes: Upon completing this course, the student will be able to

1. Acquire qualitative knowledge about the fabrication process of integrated circuits using MOS transistors.
2. Draw the layout of any logic circuit which helps to understand and estimate parasitic effect of any logic circuit
3. Design building blocks of data path systems, memories and simple logic circuits using PLA, PAL, FPGA and CPLD.
4. Understand different types of faults that can occur in a system and learn the concept of testing and adding extra hardware to improve testability of system.

UNIT – I

Introduction: Introduction to IC Technology – MOS, PMOS, NMOS, CMOS & BiCMOS

Basic Electrical Properties: Basic Electrical Properties of MOS and BiCMOS Circuits: Ids-Vds relationships, MOS transistor threshold Voltage, gm, gds, Figure of merit; Pass transistor, NMOS Inverter,Various pull ups, CMOS Inverter analysis and design, Bi-CMOS Inverters.

UNIT - II

VLSI Circuit Design Processes: VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits.

UNIT – III

Gate Level Design: Logic Gates and Other complex gates, Switch logic, Alternate gate circuits, Time delays, Driving large capacitive loads, Wiring capacitance, Fan – in, Fan – out.

UNIT - IV

Data Path Subsystems: Subsystem Design, Shifters, Adders, ALUs, Multipliers, Parity generators, Comparators, Zero/One Detectors, Counters.

Array Subsystems: SRAM, DRAM, ROM, Serial Access Memories.

UNIT - V

Programmable Logic Devices: Design Approach – PLA, PAL, Standard Cells FPGAs, CPLDs.

CMOS Testing: CMOS Testing, Test Principles, Design Strategies for test, Chip level Test Techniques.

TEXT BOOKS:

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition

2. CMOS VLSI Design – A Circuits and Systems Perspective, Neil H. E Weste, David Harris, Ayan Banerjee, 3rd Ed, Pearson, 2009.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

2. CMOS logic circuit Design - John. P. Uyemura, Springer, 2007.

3. Modern VLSI Design - Wayne Wolf, Pearson Education, 3rd Edition, 1997.]

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Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

Course: VLSI Design (C323) **Class: III ECE-A**

Course Outcomes

After completing this course, the student will be able to:

C323.1: Identify the various Fabrication techniques of IC using various MOS circuits and be able to Solve the electrical properties associated with MOS circuits. (Knowledge – Evaluation)
C323.2: Infer the steps involved in the VLSI design flow and apply the design rules of IC layout for designing stick, layout diagrams of various gates. (Comprehension – Synthesis)
C323.3: Apply Gate level design principles for the design of various logic gates and complex gates (Application - Synthesis)
C323.4: Contrast on the various techniques like Alternate gate circuits, Time delays, driving large capacitive loads and wiring capacitance (Analysis)
C323.5: Construct various data path and array subsystems for complex logic circuits and memory devices (Synthesis)
C323.6: Develop semiconductor IC design such as PLA's, PAL, FPGA, CPLDs and also assess the differential strategies for testing of IC's and CMOS. (Synthesis – Evaluation)

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C323.1	3	3	3	3	-	-	-	-	1	1	1	2	3	-
C323.2	3	3	3	3	2	-	-	-	1	1	1	2	3	2
C323.3	3	3	3	3	2	-	-	-	1	1	1	2	3	2
C323.4	3	2	2	2	-	-	-	-	1	1	1	2	3	1
C323.5	3	3	3	3	2	-	-	-	1	1	1	2	3	2
C323.6	3	3	3	3	2	-	-	2	1	1	1	2	3	2
C323	**3.00**	**2.83**	**2.83**	**2.83**	**2.00**	**-**	**-**	**2.00**	**1.00**	**1.00**	**1.00**	**2.00**	**3.00**	**1.80**

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CO- PO/PSO Mapping - Justification

Course: VLSI Design (C323) **Class: III ECE-A**

PO1.	**ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2.	**PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3.	**DESIGN/DEVELOPMENT OF SOLUTIONS:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate considerations for the public health and safety, and the cultural, societal, and environmental considerations.
PO4.	**CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
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PO8.	**ETHICS:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
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PO11.	**PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12.	**LIFE-LONG LEARNING:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.
PSO1.	**Design Skills:** Design, analysis and development a economical system in the area of Embedded system & VLSI design.
PSO2.	**Software Usage:** Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

JUSTIFICATION

C323.1: Identify the various Fabrication techniques of IC using various MOS circuits and be able to Solve the electrical properties associated with MOS circuits. (Knowledge – Evaluation)

PO1	Students apply the knowledge of science and engineering fundamentals to understand IC fabrication techniques
PO2	Students analyze the problems on various properties of IC
PO3	Students compute complex electrical properties of MOS circuits.
PO4	Students analyze and interpret the fabrication methods and properties of various semiconductor devices
PO9	Students perform individually to complete all assignments allotted on the topic
PO10	Students can share information about the complex problems on VLSI and assignments.
PO11	Students can use the Basics of VLSI in managing project work.
PO12	Students apply design principles and properties of various semiconductor devices for continuous learning
PSO1	Student can design, analysis and development a system in the area of VLSI design.

C323.2: Infer the steps involved in the VLSI design flow and apply the design rules of IC layout for designing stick, layout diagrams of various gates. (Comprehension – Synthesis)

	Justification
PO1	Students acquire knowledge on various types of methods and rules for IC design.
PO2	Students analyze the problems on the design of various semiconductor devices
PO3	Students are able to provide solution to design layout of IC using design rules
PO4	Students analyze and interpret the stick and layout diagrams of various devices
PO5	Students can use Xilinx vivado, micro wind and mentor graphics tool for design of layouts of CMOS inverter.
PO9	Students perform individually to complete all assignments allotted on the topic
PO10	Students can share information about the complex problems on VLSI and assignments.
PO11	Students can use the concept of VLSI Layout in managing project work.
PO12	Students apply the concepts of stick and layout diagrams for the design of various semiconductor devices as outcome based education on continuous learning
PSO1	Student can design, analysis and development a system in the area of VLSI design.
PSO2	Students can able to investigate and solve the engineering problems using Xilinx and micro wind.

C323.3: Apply Gate level design principles for the design of various logic gates and complex gates. (Application – Synthesis)

PO1	Students get the knowledge on analytical perspective on the design and analysis on IC fabrication.
PO2	Students analyze the problems on design principles
PO3	Students design and develop various circuits based on design rules for stick diagrams and layouts of an IC.
PO4	Students analyze and interpret the design of logic gates and complex gates
PO5	Students can use Xilinx vivado, micro wind and mentor graphics tool for design of layouts of logic gates.
PO9	Students perform individually to complete all assignments allotted on the topic
PO10	Students can share information about the complex problems on VLSI and assignments.
PO11	Students can use the concept of Gate level design in managing project work.
PO12	Students apply design principles for various semiconductor devices as continuous learning
PSO1	Student can design, analysis and development a system in the area of VLSI design.
PSO2	Students can able to investigate and solve the engineering problems using Xilinx and micro wind.

C323.4: Contrast on the various techniques like Alternate gate circuits, Time delays, driving large capacitive loads and wiring capacitance (Analysis)

PO1	Students get the knowledge on analytical perspective on the design and analysis on IC fabrication.
PO2	Students analyze the problems on various concepts
PO3	Students design and develop solutions for various circuits
PO4	Students analyze and interpret various techniques involved in design of IC
PO9	Students perform individually to complete all assignments allotted on the topic
PO10	Students can share information about the complex problems on VLSI and assignments.
PO11	Students can use the concept of Time delays and capacitive loads in managing project work.
PO12	Students apply the concepts of various design techniques for semiconductor devices as outcome based education on continuous learning
PSO1	Student can design, analysis and development a system in the area of VLSI design.
PSO2	Students can able to investigate and solve the engineering problems using Xilinx and micro wind.

C323.5: Construct various data path and array subsystems for complex logic circuits and memory devices (Synthesis)

PO1	Students get the basic knowledge which helps to understand and estimate the construction of logic circuit.
PO2	Students analyze the problems on the construction of various sub systems
PO3	Students design and develop solutions for complex logic circuits
PO4	Students analyze and interpret the construction of complex circuits and memory devices
PO5	Students can use Xilinx vivado, micro wind and mentor graphics tool for design of layouts.
PO9	Students perform individually to complete all assignments allotted to them
PO10	Students can share information about the complex problems on VLSI and assignments.
PO11	Students can use the concept of complex logic circuits and memory in managing project work.
PO12	Students apply the concepts of constructing various memory devices as outcome based education on continuous learning
PSO1	Student can design, analysis and development a system in the area of VLSI design.
PSO2	Students can able to investigate and solve the engineering problems using Xilinx and micro wind.

C323.6: Develop semiconductor IC design such as PLA's, PAL, FPGA, CPLDs and also assess the differential strategies for testing of IC's and CMOS. (Synthesis – Evaluation)

PO1	Students acquire knowledge on the development and testing of various semiconductor IC devices
PO2	Students analyze the problems on the development and testing of IC's
PO3	Students able to design different types of logic gates using CMOS inverter and analysis of their transfer characteristics and can also design building blocks of data paths using gates.
PO4	Students analyze and interpret the solutions for the development of testing of IC's
PO5	Students can use Xilinx vivado, micro wind and mentor graphics tool for design of layouts.
PO8	Understand different types of faults that can occur in a system and learn concept of testing and adding extra hardware to improve testability systems
PO9	Students perform individually to complete all assignments allotted on the topic
PO10	Students can share information about the complex problems on VLSI and assignments.
PO11	Students can use the concept of FPGA, CPLD in managing project work.
PO12	Students apply steps for development and testing of IC's as continuous learning
PSO1	Student can design, analysis and development a system in the area of VLSI design.
PSO2	Students can able to investigate and solve the engineering problems using Xilinx and micro wind.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

ACADEMIC CALENDAR 2022-23

B. Tech./B. Pharm. III YEAR I & II SEMESTERS

I SEM

S. No	Description	Duration	
		From	To
1	Commencement of I Semester classwork	**09.09.2022**	
2	1st Spell of Instructions (including Dussehra Recess)	09.09.2022	10.11.2022 (9 Weeks)
3	Dussehra Recess	03.10.2022	08.10.2022 (1 Week)
4	First Mid Term Examinations	11.11.2022	17.11.2022 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	24.11.2022	
6	2nd Spell of Instructions	18.11.2022	12.01.2023 (8 Weeks)
7	Second Mid Term Examinations	16.01.2023	21.01.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	23.01.2023	28.01.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	30.01.2023	
10	End Semester Examinations	30.01.2023	11.02.2023 (2 Weeks)

Note: No. of Working/ instructional days: 92

II SEM

S. No	Description	Duration	
		From	To
1	Commencement of II Semester classwork	**13.02.2023**	
2	1st Spell of Instructions	13.02.2023	08.04.2023 (8 Weeks)
3	First Mid Term Examinations	10.04.2023	15.04.2023 (1 Week)
4	Submission of First Mid Term Exam Marks to the University on or before	22.04.2023	
5	2nd Spell of Instructions (including Summer Vacation)	17.04.2023	24.06.2023 (10 Weeks)
6	**Summer Vacation**	15.05.2023	27.05.2023 (2 Weeks)
7	Second Mid Term Examinations	26.06.2023	01.07.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	03.07.2023	08.07.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	08.07.2023	
10	End Semester Examinations	10.07.2023	22.07.2023 (2 Weeks)

Note: No. of Working/ instructional days: 90

REGISTRAR

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Class Timetable

CLASS: III-B.Tech ECE-B A.Y:2022-23 SEMESTER: II LH: C-202

TIME/ DAY	I 9:40-10:30	II 10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00-1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON	IM	VLSID	DSP	FAI	LUNCH	ESD	A&P	SPORTS
TUE	A&P	ESD	IM	DSP		DSP LAB / e-CAD LAB		
WED	FAI	A&P(T)/DSP(T)	SL LAB			COUN	VLSID	A&P
THU	VLSID	A&P	CO-CU/DAA			DSP	ESD	DSP(T)/VLSID(T)
FRI	ESD	IM	A&P	FAI		e-CAD LAB / DSP LAB		
SAT	DSP	VLSID	VLSID(ADJUNCT)			ESD	VLSID(T)/A&P(T)	LIB

*(T) – Tutorial Concern Faculty

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the Faculty
EC601PC	A&P-Antennas and Propagation	Dr.T.Rama krishna	EC604PC	DSP LAB-Digital Signal Processing Lab	A.Apsara/M.Srilatha/Y.Rajani
EC602PC	DSP-Digital Signal Processing	A.Apsara	EC605PC	e-CAD LAB-e – CAD Lab	K.Srikanth/A.Swetha/T.Naresh
EC603PC	VLSID-VLSI Design	K.Srikanth	EC606PC	SL LAB-Scripting Languages Lab	D.Nagaraju/K.Bhaskar/G.Anitha
EC613PE	ESD-Embedded System Design(Professional Elective-II)	M.Srilatha	-	FAI-Fundamentals of Artificaial Intelligence	T.Divya
VLSID (ADJUNCT)	VLSID(ADJUNCT)	G.Chandra sekhar	COUN	Counseling	K.Srikanth/K.Mallaiah/M.Srilatha
MT600OE	IM-Industrial Management (Open Elective-I)	K.V.Nagamani	SPORTS	Sports	T.Divya/M.Srilatha
			LIB	Library	Y.Raju/P.Rajendra
			CO-CU/DAA	Co-Curricular/Dept. Assoc.Activities	G.Anusha/S.Naresh/G.Swathi

Class Incharge Head of The Department Principal

Head of the Department
Electronics and Communication Engg. Dept
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LESSON PLAN

Programme: B.Tech	Academic Year: 2022-23
Year: III	Semester: II
Course Title: VLSI DESIGN	Course Code: EC603PC
Name of Faculty: K.SRIKANTH	

Unit-I Syllabus

Introduction: Introduction to IC Technology – MOS, PMOS, NMOS, CMOS & BiCMOS.
Basic Electrical Properties: Basic Electrical Properties of MOS and BiCMOS Circuits: Ids-Vds relationships, MOS transistor threshold Voltage, gm, gds, Figure of merit ωo; Pass - Transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design, Bi-CMOS Inverters.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Introduction to VLSI	T1, R1	BB
1	Introduction to IC Technology	T2, R2	BB
1	MOS Transistor, Enhancement and Depletion Mode	T1, R3	BB
1	MOS Fabrication Process	T1, R1	BB
1	Fabrication Process: NMOS, PMOS	T2, R2	BB
1	Fabrication Process: CMOS	T1, R3	BB
1	Fabrication Process: BICMOS	T1, R1	BB
1	Oxidation, Lithography, Diffusion	T1, R3	BB
1	Ion implantation, Metallization, Encapsulation		BB
1	Ids-Vds relationships	T1, R1	BB
1	MOS transistor threshold Voltage, Latch up	T2, R2	BB
1	gm, gds, figure of merit, Pass transistor,	T1, R3	BB
1	NMOS Inverter	T1, W1	BB
1	Various pull ups (2:1)	T2, W1	BB
1	CMOS Inverter analysis and design	T1, R1	BB
1	Bi-CMOS Inverters	T2, R2	BB
Gap beyond syllabus (if any):			
Gap within the syllabus (if any)			
Course Outcome 1: Identify the various Fabrication techniques of IC using various MOS circuits and be able to Solve the electrical properties associated with MOS circuits. (Knowledge – Evaluation)			

*Session Duration: 50 minutes

*Total Number of Hours/Unit: 16

Unit-II Syllabus

VLSI Circuit Design Processes: VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, 2 μm CMOS Design rules for wires, Contacts and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	VLSI Design Flow	T1, R3	BB
1	MOS Layers, Stick Diagrams	T1, R1	BB
2	Stick Diagrams	T1, R1	BB
1	Examples of Layout	T1, R1	BB
2	Design Rules and Layout	T2, R2	BB
1	Examples of Layout	T2, R2	BB
1	2 nm CMOS Design rules for wires	T1, R3	BB
1	Contacts and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates	T2, w1	BB
1	Scaling of MOS circuits	T1, R1	BB
Gap beyond syllabus (if any):			
Gap within the syllabus (if any)			
Course Outcome 1: Infer the steps involved in the VLSI design flow and apply the design rules of IC layout for designing stick, layout diagrams of various gates, adders. (Comprehension – Synthesis)			

*Session Duration: 50 minutes *Total Number of Hours/Unit: 11

Unit-III Syllabus

Gate Level Design: Logic Gates and Other complex gates, Switch logic, Alternate gate circuits, Time delays, Driving large capacitive loads, Wiring capacitance, Fan – in, Fan – out, Choice of layers.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
2	Logic Gates	T2, R2	BB
2	Different complex gates	T2, R2	BB
1	Some Examples	T2, R2	BB
1	Switch logic	T1, R3	BB
1	Alternate gate circuits	T1, R1	BB
1	Time Delays	T2, R2	BB
1	Driving large Capacitive Loads, Wiring Capacitances,	T1, R3	BB
1	Fan-in and fan-out, Choice of layers	T1, R1	BB
Gap beyond syllabus (if any):			
Gap within the syllabus (if any)			
Course Outcome 1: Apply Gate level design principles for the design of various logic gates and complex gates (Application - Synthesis) **COURSE OUTCOME 2:** Contrast on the various techniques like Alternate gate circuits, Time delays, driving large capacitive loads and wiring capacitance (Analysis)			

*Session Duration: 50minutes *Total Number of Hours/Unit:10

Unit-IV Syllabus

Data Path Subsystems: Subsystem Design, Shifters, Adders, ALUs, Multipliers, Parity - generators, Comparators, Zero/One Detectors, Counters.

Array Subsystems: SRAM, DRAM, ROM, Serial Access Memories.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Subsystem Design, Shifters	T2, R2	BB
1	Adders	T1, R3	BB
1	ALUs	T1, R3	BB
2	Multipliers, Parity generators	T1, R3	BB
1	Comparators, Zero/One Detectors, Counters	T1, R3	BB
1	Counters	T1, R3	BB
1	Array Subsystems: SRAM, DRAM	T1, R1	BB
1	ROM, Serial Access Memories	T2, R2	BB
1	Content Addressable Memory	T1, R3	BB
Gap beyond syllabus (if any):			
Gap within the syllabus (if any)			
Course Outcome 1: Construct various data path and array subsystems for complex logic circuits and memory devices (Synthesis)			

*Session Duration: 50minutes *Total Number of Hours/Unit: 10

Unit-V Syllabus

Programmable Logic Devices: PLAs, FPGAs, CPLDs, Standard Cells, Programmable Array Logic, Design Approach, Parameters influencing low power design.

CMOS Testing: CMOS Testing, Need for testing, Test Principles, Design Strategies for test, Chip level Test Techniques.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Design Approach	T2, R2	BB
2	Standard Cells, Programmable Array Logic, PLA	T2, R2	BB
2	FPGAs, CPLDs	T2	BB
1	CMOS TESTING: CMOS Testing	T1	BB
1	Need for testing	T2	BB
1	Test Principles	T1, T2	BB
1	Design Strategies for test	T2	BB
1	Chip level Test Techniques	T1	BB
Gap beyond syllabus (if any):			
Gap within the syllabus (if any)			
Course Outcome 1: Develop semiconductor IC design such as PLA's, PAL, FPGA, CPLDs and also assess the differential strategies for testing of IC's and CMOS. (Synthesis – Evaluation)			

*Session Duration: 50minutes *Total Number of Hours/Unit: 10

Text Books	
Text-1.	Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI,2005 Edition.
Text-2.	Principles of CMOS VLSI Design - Weste and Eshraghian, Pearson Education, 1999.

Suggested / Reference Books	
Ref-1.	Modern VLSI Design - Wayne Wolf, Pearson Education, 3rd Edition, 1997.
Ref-2.	VLSI Technology – S.M. SZE, 2nd Edition, TMH, 2003.
Ref-3.	Digital Integrated Circuits - John M. Rabaey, PHI, EEE, 1997.

WEB REFERENCES

Web Sites	
W1	www.cmosedu.com
W2	https://nptel.ac.in/courses/117106092
W3	https://nptel.ac.in/courses/117101058
W4	https://archive.nptel.ac.in/courses/117/106/117106093/
W5	https://archive.nptel.ac.in/courses/117/106/117106149/
W6	https://archive.nptel.ac.in/courses/117/103/117103125/
W7	https://nptel.ac.in/courses/117106092

Lecture notes

Unit 1 link:

https://drive.google.com/file/d/13P4AhyHcOdgJwPfccmrwKnBTJ8KWaEIs/view?usp=sharing

Unit 2 link:

https://drive.google.com/file/d/1GcXeKIvvO74m5Tpfzr9Z60Oprc5STSsI/view?usp=sharing

Unit 3 link:

https://drive.google.com/file/d/1LXskNSMy-Tj1C1zGbcp2UAqMeVuSLRCg/view?usp=sharing

Unit 4 link:

https://drive.google.com/file/d/1FNhuzxEe_RA2ys3hqjbfNRa1ewWud0PR/view?usp=sharing

Unit 5 link:

https://drive.google.com/file/d/1hjAJEvQpxiy9T8WrAB3Z2-lMG7lKAUbZ/view?usp=sharing

Power point presentation

PPT link 1:

https://docs.google.com/presentation/d/15Hg-be4sfN3A5zJvpsWZ1LXP9ZOiQ2Zh/edit?usp=sharing&ouid=109692577134569542336&rtpof=true&sd=true

PPT link 2:

https://docs.google.com/presentation/d/1HVFnL4qTAaCAWfE8xlywMXV6si2fK0iZ/edit?usp=sharing&ouid=109692577134569542336&rtpof=true&sd=true

Code No: 126EN **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year II Semester Examinations, December - 2017
VLSI DESIGN
(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART – A

(25 Marks)

1.a)	What is pull up and pull down device?	[2]
b)	Why NMOS technology is preferred more than PMOS technology?	[3]
c)	What are the uses of Stick diagram?	[2]
d)	What is the fundamental goal in Device modeling?	[3]
e)	List out the sources of static and dynamic power consumption.	[2]
f)	Define Fan-in and Fan-out.	[3]
g)	Why is barrel shifter very useful in the designing of arithmetic circuits?	[2]
h)	Write the principle of any one fast multiplier.	[3]
i)	What is programmable logic array?	[2]
j)	What are feed-through cells? State their uses.	[3]

PART – B

(50 Marks)

2.a)	What is meant by latch up problem? How will you prevent.	
b)	Define threshold voltage? Drive the Vt equation for MOS transistor.	[5+5]
	OR	
3.a)	Explain with neat diagrams the various NMOS fabrication technology.	
b)	Draw and explain BiCMOS inverter circuit.	[5+5]
4.	Draw the circuit diagram, stick diagram and layout for CMOS inverter.	[10]
	OR	
5.a)	Explain about the various layout design rules.	
b)	Draw the static CMOS logic circuit for the following expression i) $Y=(ABCD)'$ ii) $Y=[D(A+BC)]'$	[5+5]
6.a)	Explain different capacitances present in CMOS design.	
b)	Explain the concept of MOSFET as switches with suitable example.	[5+5]
	OR	
7.	Write short notes on: a) Ratioed Circuits b) Dynamic Circuits.	[5+5]

8.a) Explain the operation of a basic 4 bit adder.
b) Explain the operation of booth multiplication with suitable example. [5+5]

OR

9.a) Design a 1:16 demultiplexer using 1:8 demultiplexers.
b) Draw the structure of a 4×4 static RAM and explain it's operation. [5+5]

10.a) Discuss any two types of programming technology used in FPGA design.
b) Explain ATPG fault models. [5+5]

OR

11.a) What is programmable devices? How it differs from ROM?
b) Explain fault models of VLSI Design. [5+5]

---ooOoo---

Code No: 126VN **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech III Year II Semester Examinations, December - 2018
VLSI DESIGN
(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Write about the Pass transistor. [2]
b) Distinguish between Enhancement and Depletion mode transistor action in N-MOS. [3]
c) Write about contacts and vias in layout design. [2]
d) Write about the 1.2 μm double metal single poly CMOS rules. [3]
e) Mention the different forms of Time delays in gate level circuits. [2]
f) Explain about Switch logic and its usage. [3]
g) Distinguish a synchronous and an asynchronous counters. [2]
h) Write a note on Content Addressable Memory. [3]
i) What is the need for testing of IC? [2]
j) What are the different chip-level Test Techniques? [3]

PART - B

(50 Marks)

2.a) Explain the CMOS fabrication process in p-well using suitable diagrams.
b) Discuss the effect of threshold voltage on MOSFET current Equations. [5+5]

OR

3.a) Discuss the MOS transistor Characteristics in Depletion and enhancement modes.
b) Write about Alternative forms of pull-up and describe about the NMOS pull-ups. [5+5]

4. Write about the stick diagrams and design a stick diagram for two input N-MOS NAND and NOR gates. [10]

OR

5.a) Distinguish between the Lambda-base rules and Double metal MOS process rules.
b) Draw the neat layout diagrams for NMOS shift register cell. [5+5]

6.a) Explain the formal estimation of CMOS inverter delay rise-time estimation and Fall-time estimation.
b) Write a note on the Wiring capacitance in detail. [5+5]

OR

7.a) Write about the different Alternate gate circuits in detail.
b) Discuss about the Choice of layers for the gate level design. [5+5]

8.a) Explain the working principle of Ripple carry adder using Transmission Gates.
b) Explain about the configurations and applications of SRAM and DRAM cells. [5+5]

OR

9.a) Explain the Principle and structure of Serial-Parallel multiplier.
b) Describe the design procedure for design of a asynchronous counter. [5+5]

10.a) Design a PAL to realize a full Adder circuit.
b) Explain the detailed Architecture of CPLD and its Implementations. [5+5]

OR

11. Write a short note on the following:
a) CMOS Testing
b) Strategies for testing. [5+5]

---ooOoo---

Code No: 126VN **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, May - 2019

VLSI DESIGN

(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART – A

(25 Marks)

1.a)	List the basic process for IC fabrication.	[2]
b)	Compare CMOS and BiCMOS logic.	[3]
c)	What are the different MOS layers?	[2]
d)	Give the various color coding used in stick diagram.	[3]
e)	How do understand about MOS transistor as a switch?	[2]
f)	What is meant parasitic capacitance?	[3]
g)	What is meant by bit-sliced datapath organization?	[2]
h)	Determine propagation delay of n-bit carry select adder.	[3]
i)	What is the need of testing?	[2]
j)	What are the types of programmable devices?	[3]

PART – B

(50 Marks)

2.a)	Explain the operation of PMOS Enhancement transistor.	
b)	Explain with neat diagrams the various CMOS fabrication technology.	[5+5]
	OR	
3.	Derive I_d-V_{ds} relationship of MOS in all cases.	[10]
4.	Draw the VLSI design flow diagram and explain.	[10]
	OR	
5.	Draw the circuit diagram stick diagram and layout of 2-input CMOS NAND gate.	[10]
6.a)	Explain the concept of Delay estimation, logical effort and sizing of MOSFET.	
b)	Design a 2-input AND gate using switch logic.	[5+5]
	OR	
7.a)	Describe pass transistor briefly with example.	
b)	Implement EX-OR logic gate using CMOS logic.	[4+6]
8.a)	Explain the operation of 4 bit parallel Adder / subtractor.	
b)	Draw the structure of a dynamic RAM and explain it's operation.	[5+5]
	OR	
9.a)	What are the types of ROMs?Write a block diagram of a ROM and explain it's operation.	
b)	Design a 16:1 multiplexer using 4:1 multiplexers.	[5+5]

10.a) Realize the following function using PAL.
$F1(x, y, z) = \sum (1, 2, 4, 5, 7)$ and
$F2(x, y, z) = \sum (0, 1, 3, 5, 7)$

b) Explain system-level test techniques. [5+5]

OR

11.a) With neat sketch explain the CLB, IOB and programmable interconnects of an FPGA device.

b) Explain self-test technique testing. [5+5]

---ooOoo---

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R. Dist-501 510

I - Mid Examinations, MAY -2023

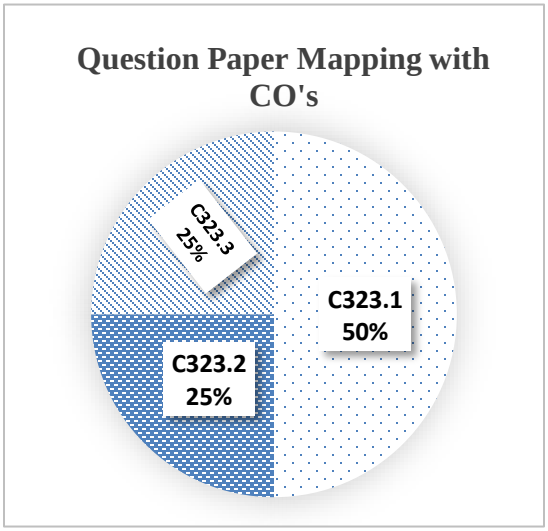
Set – I

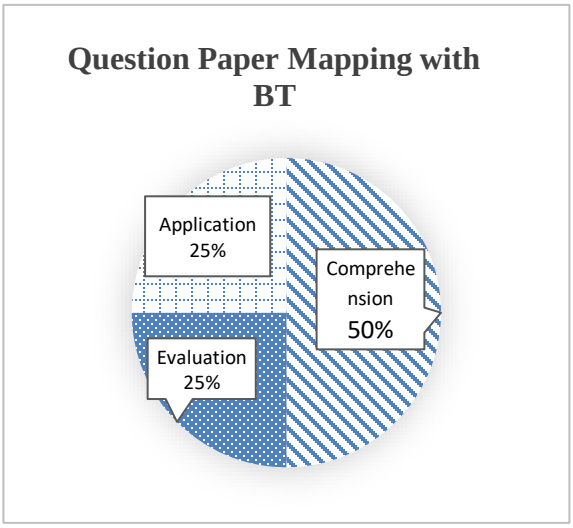
Year &Branch: III ECE A, B&C Date: 10-05-2023 (FN)

Subject: VLSID Max.Marks: 10 Time:60 mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

1	With neat diagrams explain the n-well fabrication process steps	5	(C323.1)	(Comprehension)
2	Derive the I_{ds} vs V_{ds} relation of MOS in non-saturation and saturation region.	5	(C323.1)	(Evaluation)
3	Explain clearly about Dynamic CMOS logic with Example.	5	(C323.3)	(Comprehension)
4	Draw the circuit diagram and corresponding stick diagram of CMOS inverter.	5	(C323.2)	(Application)





Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R. Dist-501 510

II - Mid Examinations,June -2023

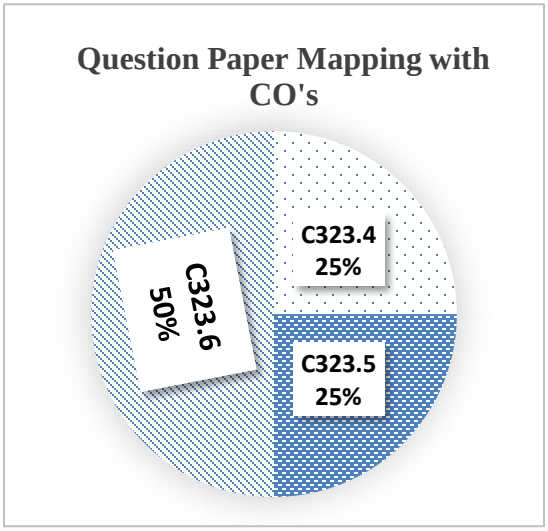
Set – I

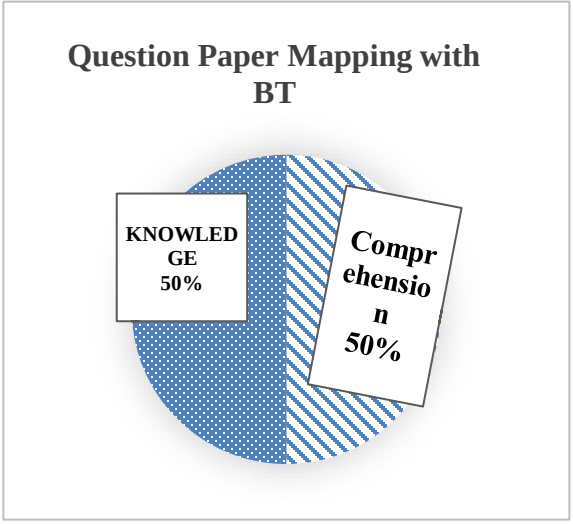
Year &Branch: III ECE A,B&C Date: 28-06-2023(FN)

Subject: VLSID Max.Marks: 10 Time:60 mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

1	Write about the different alternate gate circuits in detail	5	C323.4	KNOWLEDGE
2	Describe the design procedure of Synchronous / Asynchronous Counter	5	C323.5	KNOWLEDGE
3	Explain the architecture of FPGA in detail	5	C323.6	COMPREHENSION
4	Explain the principle of PLA and realize any combinational or sequential logic circuit using PLA.	5	C323.6	COMPREHENSION





SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ECE

B. Tech III Year II Sem I Mid –Term Examination, May-2023

VLSI Design

(Objective Exam)

DATE:10-05-2023 (FN) **TIME: 20 Min** **MAX.MARKS: 10**

NAME: | **ROLL NO:** | **MARKS**

I. Choose The Correct Alternative:

1. VLSI technology uses _____ to form integrated circuit. [ ]

   a) transistors b) switches c) diodes d) buffers

2. nMOS devices are formed in _____ [ ]
   a) p-type substrate of high doping level
   b) n-type substrate of low doping level
   c) p-type substrate of moderate doping level
   d) n-type substrate of high doping level

3. The Zpu/Zpd ratio of an inverter driven directly from the output of another is [ ]

   a) ≥8/1 b) ≤8/1 c) 4/1 d) ≤4/1

4. What is the condition for non saturated region? [ ]

   a) Vds = Vgs – Vt b) Vgs lesser than Vt c) Vds lesser than Vgs – Vt d) Vds greater than Vgs – Vt

5. In NMOS design style implant is in _____ colour [ ]

   a) Brown b) Black c) Blue d) Yellow

6. ___is used to separate N-type and P-type transistors [ ]

   a) Demarcation line b) separation line c) both a & b d) None of above

7. In MOS transistors _____ is used for their gate. [ ]

   a) metal b) silicon-di-oxide c) polysilicon d) gallium

8. Which has high input resistance? [ ]

   a) nMOS b) CMOS c) pMOS d) BiCMOS

9. Ids can be given by _____ [ ]

   a) Qc x Ƭ b) Qc / Ƭ c) Ƭ / Qc d) Qc / 2Ƭ

10. Transit time can be given by _____ [ ]

    a) L / v b) v / L c) v x L d) v x d

II. Fill in The Blanks:

11. Velocity can be given as _____

12. Eds is given by _____

13. For depletion mode transistor, gate should be connected to _____

14. In nMOS inverter configuration depletion mode N type device is used in _____

15. What is the ratio of Zp.u/Zp.d----------

16. Pass transistors are transistors used as _____

17. Which colour is used for n-diffusion ----------

18. Which colour is used for Demarcation line----------

19. Total gate capacitance Cg=_____

20. Figure of merit W_O = ----------

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ECE

B.Tech III Year II Sem II Mid –Term Examination, June-2023

VLSI Design

(Objective Exam)

DATE: /06/2023 **TIME: 20 Min** **MAX.MARKS: 10**

NAME : _____ **ROLL NO:** _____ **MARKS:** _____

I. Choose The Correct Alternative:

1) Which are the following memories require fuses for a standard CMOS process [ ]

a. EPROM b.EEPROM c. PROM d. Flash

2 Decoder in simplest form consist of [ ]

a. NOR Gates b. OR Gates c. AND Gates d. Inverter

3) The heart of ALU is [ ]
a. Silicon b.Adder c. Control bus d. I/O port

4) _____ Is defines as number of inputs to the gate [ ]
a. Fan-In b. Fan-out c. Inverter dalay d.None

5) For a poly silicon layer ,the value of R and C are [ ]
a. Low, Low b. High, moderate c. High, Low d. Low, High

6) 6-Transister SRAM cell uses ____ number of word lines [ ]
a. 1 b.2 c.0 d. 3

7) The logic cells in FPGA Contains [ ]

a. only combinational circuits b.Only sequential circuits
c. Both aand b d. Only Flip-Flop circuits

8) The number of product terms in PAL depends on [ ]
a. Number of AND gates b. Number of OR gates c. Number of addition of both AND& OR
d. Number of independent gates

9) Logic gates are placed in Rows of standard cells of [ ]
a. Equal height b. Equal width c. Varaible height d.constant width

10) VHDL. Verilog description languages are used for testing of [ ]
a. Manufacturing test b. Functionality test c. Design test d.None

II. Fill In The Blanks:

1.There are _____types of super buffer.

2.Total wire capacitance , Cw= _____ .

3.In order to avoid significant delay problems due to asymmetry of conventional

inverters _____ are used .

4. Dynamic RAM's store their content as_____ on a capacitor.

5. The standard cell for a N-Bit parity generator is _____.

6. The level of any particular design can be measured by _____.

7. Large memories are partitioned in to multiple smaller memory arrays known as _____.

8. The general arrangements of PLA is _____ structure.

9. On chip Testing is obtained by _____ .

10. CPLD devices are used for design modification, because these are _____.

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

B-Tech I - Mid Examinations, MAY-2023

Objective Type Exam

Year &Branch: III –ECE-A, B&C **Date: 10-05-2023 (FN)**

Subject: VLSI Design Max. Marks: 10 Time: 20 mins

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1nasxoFU_9ld29aDSeNcomlSqiQ-YrSX0/view?usp=sharing

Objective/Quiz Key Paper

I. Choose the correct alternative:

1) a) transistors
2) c) p-type substrate of moderate doping level
3) c) 4/1
4) c) Vds lesser than Vgs – Vt
5) d) Yellow
6) a) Demarcation line
7) c) polysilicon
8) b) CMOS
9) b) Qc / Ƭ
10) a) L / v

Fill in the blanks:

1) µEds
2) Vds / L
3) Source
4) Pull up
5) 4/1
6) Switches or Logic functions
7) Green
8) brown
9) C_g = CoWL
10) $W_O = g_m/c_g$

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ECE

B.Tech III Year II Sem II Mid –Term Examination, JUNE-2023

VLSI Design

DATE: 28-06-2023(FN) **TIME: 20 Min** **MAX.MARKS: 10**

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1iVp7Mm2yYZscxDeFyIHNHuxbeXaFpmzw/view?usp=sharing

Objective/Quiz Key Paper

I. Choose The Correct Alternative:

1) c. PROM
2 c. AND Gates
3) c. Control bus
4) a. Fan-In
5) b. High, moderate
6) a. 1
7) b.Only sequential circuits
8) a. Number of AND gates
9) a. Equal height
10) a. Manufacturing test

II. Fill In The Blanks:

1. (2)

2. (Carea+Cf)

3.(super buffer)

4. (Charge)

5. (1 Bit cell)

6. (Regularity)

7. (Banks or Sub Arrays)

8. (AND /OR)

9. Self test circuitry)

10. (Reprogrammable)

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

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(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

ASSIGNMENT- 1 **SUBJECT: VLSI DESIGN**

1	With neat diagrams explain the n-well fabrication process steps	(C323.1)	(Comprehension)
2	Derive the I_{ds} vs V_{ds} relation of MOS in non-saturation and saturation region.	(C323.1)	(Evaluation)
3	Explain clearly about Dynamic CMOS logic with Example.	(C323.3)	(Comprehension)
4	Draw the circuit diagram and corresponding stick diagram of CMOS inverter.	(C323.2)	(Application)
5	With neat diagrams explain the NMOS Fabrication process steps.	(C323.1)	(Comprehension)
6	Draw the circuit diagram and corresponding Layout of NMOS inverter.	(C323.2)	(Application)
7	Explain clearly about pseudo NMOS logic with Example.	(C323.3)	(Comprehension)

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VLSI DESIGN ASSIGNMENT –II

1.	Write about the different alternate gate circuits in detail	C323.4	KNOWLEDGE
2.	Describe the design procedure of Synchronous / Asynchronous Counter	C323.5	KNOWLEDGE
3.	Explain the architecture of FPGA in detail	C323.6	COMPREHENSION
4.	Explain the principle of PLA and realize any combinational or sequential logic circuit using PLA.	C323.6	COMPREHENSION
5.	Explain about the configurations and applications of SRAM and DRAM Cells	C323.6	COMPREHENSION

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TUTORIAL TOPICS **SUBJECT: VLSI DESIGN**

S.NO	Unit	TOPIC	Number of Sessions Planned	Teaching method/Aids
1.	1	Discussion on MOSFET Concept?	1	**BB**
2.		Discussion on TWIN TUB Process?	1	BB
3.		Discussion on pull ups (4:1)?	1	BB
4.	2	Bi-CMOS inverter Stick Diagram?	1	BB
5.		Layout Diagram for 3 input NAND gate?	1	BB
6.	3	Gate level design of 3 input CMOS NOR gate?	1	BB
7.		Clocked CMOS logic with example	1	BB
8.	4	Concept on parity generators?	1	BB
9.		Design of DRAM?	1	BB
10.	5	Discussion on CPLD Concept?	1	BB
11.		Chip level techniques?	1	BB

Course Title	VLSI DESIGN
Course Code	EC603PC
Programme	B.Tech
Year & Semester	III year II-semester, B sec
Regulation	R18
Course Faculty	K. SRIKANTH, Assistant Professor, ECE

Slow learners:

Slow Learners (From III-I Result Analysis having >=3 backlogs) : Total 22 slow learners are identified.
Remedial classes are held for improvement of slow learners

S No	Roll no	No of backlogs	Internal-I Status	Internal-II Status
1	20X31A0465	5	14	14
2	20X31A0471	4	23	21
3	20X31A0474	5	21	20
4	20X31A0477	5	21	16
5	20X31A0479	4	20	16
6	20X31A0481	3	21	18
7	20X31A0484	5	17	16
8	20X31A0485	3	14	14
9	20X31A0491	5	18	14
10	20X31A0495	4	18	14
11	20X31A0497	5	16	20
12	20X31A0498	3	21	22
13	20X31A0499	3	18	19
14	20X31A04A5	3	15	16
15	20X31A04A6	5	21	16
16	20X31A04A7	4	19	16
17	20X31A04A8	4	19	17
18	20X31A04B4	4	14	18
19	20X31A04B5	5	15	14
20	20X31A04B6	5	20	18
21	20X31A04C2	5	19	14

22	20X31A04C4	8	15	14

Advanced learners:

S.NO	ROLL.NO.	Assigned work
1	20X31A0463	Advanced Concepts material is provided for advanced learners, Subject seminars are presented by advanced learners in the class., and Advanced learners are encouraged to support slow learners.
2	20X31A0464	
3	20X31A0468	
4	20X31A0469	
5	20X31A0472	
6	20X31A0473	
7	20X31A0475	
8	20X31A0478	
9	20X31A0480	
10	20X31A0482	
11	20X31A0486	
12	20X31A0489	
13	20X31A0492	
14	20X31A0496	
15	20X31A04A0	
16	20X31A04A1	
17	20X31A04A2	
18	20X31A04A3	
19	20X31A04A4	
20	20X31A04A9	
21	20X31A04B1	
22	20X31A04B2	
23	20X31A04B3	
24	20X31A04B8	
25	20X31A04B9	
26	20X31A04C0	
27	20X31A04C3	
28	20X31A04C6	

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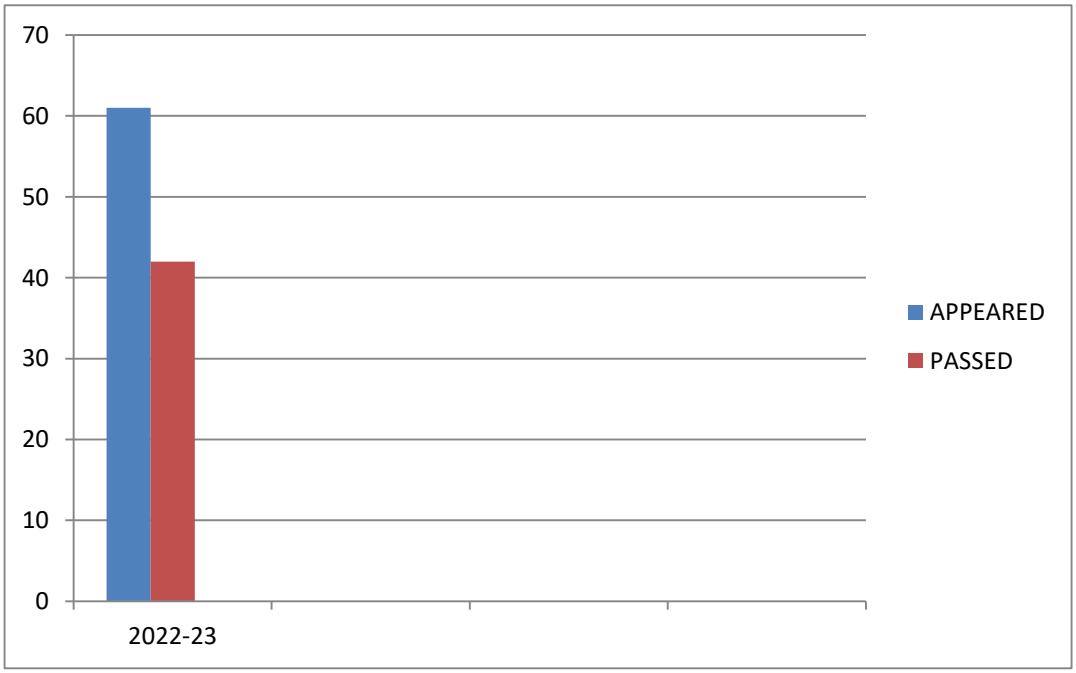
Website: https://siiet.ac.in/

BATCH ECE-III BTECH II SEM ECE-B RESULT ANALYSIS

ACADAMIC YEAR	COURSE NAME	NUMBER OF STUDENTS		QUESTION PAPER SETTING		PASS%
		APPEARED	PASSED	INTERNAL	EXTERNAL	
2022-23	VLSI DESIGN	61	42	COURSE FACULTY	JNTUH	68.85

CONTROL SYSTEM (C323) RESULT ANALYSIS



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

REMEDIAL CLASSES TIME TABLE

A.Y 2022-23 **SEMESTER-II**

BRANCH/ SEC	MON 4.00 PM- 5.00 PM	TUE 4.00 PM- 5.00 PM	WED 4.00 PM- 5.00 PM	THUR 4.00 PM- 5.00 PM	FRI 4.00 PM- 5.00 PM
II ECE-A	EMF&W	LTNM	A&DC	LICA	ECA
II ECE-B	LICA	A&DC	EMF&W	ECA	LTNM
III ECE-A	DSP	VLSID	A&P	ESD	IM
III ECE-B	A&P	ESD	DSP	IM	VLSID
III ECE-C	IM	A&P	ESD	VLSID	DSP
IV ECE-A	WSN	ML	LPVLSID	-	-
IV ECE-B	ML	LPVLSID	WSN	-	-
IV ECE-C	LPVLSID	WSN	ML	-	-

HOD
Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL
PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R R Dist Telangana -501 510

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty : KONGARI SRIKANTH Academic Year: 2022-23

Branch & Section: ECE - B Examination: I Internal

Course Name: VLSI DESIGN Year: III Semester: II

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj1	A1
Max. Marks ==>		5		5		5		5		10	5
1	20X31A0463					5		4		10	5
2	20X31A0464			5				4		10	5
3	20X31A0465			5						4	5
4	20X31A0466			4				3		10	5
5	20X31A0467			4		4				8	5
6	20X31A0468			5				3		9	5
7	20X31A0469			4				4		9	5
8	20X31A0470	4						3		10	5
9	20X31A0471	4						4		10	5
10	20X31A0472			5		5				10	5
11	20X31A0473			5				5		10	5
12	20X31A0474			4				2		10	5
13	20X31A0475	4		5						10	5
14	20X31A0477	4		4						8	5
15	20X31A0478	5						5		10	5
16	20X31A0479			3		4				8	5
17	20X31A0480	5						5		10	5
18	20X31A0481	4		4						8	5
19	20X31A0482					4		4		10	5
20	20X31A0483	4		1						7	5
21	20X31A0484	2								8	5
22	20X31A0485									9	5
23	20X31A0486	4				3				9	5
24	20X31A0489	5						4		10	5
25	20X31A0490			2						9	5
26	20X31A0491	2		2						9	5
27	20X31A0492			5		5				10	5
28	20X31A0493			5		4				9	5
29	20X31A0494	4						4		9	5
30	20X31A0495	4								9	5
31	20X31A0496	5						3		10	5
32	20X31A0497			4						7	5
33	20X31A0498			5		2				9	5
34	20X31A0499							4		9	5
35	20X31A04A0			4				4		10	5
36	20X31A04A1	3		4						9	5
37	20X31A04A2			4		5				9	5
38	20X31A04A3	5						5		10	5
39	20X31A04A4			5				5		10	5
40	20X31A04A5									10	5
41	20X31A04A6	4				4				8	5
42	20X31A04A7			3		3				8	5
43	20X31A04A8	3		2						9	5
44	20X31A04A9			3				3		10	5
45	20X31A04B0	4								5	5
46	20X31A04B1							5		5	5
47	20X31A04B2			5				5		9	5
48	20X31A04B3			4		2				10	5

49	20X31A04B4	5								4	5
50	20X31A04B5									10	5
51	20X31A04B6	5						5		10	5
52	20X31A04B7					2		5		8	5
53	20X31A04B8			5				5		10	5
54	20X31A04B9			3				2		9	5
55	20X31A04C0	5						3		10	5
56	20X31A04C1			4				4		10	5
57	20X31A04C2			4						10	5
58	20X31A04C3	3				2				10	5
59	20X31A04C4			2						8	5
60	20X31A04C5	5								4	5
61	20X31A04C6			5		2				10	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		23	0	30	0	11	0	26	0	56	61
Number of students attempted		25	0	35	0	16	0	28	0	61	61
Percentage of students scored more than target		92%		86%		69%		93%		92%	100%

CO Mapping with Exam Questions:

CO - 1	Y		Y						Y	Y
CO - 2							Y		Y	Y
CO - 3					Y				Y	Y
CO - 4										
CO - 5										
CO - 6										

% Students Scored >Target %	92%		86%		69%		93%		92%	100%

CO Attainment based on Exam Questions:

CO - 1	92%		86%						92%	100%
CO - 2							93%		92%	100%
CO - 3					69%				92%	100%
CO - 4										
CO - 5										
CO - 6										

CO	Subj	obj	Asgn	Overall	Level
CO-1	89%	92%	100%	94%	3.00
CO-2	93%	92%	100%	95%	3.00
CO-3	69%	92%	100%	87%	3.00
CO-4					
CO-5					
CO-6					

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal 1 Examination) = **3.00**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-2)

Name of the faculty : KONGARI SRIKANTH Academic Year: 2022-23

Branch & Section: ECE - B Examination: II Internal

Course Name: VLSI DESIGN Year: III Semester: II

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj2	A2
Max. Marks ==>		5		5		5		5		10	5
1	20X31A0463					5		5		9	5
2	20X31A0464					5		5		9	5
3	20X31A0465	5								4	5
4	20X31A0466	4		3						9	5
5	20X31A0467					3				9	5
6	20X31A0468	5		4						9	5
7	20X31A0469					4		5		9	5
8	20X31A0470					4		3		9	5
9	20X31A0471	4				3				9	5
10	20X31A0472					5		5		9	5
11	20X31A0473			5		5				9	5
12	20X31A0474			3		3				9	5
13	20X31A0475			5		5				9	5
14	20X31A0477			3						8	5
15	20X31A0478					5		5		9	5
16	20X31A0479	2								9	5
17	20X31A0480					5		5		9	5
18	20X31A0481							4		9	5
19	20X31A0482					5		5		8	5
20	20X31A0483					5		3		8	5
21	20X31A0484							2		9	5
22	20X31A0485			5						4	5
23	20X31A0486	4		4						9	5
24	20X31A0489			5		5					5
25	20X31A0490	4		3						9	5
26	20X31A0491					5				6	5
27	20X31A0492					5		5		9	5
28	20X31A0493	3				5				9	5
29	20X31A0494	3		5						7	5
30	20X31A0495					5				4	5
31	20X31A0496					5		4		7	5
32	20X31A0497	3		3						9	5
33	20X31A0498	4				4				9	5
34	20X31A0499	3		3						8	5
35	20X31A04A0	4						4		9	5
36	20X31A04A1	5								4	5
37	20X31A04A2			5				5		9	5
38	20X31A04A3					5		5		8	5
39	20X31A04A4					5		5		9	5
40	20X31A04A5	1								10	5
41	20X31A04A6	1						3		7	5
42	20X31A04A7	3								8	5
43	20X31A04A8	2		2						8	5
44	20X31A04A9					5		4		8	5
45	20X31A04B0	3						2		9	5

46	20X31A04B1	4		4						9	5
47	20X31A04B2					5		5		9	5
48	20X31A04B3			3		3				9	5
49	20X31A04B4			4						9	5
50	20X31A04B5										5
51	20X31A04B6					4				9	5
52	20X31A04B7	3				4				9	5
53	20X31A04B8	5						5		9	5
54	20X31A04B9	4				4				8	5
55	20X31A04C0	4				5				9	5
56	20X31A04C1	3						5		9	5
57	20X31A04C2					5				6	5
58	20X31A04C3					4				7	5
59	20X31A04C4							5		6	5
60	20X31A04C5			4		2				7	5
61	20X31A04C6	2						5		9	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		21	0	18	0	32	0	23	0	55	61
Number of students attempted		26	0	19	0	33	0	25	0	59	61
Percentage of students scored more than target		81%		95%		97%		92%		93%	100%

CO Mapping with Exam Questions:

CO - 1										
CO - 2										
CO - 3									Y	Y
CO - 4	Y								Y	Y
CO - 5			Y						Y	Y
CO - 6					Y		Y		Y	Y

CO Attainment based on Exam Questions:

CO - 1									
CO - 2									
CO - 3								93%	100%
CO - 4	81%							93%	100%
CO - 5			95%					93%	100%
CO - 6					97%		92%	93%	100%

CO	Subj	obj	Asgn	Overall	Level
CO-1					
CO-2					
CO-3		93%	100%	97%	3.00
CO-4	81%	93%	100%	91%	3.00
CO-5	95%	93%	100%	96%	3.00
CO-6	94%	93%	100%	96%	3.00

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal Examination-2) = **3.00**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty : KONGARI SRIKANTH Academic Year: 2022-23

Branch & Section: ECE - B Year / Semester: III / II

Course Name: VLSI DESIGN

S.No	Roll Number	Marks Secured
1	20X31A0463	45
2	20X31A0464	48
3	20X31A0465	0
4	20X31A0466	37
5	20X31A0467	14
6	20X31A0468	42
7	20X31A0469	34
8	20X31A0470	27
9	20X31A0471	27
10	20X31A0472	37
11	20X31A0473	51
12	20X31A0474	11
13	20X31A0475	27
14	20X31A0477	26
15	20X31A0478	34
16	20X31A0479	1
17	20X31A0480	32
18	20X31A0481	7
19	20X31A0482	28
20	20X31A0483	14
21	20X31A0484	0
22	20X31A0485	9
23	20X31A0486	15
24	20X31A0489	30
25	20X31A0490	16
26	20X31A0491	0
27	20X31A0492	33
28	20X31A0493	15
29	20X31A0494	30
30	20X31A0495	26
31	20X31A0496	26
32	20X31A0497	14
33	20X31A0498	26
34	20X31A0499	26
35	20X31A04A0	35
Max Marks		75

S.No	Roll Number	Marks Secured
36	20X31A04A1	30
37	20X31A04A2	40
38	20X31A04A3	46
39	20X31A04A4	58
40	20X31A04A5	27
41	20X31A04A6	0
42	20X31A04A7	7
43	20X31A04A8	8
44	20X31A04A9	40
45	20X31A04B0	30
46	20X31A04B1	29
47	20X31A04B2	37
48	20X31A04B3	26
49	20X31A04B4	26
50	20X31A04B5	0
51	20X31A04B6	27
52	20X31A04B7	32
53	20X31A04B8	50
54	20X31A04B9	26
55	20X31A04C0	48
56	20X31A04C1	36
57	20X31A04C2	0
58	20X31A04C3	26
59	20X31A04C4	0
60	20X31A04C5	30
61	20X31A04C6	39

Class Average mark	26
Number of students performed above the target	42
Number of successful students	61
Percentage of students scored more than target	69%
Attainment level	**3**

Attainment Level	% students
1	40%
2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment

Name of the faculty KONGARI SRIKANTH
Branch & Section: ECE - B
Course Name: VLSI DESIGN

Academic Year: 2022-23
Examination: I Internal
Year: III
Semester: II

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00		3.00	3.00	3.00
CO2	3.00		3.00	3.00	3.00
CO3	3.00	3.00	3.00	3.00	3.00
CO4		3.00	3.00	3.00	3.00
CO5		3.00	3.00	3.00	3.00
CO6		3.00	3.00	3.00	3.00
Internal & University Attainment:			3.00	3.00	
Weightage			25%	75%	
O Attainment for the course (Internal, Universi			0.75	2.25	
CO Attainment for the course (Direct Method)			3.00		

Overall course attainment level **3.00**

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Program Outcome Attainment (from Course)

Name of Faculty:	KONGARI SRIKANTH	Academic Year:	2022-23
Branch & Section:	ECE - B	Year:	III
Course Name:	VLSI DESIGN	Semester:	II

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	-	-	-	-	1	1	1	2	3	-
CO2	3	3	3	3	2	-	-	-	1	1	1	2	3	2
CO3	3	3	3	3	2	-	-	-	1	1	1	2	3	2
CO4	3	2	2	2	-	-	-	-	1	1	1	2	3	1
CO5	3	3	3	3	2	-	-	-	1	1	1	2	3	2
CO6	3	3	3	3	2	-	-	2	1	1	1	2	3	2
Course	**3.00**	**2.83**	**2.83**	**2.83**	**2.00**	**-**	**-**	**2.00**	**1.00**	**1.00**	**1.00**	**2.00**	**3.00**	**1.80**

CO	**Course Outcome Attainment**
CO1	3.00
CO2	3.00
CO3	3.00
CO4	3.00
CO5	3.00
CO6	3.00
Overall course attainment level	**3.00**

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainment	**3.00**	**2.83**	**2.83**	**2.83**	**2.00**			**2.00**	**1.00**	**1.00**	**1.00**	**2.00**	**3.00**	**1.80**

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
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(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

ASSIGNMENTS AND REGISTER

Assignment 1 script link:

https://drive.google.com/file/d/1qCjvB8XaHZAwq-BXCLCuhkACsWqWHanF/view?usp=sharing

Assignment 2 script link:

https://drive.google.com/file/d/1gr6GyuFaflaE6vtrsXH2OJkI_x-3s_UW/view?usp=sharing

Attendance register link:

https://drive.google.com/file/d/1WV0Fl15kTfneFYi7dqCMcZ74eqjlLw3o/view?usp=sharing

COURSE FILE (DIGITAL FORM)

Digital Form Link:

https://drive.google.com/file/d/1lA1iRtvuyhoDxZJjdEA3dYweozpx6Osm/view?usp=sharing