Sri Indu Institute of Engineering & Technology

Recognized Under 2(f) of UGC Act 1956
Approved by AICTE, New Delhi
Affiliated to JNTUH, Hyderabad.

COURSE FILE

ON

ELECTRONIC DEVICES AND CIRCUITS

Course Code – EC301PC

II B.Tech I-SEMESTER

A.Y.: 2022-2023

Prepared by

Mr. K. RAJENDER
Assistant Professor

Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year	2022-2023
Course Title	ELECTRONIC DEVICES AND CIRCUITS
Course Code	EC301PC
Programme	B.Tech
Year & Semester	II year I-semester
Branch & Section	ECE-A
Regulation	R18
Course Faculty	Mr. K. RAJENDER, Assistant Professor

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INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To Continuous assess of teaching-learning process through institute-industry collaboration.

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.

IM4: To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

DM1: To facilitate an academic environment that enables student's centric learning.

DM2: To provide state-of-the-art hardware and software technologies to meet industry requirements.

DM3: To continuously update the Academic and Research infrastructure.

DM4: To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

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PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

PEO1: Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.

PEO2: Graduates with ability to execute innovative ideas for Research and Development with continuous learning.

PEO3: Graduates inculcated with industry based soft-skills to enable employability.

PEO4: Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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PROGRAM OUTCOMES

1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

6. **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY
HYDERABADB.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING COURSE STRUCTURE & SYLLABUS (R18)
Applicable From 2018-19 Admitted Batch

II YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC301PC	Electronic Devices and Circuits	3	1	0	4
2	EC302PC	Network Analysis and Transmission Lines	3	0	0	3
3	EC303PC	Digital System Design	3	1	0	4
4	EC304PC	Signals and Systems	3	1	0	4
5	EC305ES	Probability Theory and Stochastic Processes	3	0	0	3
6	EC306PC	Electronic Devices and Circuits Lab	0	0	2	1
7	EC307PC	Digital System Design Lab	0	0	2	1
8	EC308ES	Basic Simulation Lab	0	0	2	1
9	*MC309	Constitution of India	3	0	0	0
		Total Credits	**18**	**3**	**6**	**21**

II YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	MA401BS	Laplace Transforms, Numerical Methods & Complex Variables	3	1	0	4
2	EC402PC	Electromagnetic Fields and Waves	3	0	0	3
3	EC403PC	Analog and Digital Communications	3	1	0	4
4	EC404PC	Linear IC Applications	3	0	0	3
5	EC405PC	Electronic Circuit Analysis	3	0	0	3
6	EC406PC	Analog and Digital Communications Lab	0	0	3	1.5
7	EC407PC	IC Applications Lab	0	0	3	1.5
8	EC408PC	Electronic Circuit Analysis Lab	0	0	2	1
9	*MC409	Gender Sensitization Lab	0	0	2	0
		Total Credits	**15**	**2**	**10**	**21**

***MC – Satisfactory/Unsatisfactory**

EC301PC: ELECTRONIC DEVICES AND CIRCUITS

B.Tech. II Year I Sem.

L	T	P	C
3	1	0	4

Course Objectives:

- To introduce components such as diodes, BJTs and FETs.
- To know the applications of components.
- To know the switching characteristics of components
- To give understanding of various types of amplifier circuits

Course Outcomes: Upon completion of the Course, the students will be able to:

- Know the characteristics of various components.
- Understand the utilization of components.
- Understand the biasing techniques
- Design and analyze small signal amplifier circuits.

UNIT - I

Diode and Applications: Diode - Static and Dynamic resistances, Equivalent circuit, Load line analysis, Diffusion and Transition Capacitances, Diode Applications: Switch-Switching times.

Rectifier - Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Rectifiers with Capacitive and Inductive Filters, Clippers-Clipping at two independent levels, Clamper-Clamping Circuit Theorem, Clamping Operation, Types of Clampers.

UNIT - II

Bipolar Junction Transistor (BJT): Principle of Operation, Common Emitter, Common Base and Common Collector Configurations, Transistor as a switch, switching times, Transistor Biasing andStabilization - Operating point, DC & AC load lines, Biasing - Fixed Bias, Self Bias, Bias Stability, Bias Compensation using Diodes.

UNIT - III

Junction Field Effect Transistor (FET): Construction, Principle of Operation, Pinch-Off Voltage, Volt-Ampere Characteristic, Comparison of BJT and FET, Biasing of FET, FET as Voltage Variable Resistor. **Special Purpose Devices:** Zener Diode - Characteristics, Voltage Regulator. Principle of Operation -SCR, Tunnel diode, UJT, Varactor Diode.

UNIT – IV

Analysis and Design of Small Signal Low Frequency BJT Amplifiers: Transistor Hybrid model, Determination of h-parameters from transistor characteristics, Typical values of h- parameters in CE, CB and CC configurations, Transistor amplifying action, Analysis of CE, CC, CB Amplifiers and CE Amplifier with emitter resistance, low frequency response of BJT Amplifiers, effect of coupling and bypass capacitors on CE Amplifier.

UNIT – V

FET Amplifiers: Small Signal Model**,** Analysis of JFET Amplifiers, Analysis of CS, CD, CG JFET Amplifiers. MOSFET Characteristics in Enhancement and Depletion mode, Basic Concepts of MOS Amplifiers.

TEXT BOOKS:

1. Electronic Devices and Circuits- Jacob Millman, McGraw Hill Education
2. Electronic Devices and Circuits theory– Robert L. Boylestead, Louis Nashelsky, 11th Edition,2009, Pearson**.**

REFERENCE BOOKS:

1. The Art of Electronics, Horowitz, 3rd Edition Cambridge University Press
2. Electronic Devices and Circuits, David A. Bell – 5th Edition, Oxford.
3. Pulse, Digital and Switching Waveforms –J. Millman, H. Taub and Mothiki S. Prakash Rao, 2Ed.,2008, Mc Graw Hill.

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Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

Course: Electronic Devices and Circuits (C211) **Class: II ECE-A**

Course Outcomes

After completing this course the student will be able to:

C211.1	Ability to analyze the diode under various applications such as rectifier, clippers, clamper Circuits.	Creating, Applying, Analyzing
C211.2	Ability to Classify various configurations and analyze the need for stabilization and biasing techniques of BJT.	Understanding Analyzing, Applying
C211.3	Ability to Discuss operation, biasing and applications of JFET.	Understanding, Applying, Evaluating
C211.4	Ability to Demonstrate special purpose devices like Zener, Tunnel, varactor diode, UJT,SCR.	Understanding, Applying
C211.5	Ability to design and analyze the Small signal low frequency of BJT amplifiers	Understanding ,Creating, Applying
C211.6	Ability to Design and analyze FET amplifiers	Understanding ,Creating, Applying

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO / CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
C211.1	3	2	-	-	3	1	1	1	-	2	2	3	3	3
C211.2	-	1	3	-	-	1	1	1	-	2	2	2	3	3
C211.3	1	3	-	-	2	1	1	1	-	2	2	-	3	3
C211.4	2	-	2	2	-	1	1	1	-	2	2	3	3	3
C211.5	2	3	3	-	3	1	1	1	2	2	2	2	3	3
C211.6	3	3	-	-	3	1	1	1	2	2	2	3	3	3
C211	**2.20**	**2.40**	**2.67**	**2.00**	**2.75**	**1.00**	**1.00**	**1.00**	**2.00**	**2.00**	**2.00**	**2.60**	**3.00**	**3.00**

Course: Electronic Devices and Circuits (C211) **Class: II ECE-A**

P01.ENGINEERING KNOWLEDGE: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

P02.PROBLEM ANALYSIS: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

P03.DESIGN/DEVELOPMENT OF SOLUTIONS: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations

PO 4.CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS: Use research-based Knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

P05.MODERN TOOL USAGE: Create, select, and apply appropriate techniques, resources, andmodern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6:THE ENGINEER AND SOCIETY: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7:ENVIRONMENT AND SUSTAINABILITY: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

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PO12.LIFE-LONG LEARNING: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PSO1: DESIGN SKILLS: Design, analysis and development a economical system in the area of Embedded system & VLSI design

PSO2: SOFTWARE USAGE: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

CO-PO mapping Justification

C211.1 Ability to analyze the diode under various applications such as rectifier, clippers, clamper Circuits. (Creating, Applying, Analyzing)

	Justification
PO1	The ability to analyze diodes in various applications involves applying a solid foundation in mathematics, science, and engineering fundamentals. Engineers use this knowledge to design and troubleshoot circuits, ensuring that diodes function effectively in rectifiers, clippers, and clamper circuits. (level 3)
PO2	Students can analyze the rectifier, clippers, clamper Circuits using loop equations. (level 2)
PO5	Students can design different basic electronic circuits with the knowledge of clippers, clampers, rectifiers. (level 1)
PO6	Engineers must be aware of the broader impact of their work and strive to balance technical excellence with social responsibility. (level 1)
PO7	Students must know that engineers need to consider the efficiency, reliability, and environmental impact of these circuits during the design and analysis phase. (level 1)
PO8	Students can gain knowledge that engineers must prioritize integrity, safety, environmental responsibility, social impact, and transparency in their designs and analyses, ensuring that their work aligns with the highest standards of professional ethics in the field of engineering. (level 1)
PO10	Engineers should engage in discussions, share insights, and contribute to the collective knowledge base, fostering an environment of collaboration and innovation in diode analysis and related fields. (level 2)
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.(level 2)
PO12	Students can continuously learning to explore more knowledge in semiconductor devices. (level 2)
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems. (level 3)
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.(level 3)

C211.2 Ability to classify various configurations and analyze the need for stabilization and biasing techniques of BJT. (Understanding Analyzing, Applying)

	Justification
PO2	Students can learn the operation of transistor in different biasing configurations.(level 1)
PO3	Students can design the different transistor configuration circuits.(level 3)
PO6	Engineers must be aware of the broader impact of their work and strive to balance technical excellence with social responsibility. (level 1)
PO7	Students must know that engineers need to consider the efficiency, reliability, and environmental impact of these circuits during the design and analysis phase. (level 1)
PO8	Students can gain knowledge that engineers must prioritize integrity, safety, environmental responsibility, social impact, and transparency in their designs and analyses, ensuring that their work aligns with the highest standards of professional ethics in the field of engineering. (level 1)
PO10	Effective communication through written materials ensures that the rationale, methodologies, and outcomes of BJT analysis are understood by diverse audiences within the engineering community and beyond. (level 2)
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.(level 2)
PO12	Students can continuously learning to explore more knowledge in semiconductor devices. (level 3)
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems. (level 3)
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.(level 3)

C211.3 Ability to Discuss operation, biasing and applications of JFET. (Understanding, Analyzing, Evaluating)

	Justification
PO1	Students are able to understand the basic knowledge of FET. (level 1).
PO2	Students can analyze the operation of different electronic devices. (level 3)
PO5	Students can apply different biasing techniques in the design of FETs (Field-Effect Transistors) (level 2).
PO6	Student must know an engineer's must be aware of the broader impact of their work and strive to balance technical excellence with social responsibility. (level 1)
PO7	Students must know that engineers need to consider the efficiency, reliability, and environmental impact of these circuits during the design and analysis phase. (level 1)
PO8	Students can gain knowledge that engineers must prioritize integrity, safety, environmental responsibility, social impact, and transparency in their designs and analyses, ensuring that their work aligns with the highest standards of professional ethics in the field of engineering. (level 1)
PO10	Engineers analyzing JFET operation, biasing, and applications need to communicate their findings through clear and comprehensive reports and documentation. (level 2)
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.(level 2)

PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems. (level 3)
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.(level 3)

C211.4 Ability to demonstrate special purpose devices like Zener, Tunnel, varactor diode, UJT, SCR. (Understanding, Applying)

	Justification
PO1	Students get the knowledge on special purpose devices like Zener, Tunnel, varactor diode, UJT, SCR to simplify the complex circuits for analysis. (level 2)
PO3	Students can design the special purpose devices like Zener, Tunnel, varactor diode, UJT, SCR .(level 2)
PO4	Student can solve different complex electronic circuits design with the knowledge of special purpose devices.(level2)
PO6	Engineers must be aware of the broader impact of their work and strive to balance technical excellence with social responsibility. (level 1)
PO7	Students must know that engineers need to consider the efficiency, reliability, and environmental impact of these circuits during the design and analysis phase. (level 1)
PO8	Students can gain knowledge that engineers must prioritize integrity, safety, environmental responsibility, social impact, and transparency in their designs and analyses, ensuring that their work aligns with the highest standards of professional ethics in the field of engineering. (level 1)
PO10	Engineers demonstrating special purpose devices like Zener diodes, Tunnel diodes, varactor diodes, UJTs, and SCRs need to communicate their findings through clear and comprehensive reports and documentation. (level 2)
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.(level 2)
PO12	Students can continuously learning to explore more knowledge in semiconductor devices. (level 3)
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems. (level 3)
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.(level 3)

C211.5 Ability to design and analyze the Small signal low frequency of BJT amplifiers. (Understanding, Creating, Applying)

	Justification
PO1	Students get the knowledge on Transistor Hybrid model to simplify the complex circuits for analysis (level 2)
PO2	Students can analyze the operation of BJT amplifiers using transistor hybrid model. (level 3)
PO5	Students can apply small signal model techniques in the design of FET amplifiers(level 3)
PO6	Engineers must be aware of the broader impact of their work and strive to balance technical excellence with social responsibility. (level 1)
PO7	Students must know that engineers need to consider the efficiency, reliability, and environmental impact of these circuits during the design and analysis phase. (level 1)
PO8	Students can gain knowledge that engineers must prioritize integrity, safety, environmental responsibility, social impact, and transparency in their designs and analyses, ensuring that

	their work aligns with the highest standards of professional ethics in the field of engineering. (level 1)
PO9	Understanding and designing BJT amplifiers involve integrating knowledge from electronics, signal processing, and possibly other fields. Collaborating in a multidisciplinary team allows for a more comprehensive analysis, incorporating varied perspectives and expertise. (level 2)
PO10	Effective communication skills are integral to successful engineering practices, especially when designing and analyzing complex systems like small signal low-frequency BJT amplifiers. (level 2)
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments(level 2)
PO12	Students can continuously learning to explore more knowledge in semiconductor devices. (level 2)
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems. (level 3)
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.(level 3)

C211.6 Ability to Design and analyze FET amplifiers (Understanding ,Creating, Applying)

	Justification
PO1	Student get the knowledge on FET amplifiers to simplify complex circuit analysis .(level 3)
PO2	Students can analyze the operation of FET amplifiers using small signal model. (level 3)
PO3	Students can design the Transistor Hybrid model circuits for different transistor configurations.(level 3)
PO5	Students can apply transistor hybrid model techniques in the design of BJT amplifiers(level 3)
PO6	Engineers must be aware of the broader impact of their work and strive to balance technical excellence with social responsibility. (level 1)
PO7	Students must know that engineers need to consider the efficiency, reliability, and environmental impact of these circuits during the design and analysis phase. (level 1)
PO8	Students can gain knowledge that engineers must prioritize integrity, safety, environmental responsibility, social impact, and transparency in their designs and analyses, ensuring that their work aligns with the highest standards of professional ethics in the field of engineering. (level 1)
PO9	The ability to design small signal low-frequency BJT amplifiers requires individual competence in understanding electronic circuit theory, BJT characteristics, and amplifier design principles. Engineers must independently analyze specifications and constraints to create effective amplifier designs. (level 2)
PO10	Engineers involved in the design and analysis of FET amplifiers need to communicate their findings through clear and comprehensive reports and documentation. (level 2)
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.(level 2)
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems. (level 3)
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.(level 3)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

ACADEMIC CALENDAR 2022-23

B. Tech./B.Pharm. II YEAR I & II SEMESTERS

I SEM

S. No	Description	Duration	
		From	To
1	Commencement of I Semester classwork	**28.11.2022**	
2	1st Spell of Instructions	28.11.2022	21.01.2023 (8 Weeks)
3	First Mid Term Examinations	23.01.2023	30.01.2023 (1 Week)
4	Submission of First Mid Term Exam Marks to the University on or before	04.02.2023	
5	2nd Spell of Instructions	31.01.2023	29.03.2023 (8 Weeks)
6	Second Mid Term Examinations	31.03.2023	08.04.2023 (1 Week)
7	Preparation Holidays and Practical Examinations	10.04.2023	15.04.2023 (1 Week)
8	Submission of Second Mid Term Exam Marks to the University on or before	15.04.2023	
9	End Semester Examinations	17.04.2023	29.04.2023 (2 Weeks)

Note: No. of Working / Instructional Days: 93

II SEM

S. No	Description	Duration	
		From	To
1	Commencement of II Semester classwork	**01.05.2023**	
2	1st Spell of Instructions (including Summer Vacation)	01.05.2023	08.07.2023 (10 Weeks)
3	**Summer Vacation**	15.05.2023	27.05.2023 (2 Weeks)
4	First Mid Term Examinations	10.07.2023	15.07.2023 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	22.07.2023	
6	2nd Spell of Instructions	18.07.2023	11.09.2023 (8 Weeks)
7	Second Mid Term Examinations	12.09.2023	16.09.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	19.09.2023	23.09.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	23.09.2023	
10	End Semester Examinations	25.09.2023	07.10.2023 (2 Weeks)

Note: No. of Working / Instructional Days: 92

24/11/22

REGISTRAR

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC)

Accredited by NAAC A+ Grade, Recognized under 2(f) of UGC Act 1956.

(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana – 501 510

https://siiet.ac.in/

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Class Timetable

CLASS: II-B.Tech ECE-A A.Y:2022-23 SEMESTER: I LH: C-101

TIME/ DAY	I 9:40-10:30	II 10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00-1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON	EDC	COI	EDC LAB / DSD LAB		LUNCH	DSD	NATL	SPORTS
TUE	PTSP	NATL	DSD	COI		EDC	SS	DSD(T)/SS(T)
WED	SS	PTSP	DSD LAB / BS LAB			DSD	SS(T)/EDC(T)	EDC
THU	NATL	PTSP	COI	EDC(T)/DSD(T)		SS	DSD	COUN
FRI	SS	EDC	COI	PTSP		LIB	CO-CU/DAA	
SAT	EDC	DSD	SS	NATL		PTSP	BS LAB / EDC LAB	

*(T) – Tutorial Concern Faculty

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the Faculty
EC301PC	EDC-Electronic Devices and Circuits	K.Rajender	EC306PC	EDC LAB - Electronic Devices and Circuits Lab	K.Rajender/B.Ashwini/M.Srilatha
EC302PC	NATL-Network Analysis and Transmission Lines	M.Nagaraju	EC307PC	DSD LAB - Digital System Design Lab	G.Anusha/T.Divya/P.Krishna Rao
EC303PC	DSD-Digital System Design	G.Anusha	EC308ES	BS LAB - Basic Simulation Lab	P.Rajendra/T.Naresh
EC304PC	SS-Signals and Systems	P.Rajendra	LIB	Library	B.Ashwini/Dr.K.Srinivasa Reddy
EC305ES	PTSP-Probability Theory and Stochastic Processes	T.Naresh	COUN	Counseling	K.Rajender/G.Anusha/G.Anitha
*MC309	COI-Constitution of India	S.Swapna	CO-CU/DAA	Co-Curricular/Dept.Assc.Act.	K.Rajender/T.Naresh/D.Aruna
			SPORTS	Sports	G.Anitha/P.Sumana

Class Incharge Head of The Department PRINCIPAL

Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana -501 510

LESSON PLAN

Programme: B.Tech	Academic Year: 2022-23
Year: II	Semester: I
Course Title: Electronic devices and circuits	Course Code: EC301PC
Name of Faculty: K.Rajender	Number of lectures per week:3

Unit-I Syllabus

Diode and Applications: Diode - Static and Dynamic resistances, Equivalent circuit, Load line analysis, Diffusion and Transition Capacitances, Diode Applications: Switch-Switching times. Rectifier - Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Rectifiers with Capacitive and Inductive Filters, Clippers-Clipping at two independent levels, Clamper-Clamping Circuit Theorem, Clamping Operation, Types of Clampers.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
01	Diode - Static and Dynamic resistances	T1, R 2	BB,
02	Equivalent circuit, Load line analysis	T1, R 2	BB
01	Diffusion and Transition Capacitances	T1, R 2	BB,PPT
01	Diode Applications: Switch-Switching times	T1, R 2	BB
02	Rectifier - Half Wave Rectifier, Full Wave Rectifier	T1, R 2	BB,PPT
01	Bridge Rectifier	T1, R 2	BB
02	Rectifiers with Capacitive and Inductive Filters	T1, R 2	BB
01	Clippers-Clipping at two independent levels	R 3,W1	BB
02	Clamper-Clamping Circuit Theorem, Clamping Operation, Types of Clampers.	R 3,W2	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Describe the applications of diode as rectifier, clippers, clamper Circuits.			

*Session Duration: 50 minutes

*Total Number of Hours/Unit: 13

Course Title: Electronic devices and circuits	Course Code: EC301PC

Unit-II Syllabus

Bipolar Junction Transistor (BJT): Principle of Operation, Common Emitter, Common Base and Common Collector Configurations, Transistor as a switch, switching times, Transistor Biasing and Stabilization - Operating point, DC & AC load lines, Biasing - Fixed Bias, Self Bias, Bias Stability, Bias Compensation using Diodes.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
01	Principle Operation of BJT	T1,R 2	BB
01	Common Emitter Configuration	T2,W3	BB,PPT
02	Common Base and Common Collector Configurations	T1,R 2	BB,PPT
01	Transistor as a switch, switching times	T1,R 1	BB
01	Transistor Biasing and Stabilization - Operating point	T1,R 2	BB,PPT
02	DC & AC load lines	T2,R 2	BB
01	Biasing - Fixed Bias	T1, W4	BB
02	Self Bias, Bias Stability	T1, R 2	BB
02	Bias Compensation using Diodes	T2, R 2	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Design various switching devices such as, transistor , Transistor biasing			

*Session Duration: 50 minutes

*Total Number of Hours/Unit: 13

Course Title: Electronic devices and circuits	Course Code: EC301PC

Unit-III Syllabus

Junction Field Effect Transistor (FET): Construction, Principle of Operation, Pinch-Off Voltage, Volt-Ampere Characteristic, Comparison of BJT and FET, Biasing of FET, FET as Voltage Variable Resistor. **Special Purpose Devices:** Zener Diode - Characteristics, Voltage Regulator. Principle of Operation - SCR, Tunnel diode, UJT, Varactor Diode

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
02	Construction and Principle Operation of FET	T1, R1	BB
02	Pinch-Off Voltage, Volt-Ampere Characteristic	T2, R2	BB
01	Comparison of BJT and FET	T1, R 1	BB
02	Biasing of FET, FET as Voltage Variable Resistor	T1, R 2	BB
01	Zener Diode - Characteristics	T2, R 2	BB, PPT
01	Voltage Regulator	T1, R 1	BB
01	Principle of Operation – SCR	T1, W5	BB,PPT
01	Tunnel diode	T2, W6	BB,PPT
02	UJT, Varactor Diode	T1, R2	BB,PPT
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Analyze the operation FET ,Special Devices like Zener, Tunnel, varactor diode,UJT,SCR.			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 13

Course Title: Electronic devices and circuits	Course Code: EC301PC

Unit-IV Syllabus

Analysis and Design of Small Signal Low Frequency BJT Amplifiers: Transistor Hybrid model, Determination of h-parameters from transistor characteristics, Typical values of h-parameters in CE, CB and CC configurations, Transistor amplifying action, Analysis of CE, CC, CB Amplifiers and CE Amplifier with emitter resistance, low frequency response of BJT Amplifiers, effect of coupling and bypass capacitors on CE Amplifier.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
02	Transistor Hybrid model	T1, R2	BB
02	Determination of h-parameters from transistor characteristics	T2, R1	BB
01	Typical values of h- parameters in CE, CB and CC configurations	T1, R2	BB
01	Transistor amplifying action	T1, R1	BB
01	Analysis of CE Amplifier	T1, R1	BB
01	Analysis of CB Amplifier	T1, R1	BB
01	Analysis of CC Amplifier	T1, R1	BB
02	Analysis of CE Amplifier with emitter resistance	T1,W7	BB
01	low frequency response of BJT Amplifiers	T2,W8	BB,PPT
01	effect of coupling and bypass capacitors on CE Amplifier	T1, R2	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Define explain Transistor Hybrid model			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 13

Course Title: Electronic devices and circuits	Course Code: EC301PC

Unit-V Syllabus

FET Amplifiers: Small Signal Model**,** Analysis of JFET Amplifiers, Analysis of CS, CD, CG JFET Amplifiers. MOSFET Characteristics in Enhancement and Depletion mode, Basic Concepts of MOS Amplifiers.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
02	Small Signal Model	T1, R2	BB
01	Analysis of JFET Amplifiers	T2, R2	BB
02	Analysis of CS JFET Amplifiers	T1, W9	BB
01	Analysis of CD JFET Amplifiers	T1, W10	BB
01	Analysis of CG JFET Amplifiers	T2, R 1	BB
02	MOSFET Characteristics in Enhancement mode	T1, R 2	BB
02	MOSFET Characteristics in Depletion mode	T2, R 1	BB
02	Basic Concepts of MOS Amplifiers	T2, R 2	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Draw the operation of small signal model FET operation.			

*Session Duration: 50minutes
*Total Number of Hours/Unit: 13

Text Books:

1. Electronic Devices and Circuits- Jacob Millman, McGraw Hill Education
2. Electronic Devices and Circuits theory– Robert L. Boylestead, Louis Nashelsky, 11th Edition, 2009, Pearson**.**

Reference Books:

1. The Art of Electronics, Horowitz, 3rd Edition Cambridge University Press
2. Electronic Devices and Circuits, David A. Bell – 5th Edition, Oxford.
3. Pulse, Digital and Switching Waveforms –J. Millman, H. Taub and Mothiki S. Prakash Rao, 2Ed., 2008, Mc Graw Hill.

Web References for Electronic devices and circuits:

S.NO	WEB LINK
1	https://www.electronics-tutorials.ws/diode/diode-clipping-circuits.html
2	https://www.physics-and-radio-electronics.com/electronic-devices-and-circuits/rectifier/clampercircuits.html
3	https://www.electronics-tutorials.ws/amplifier/amp_2.html
4	https://www.electronics-tutorials.ws/amplifier/transistor-biasing.html
5	https://www.daenotes.com/electronics/industrial-electronics/silicon-controlled-rectifiers-scr
6	https://www.physics-and-radio-electronics.com/electronic-devices-and-circuits/semiconductor-diodes/tunneldiode-howitworks.html
7	https://www.slideshare.net/syedafroz1234/common-emitter-with-emi
8	https://unacademy.com/lesson/low-frequency-analysis-of-bjt-amplifier/5TUKWO6Z
9	http://www.mhhe.com/engcs/electrical/neamen01/ch06.pdf
10	https://www.coursehero.com/file/ph9hsb/UNIT-III-FET-Amplifiers-Analysis-of-JFET-Amplifiers-Analysis-of-CS-CD-CG-JFET/

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

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(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

Lecture notes

Unit 1 link:
https://drive.google.com/file/d/1CRNQMLV6wrWe4gKGPB_T9aANVmiEsDjy/view?usp=sharing

Unit 2 link:
https://drive.google.com/file/d/13ju0qaLBFIoUEven9cnH7sl3yONo-U19/view?usp=sharing

Unit 3 link:
https://drive.google.com/file/d/1E6YT7W7GNVI-YmJE9M-aTYW6-NSDdFkE/view?usp=sharing

Unit 4 link:
https://drive.google.com/file/d/13olKNFwTtnpLVs_9fi4JnPADivwGTxl_/view?usp=sharing

Unit 5 link:
https://drive.google.com/file/d/1tR2whxV6YK1SFfV_DLKvIfFvKQXZP7aq/view?usp=sharing

Power point presentation

PPT link:

https://docs.google.com/presentation/d/1vcLrryBksZjVWcD08MtySVjBxz6-Hrgl/edit?usp=sharing&ouid=106700162151853541587&rtpof=true&sd=true

https://docs.google.com/presentation/d/1cL6gOnDCowYbCph1mBac9LBhY-F8ccT4/edit?usp=sharing&ouid=106700162151853541587&rtpof=true&sd=true

https://docs.google.com/presentation/d/1GFPEI6lLkdW0MBaTvfjWoHkbDIzCb_SZ/edit?usp=sharing&ouid=106700162151853541587&rtpof=true&sd=true

Code No: 123AU **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, November/December - 2016
ELECTRONIC DEVICES AND CIRCUITS
(Common to EEE, ECE, CSE, EIE, IT, ETM, MCT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Define static and dynamic resistance of P-N diode. [2]
b) Explain about Zener break down. [3]
c) Define ripple factor. [2]
d) Explain about voltage regulation. [3]
e) What are the applications of UJT? [2]
f) What do you mean by early effect? [3]
g) Explain about collector feedback bias. [2]
h) Write about thermal runaway. [3]
i) Mention small signal parameters of JFET. [2]
j) Differentiate between BJT and JFET. [3]

PART-B

(50 Marks)

2.a) Compare the characteristics of PN junction diode, Zener Diode and Tunnel diode.
b) For a Ge diode, the I_0=2μA and the voltage of 0.26V is applied. Calculate the forward and reverse dynamic resistance values at room temperature. [5+5]

OR

3.a) Derive an expression for transition capacitance of a diode.
b) Explain Avalanche and Zener Breakdowns. [5+5]

4.a) Explain the operation of Full Wave Rectifier with Induction filter with necessary diagrams.
b) A diode whose internal resistance is 20Ω is to supply power to a 100Ω load from 110V (R.M.S) source of supply. Calculate:
i) Peak Load Current
ii) DC Load Current
iii) AC Load Current
iv) % Regulation from No load to given load. [5+5]

OR

5.a) Explain the operation of Full Wave Rectifier with necessary graphs.
b) A 3KΩ resistive load is to be supplied with a D.C. voltage of 300V from A.C. voltage of adequate magnitude and 50Hz frequency by wave rectification. The LC filter is used along the rectifier. Design the bleeder resistance, turns ratio of transformer, VA rating of transformer and PIV rating of diodes. [5+5]

6.a) Derive Emitter Efficiency, Transport factor and large signal current gain and derive the relation between them.

b) Explain how transistor works as an amplifier? [5+5]

OR

7.a) Explain the operation of CC Configuration of BJT and its input and output characteristics briefly.

b) Explain about Punch through and Base width modulation. [5+5]

8.a) What is Biasing? Explain the need of it. List out different types of biasing methods.

b) In a Silicon transistor circuit with a fixed bias,
V_{CC}=9V, R_C=3KΩ, R_B=8KΩ, β=50, V_{BE}=0.7V.
Find the operating point and Stability factor. [5+5]

OR

9.a) Derive the expression for stability factor of self bias circuit.

b) Explain in detail about Thermal Runaway and Thermal Resistance. [5+5]

10.a) Why we call FET as a Voltage Controlled Device.

b) For the Common Source Amplifier, calculate the value of the voltage gain, given
i) r_d=100KΩ, R_L=10KΩ, g_m=300μ and R_O=9.09KΩ.
ii) If C_{DS}=3pF, determine the output impedance at a signal frequency of 1 MHz.
[5+5]

OR

11.a) Define DC Drain resistance, AC Drain Resistance, Amplification Factor and derive them.

b) What are the values of I_D and g_m for V_{GS} = -0.8V if I_{DSS} and V_P are given as 12.4mA and -6V respectively? [5+5]

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R15

Code No: 123AU

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2017
ELECTRONIC DEVICES AND CIRCUITS
(Common to CSE, ECE, EEE, EIE, ETM, IT, MCT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
. Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART-A

(25 Marks)

1.a) Draw Zener Diode Characteristics. [2]
b) Draw the Diode Equivalent Circuit. Mention the applications of PN-junction diode. [3]
c) Explain how P-N junction diode acts as a Rectifier. [2]
d) Explain the necessity of filter circuit after the rectifier circuit. [3]
e) Explain how transistor work as an amplifier. [2]
f) Compare CE,CC and CB configurations. [3]
g) What is the need of biasing? [2]
h) Explain Bias Compensation using Diodes. [3]
i) Compare BJT and FET. [2]
j) How FET acts as Voltage Variable Resistor? [3]

PART-B

(50 Marks)

2.a) Explain the Avalanche and Zener Breakdowns in PN junction diode.
b) What is tunneling phenomena? Explain the principle of operation of tunnel diode with its characteristics. [5+5]

OR

3.a) Derive the expression for transition capacitance of a diode.
b) Define varactor diode? Explain the operation of varactor diode with its equivalent circuit and mention its applications. [5+5]

4. A sinusoidal voltage whose V_m=26V is applied to half-wave rectifier. The diode may be considered to be ideal and R_L=1.2 KΩ is connected as load. Find out peak value of current, RMS value of Current, DC value of current and Ripple factor. [10]

OR

5.a) Derive the expression for Ripple factor for Full Wave Rectifier with L-section filter.
b) Compare FWR and Bridge rectifier. [5+5]

6. The reverse leakage current of the transistor when in CB configuration is 0.3μA while it is 16μA when the same transistor is connected in CE configuration. Determine α, β and γ. [10]

OR

7.a) Explain input and output characteristics of transistor in CB configuration with neat diagram.

b) Discuss the base width modulation. [5+5]

8.a) Derive the operating point using AC and DC load lines.

b) Draw the circuit diagram of a voltage divider bias and derive expression for Stability factor. [4+6]

OR

9. Draw the circuit diagram of CC amplifier using hybrid parameters and derive the expression for A_I, A_V, R_i and R_O. [10]

10. Explain the different biasing techniques of JFET. [10]

OR

11. Describe the construction and working principle of Enhancement mode and depletion mode MOSFET and draw its characteristics. [10]

Code No: 113AU **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2017
ELECTRONIC DEVICES AND CIRCUITS
(Common to EEE, ECE, CSE, EIE, IT, MCT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Explain the Space charge region. [2]
b) Explain the operation of p-n junction biased in the reverse direction. [3]
c) Define Peak Inverse Voltage. [2]
d) Explain the harmonic components in rectifier. [3]
e) Write the complete expression for IC for any VC and IE. [2]
f) Explain the basewidth modulation. [3]
g) Why a capacitive coupling used to connect signal source to an amplifier. [2]
h) Explain the thermal instability. [3]
i) What is Pinchoff Voltage? [2]
j) Define transconductance gm and drain resistance of a FET. [3]

PART-B

(50 Marks)

2.a) Explain about the Current components in a p-n diode.
b) Sketch the piecewise linear characteristics of a diode. What are the approximate cutin voltages for silicon and germanium? [5+5]

OR

3.a) Obtain the static and dynamic resistances of the p-n junction germanium diode, if the temperature is 27^0 C and I_o=1μA for an applied forward bias of 0.2 V.
Assume =1.38×10^{-23} J/^{o}k.
b) Define diffusion and transition capacitance of p-n junction diode. Prove that diffusion capacitance is proportional to current I. [5+5]

4.a) Explain about L section Filters.
b) A full-wave single phase rectifier employs a pi- section filter consisting of two 4 μF capacitances and a 20 H choke. The transformer voltage to the center tap is 300 V rms. The load current is 500 mA. Calculate the dc output voltage and the ripple voltage. The resistance of the choke is 200Ω. [5+5]

OR

5.a) Draw and explain the Thevenin's model for Full-wave rectifier.
b) Explain the Voltage regulation using Zener Diode. [5+5]

6.a) Differentiate between NPN and PNP transistors.

b) Explain the input and output characteristics of the transistor in CC configuration with diagrams. How do you obtain from these? [3+7]

OR

7.a) Draw the circuit diagram of a pnp junction transistor in CE configuration and describe its characteristics.

b) Compare CB and CC configurations. [5+5]

8.a) Explain the DC and AC load Line analysis.

b) Draw and explain the Fixed Bias Circuit. Explain why the circuit is unsatisfactory if the transistor is replaced by another of same type. [5+5]

OR

9.a) Draw and explain the Voltage Divider Biasing.

b) Explain the Thermal runaway. [5+5]

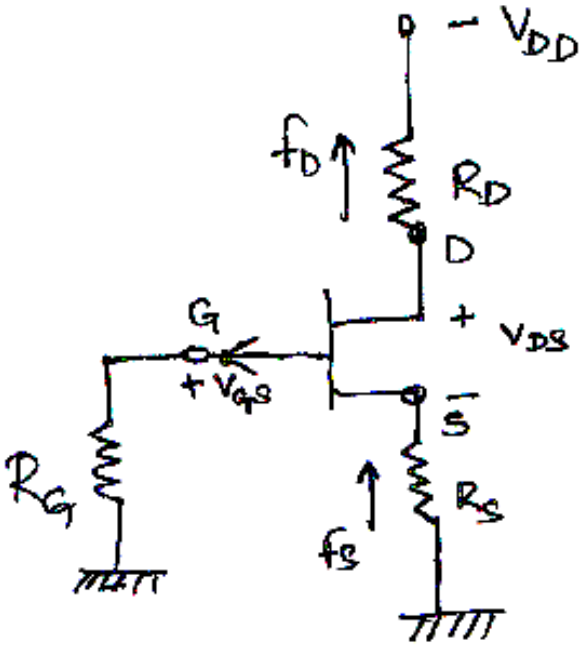
10.a) Explain the JFET Small signal Model.

b) Explain the MOSFET characteristics in enhancement mode. [5+5]

OR

11.a) Explain the FET Common Drain Amplifier.

b) A P-channel FET has V_P = 4V and I_{DSS} = 12mA. For the figure, determine R_D and R_S so that I_D=4 mA and V_{DS}=6V. V_{DD} is 12 V. [5+5]



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Code No: 113AU **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, November/December - 2017
ELECTRONIC DEVICES AND CIRCUITS
(Common to EEE, ECE, CSE, EIE, IT, MCT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) For what voltage will the reverse current in p-n junction Germanium diode reach 90% of its saturation value at room temperature? [2]
b) Write a short note on Varactor diode. [3]
c) Derive the ripple factor for full wave rectifier. [2]
d) Explain voltage regulation using zener diode. [3]
e) Explain how transistor acts as an amplifier. [2]
f) Give the Comparisons between CB, CE, CC configurations. [3]
g) Define thermal runaway. [2]
h) Compare all the three biasing circuits. [3]
i) For a p-channel Silicon FET, with effective width 'a'=2×10^{-4} cm and channel resistivity ρ =10 Ω. Find the pinch off voltage. [2]
j) Draw the circuit diagram of fixed bias arrangement of a JFET. [3]

PART-B

(50 Marks)

2.a) Explain PN diode characteristics in forward bias and reverse bias regions.
b) Find the width of the depletion layer in a germanium junction diode which has the following specifications: Area A = 0.001 cm^2, σ_n = 1 mhos / cm, μ_n = 3800 cm^2/sec, μ_p = 1800 cm^2/sec. [5+5]

OR

3.a) Explain tunnel diode operation with the help of energy band diagrams.
b) Explain the static characteristics of SCR. [5+5]

4.a) A full wave rectifier circuit with C-type capacitor filter is to supply a D.C. Current of 20 mA at 16V. If frequency is 50 Hz ripple allowed is 5%. Calculate:
i) Required secondary voltage of the transformer.
ii) Ratio of I peak/ I_{max} through diodes and the value of C required.
b) With a neat circuit diagram and necessary wave forms explain the operation of half wave rectifier. [5+5]

OR

5.a) An ac supply of 220V is applied to a half wave rectifier circuit through a transformer with a turns ratio of 10:1. Assume the ideal diode. Find:
i) dc output voltage ii) PIV.
b) Compare half wave, full wave and bridge rectifier circuits. [5+5]

6.a) Explain CE configuration with the help of input and output characteristics.

b) A transistor is operated at a forward current of 2μA and with the collector open circuited. Calculate the junction voltages V_C and V_E, the collector to emitter voltage V_{CE} assuming I_{CO} = 2μA, I_{EO} = 1.6μA and α_N = 0.98. [5+5]

OR

7.a) Draw and explain h-parameter model of BJT.

b) Qualitatively explain the static V-I characteristics of UJT. [5+5]

8.a) Explain the need for biasing in electronic circuits. What are the factors affecting the stability factor.

b) A transistor with β = 100 is to be used in Common Emitter Configuration with collector to base bias. The collector circuit resistance is R_C = 1kΩ and V_{CC} = 10V. Assume V_{BE} = 0.

i) Choose R_B so that the quiescent collector to emitter voltage is 4V.

ii) Find the stability factor. [5+5]

OR

9.a) Determine the quiescent currents and the collector to emitter voltage for a Ge transistor with β = 50 in the self biasing arrangements. The circuit component values are V_{CC} = 20V, R_C = 2kΩ, R_e = 0.1 kΩ, R_1 = 100 kΩ and R_2 = 5 kΩ. Find the stability factor S.

b) Explain the terms Bias Stabilization and Bias Compensation. [5+5]

10.a) Derive the expression for the width of depletion region 'W' in the case of p-channel JFET.

b) Explain the working of a depletion type MOSFET with a neat construction diagram and its characteristics. [5+5]

OR

11. Draw the circuit of source follower Amplifier and derive the expressions for A_I, A_V, R_i and R_o. [10]

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SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

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Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana – 501 510
Website : https://siiet.ac.in/

SET-I

I- Mid Examinations, JAN -2023

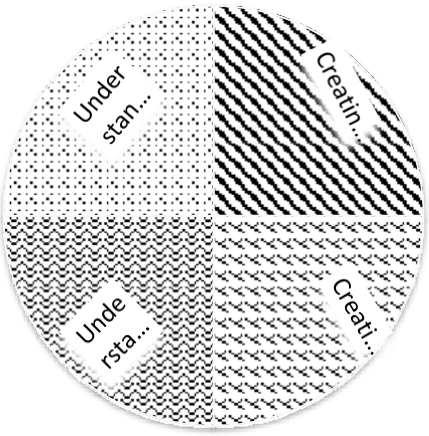
Year &Branch: II ECE A **Date: 24/01/2023**

Subject: EDC **Max. Marks: 10** **Time: 60 mins**

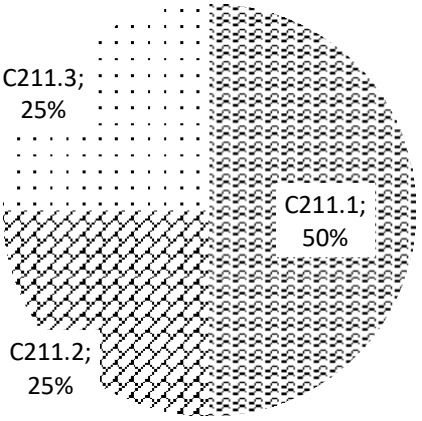
Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10

1. Derive the expression for ripple factor for full wave rectifier with shunt capacitor filter? (C211.1 Creating, Applying)
2. Write the statement of Clamping theorem and prove it? (C211.1 Creating, Analyzing)
3. Explain different methods of Biasing? (C211.2 Understanding)
4. Explain construction and principle operation of N-channel JFET? (C211.3 Understanding, Applying)

Question Paper Mapping with BT



Question Paper Mapping with CO's



Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

B-Tech I - Mid Examinations, JAN-2023

Objective Type Exam

Year & Branch: II –ECE-A Date: 24 /01/2023

Subject: **EDC** Max. Marks: 10 Time: 20 mins

Name: ……Roll No……

I. Choose the correct answers.

1. Which of the following is not a physical component of an electronic circuit [ ]
   a) Capacitor b) Inductor c) Diode d) Temperature

2. Which of the following equation represents mass action law for semiconductors in electronic circuits? [ ]
   a) $n \times p = n_i^2$ b) $n \times p = n_i$ c) $n \times p = n_i^3$ d) $n \times p = n_i^{1/2}$

3. In which of the following region does BJT act as the amplifier electronic device? [ ]
   a) Cut-off b) Saturation c) Active d) Reverse saturation

4. Which of the following is the correct expression of current in an intrinsic semiconductor electronic circuit? [ ]
   a) $I_{Total} = I_e + I_h$ b) $I_{Total} = I_e - I_h$ c) $I_{Total} = I_e + 2I_h$ d) $I_{Total} = 2I_e + I_h$

5. What is the conductivity of an extrinsic type semiconductor electronic device at 0K? [ ]
   a) maximum b) zero c) can't be determined d) minimum

6. Reverse recovery time for a diode is? [ ]
   a) Time taken to eliminate excess minority charge carriers
   b) Sum of storage time (TS) and transition time (TT)
   c) Time taken to eliminate excess majority charge carriers
   d) Time elapsed to return to non conduction state

7. In the volt ampere characteristics of the diode, the slope of the line joining the operating point to the origin at any point is equal to reciprocal of the [ ]
   a) resistance b) conductance c) voltage d) current

8. Which of the following is true? [ ]
   a) Ib = ß Ic b) Ib = ß + 1/ Ic
   c) Ib = Ic/ß d) Ib = Ic/ ß – 1

9. Which of the following is true for the cut-off region in an npn transistor? [ ]
   a) Potential difference between the emitter and the base is smaller than 0.5V
   b) Potential difference between the emitter and the base is smaller than 0.4V
   c) The collector current increases with the increase in the base current
   d) The collector current is always zero and the base current is always non zero

10. What is pinch off voltage? [ ]

a) The minimum voltage required to turn on the FET
b) The maximum voltage a FET can withstand
c) Current amplification factor/voltage gain
d) The value of voltage at which the current gets pinched to zero

II. Fill in the Blanks.

1. Q point can be set to work on active region requires _____ conditions.

2. The maximum efficiency of half wave rectifier is_____

3. The base emitter voltage in a cut off region is _____

4. Ripple factor for full wave rectifier_____

5. _____are used to clip the output waveforms upwards or downwards at a certain level according to the requirements.

6. The Junction Field Effect Transistor is a_____device

7._____circuit is used for adding a DC shift to an AC signal.

8. The rate of change of collector current I_C with respect to the collector leakage current I_{CO} atconstant β and I_B is called _____

9._____is the output obtained from full wave rectifier.

10. N-type semiconductor has_____as majority charge carriers and P-type semiconductor has_____as majority charge carriers

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SET-II

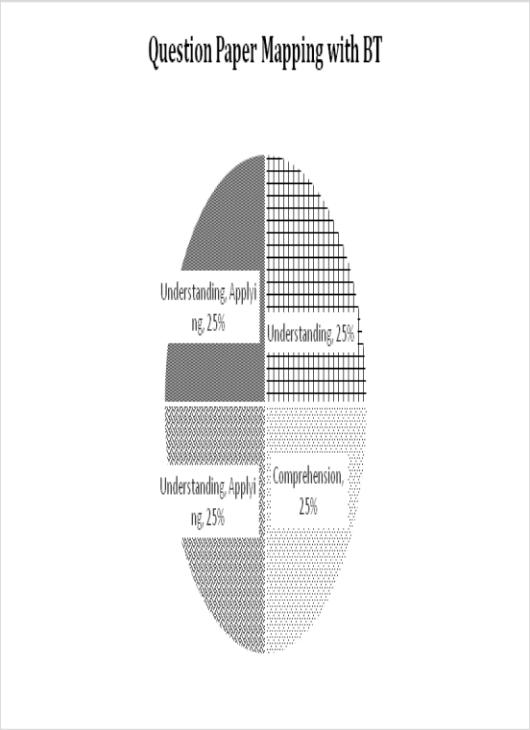
II- Mid Examinations, APRIL -2023

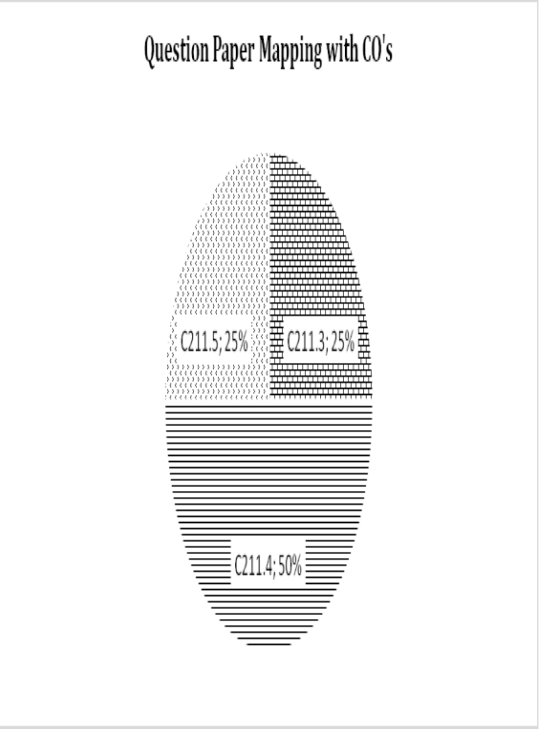
Year &Branch: II ECE A **Date: 01/04/2023**

Subject: EDC **Max. Marks: 10** **Time: 60 mins**

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10

1. What is UJT and draw the Construction, operation of a UJT along with its characteristics (C211.3 Understanding)
2. Draw the circuit diagram of CC amplifier using hybrid parameters and derive the expression for AI , AV, Ri and RO (C211.4 Understanding, Applying)
3. In the CE amplifier calculate the mid frequency voltage gain and lower 3-db point. The transistor has h-parameters h_{fe} =400 and hie=10KΩ, the circuit details are R_S =600Ω, R_L =5KΩ, R_e =1KΩ, V_{cc} =12V, R1=15KΩ, R_2 = 2.2KΩ and C_e= 50μF. (C211.4 Understanding, Applying)
4. What are the values of I_D and g_m for V_{GS} = -0.8 V if I_{DSS} and V_P are given as 12.4 mA and -6V respectively. Sketch the circuit of CS amplifier and derive the expression for voltage gain at low frequencies. (C211.5 Understanding, Applying)





Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

B-Tech II - Mid Examinations, APRIL-2023

Objective Type Exam

Year & Branch: II –ECE-A Date: 01/04/2023

Subject: **EDC** Max. Marks: 10 Time: 20 mins

Name: ……Roll No……

I. Choose the correct answers.

1. Which one of the following statement is correct? A tunnel diode is always biased [ ]
   (a) by a D.C. source (b) in the middle of its negative resistance region
   (c) In the positive resistance region nearest to zero (d) in the reverse direction

2. Zener diodes with breakdown voltages less than 5 V operate predominantly in what type of breakdown? [ ]
   a) Avalanche b) Zener c) Varactor d) Schottky

3. When depletion region becomes widen in Varactor diode, plate separation? [ ]
   a) will increases b) will decrease c) become zero d) become infinite

4. An SCR behaves as a_____switch? [ ]
   a) Unidirectional b) Bidirectional c) Mechanical d) None of the above

5. In a certain common-source D-MOSFET amplifier, Vds =3.2 V r.m.s and V_{gs} = 280 mV r.m.s. The voltage gain is_____ [ ]
   a) 1 b) 11.4 c) 8.75 d) 3.2

6. I_{DSS} can be defined as_____ [ ]
   a) the minimum possible drain current
   b) the maximum possible current with V_{GS} held at –4 V
   c) the maximum possible current with V_{GS} held at 0 V
   d) the maximum drain current with the source shorted

7. For what value of I_D is g_m equal to 0.5 g_{m0}? [ ]
   a) 0 mA b) 0.25 I_{DSS} c) 0.5 I_{DSS} d) I_{DSS}

8. Which of the following is the output terminal of common collector BJT amplifier? [ ]
   a) Emitter b) Base c) Collector d) All the above

9. Inverted signal as outcome obtained in_____amplifiers? [ ]
   a) Common Emitter b) Common Base
   c) Common Collector d) All of the above

10. How the β is the defined for CE amplifiers? [ ]
    a) $\Delta I_C / \Delta I_B$ b) $\Delta I_B / \Delta I_E$ c) $\Delta I_C / \Delta I_E$ d) $\Delta I_E / \Delta I_C$

I. Fill in the Blanks.

1. _____ amplifier has both voltage and current gains.

2. _____terminals of MOSFET do not have direct connection**.**

3. The types of MOSFETs are _____

4. _____is used as a voltage regulator.

5. The capacitance of varactor varies _____

6. A tunnel diode is also called_____

7. The control element of an SCR is _____

8. Between The peak point and the valley point of UJT Emitter characteristics we have _____region.

9. Small signal response is analyzed using the_____model.

10. The quantities are_____called the hybrid parameters

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SET-I

I- Mid Examinations, JAN -2023

Year &Branch: II ECE A **Date: 24/01/2023**
Subject: EDC

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1wHyLwiUR4J0fho_DL8cBTYpMC0pWP0P8/view?usp=sharing

Objective Key Paper

I. Choose the correct alternative:

1) a) Capacitor
2) a) $n \times p = n_i^2$
3) c) Active
4) b) $I_{Total} = I_e - I_h$
5) b) zero
6) a) Time taken to eliminate excess minority charge carriers
7) a) resistance
8) c) Ib = Ic/ß
9) b) Potential difference between the emitter and the base is smaller than 0.4V
10) d) The value of voltage at which the current gets pinched to zero

Fill in the blanks:

1. BE forward biased and BC reverse biased

2.40.6%

3. less than 0.7V

4.0.48

5. Clipper

6. Unipolar

7. Clamper

8. Stability factor

9. Pulsating DC

10. Electrons, holes

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SET-II

II-Mid Examinations, APRIL -2023

Year &Branch: II ECE A **Date: 01/04/2023**
Subject: EDC

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1m5onBHAlYUsPX5NBXJmnsfHo0e5dUtBh/view?usp=sharing

Objective Key Paper

I. Choose the correct alternative:

1) b) in the middle of its negative resistance region
2) b) Zener
3) a) will increases
4) a) Unidirectional
5) b) 11.4
6) c) the maximum possible current with V_{GS} held at 0 V
7) b) 0.25 I_{DSS}
8) a) Emitter
9) a) Common Emitter
10) a) $\Delta I_C / \Delta I_B$

Fill in the blanks:

1. Common Emitter

2. Gate-Channel

3. Depletion and enhancement MOSFETs

4. Zener diode

5. Inversely with reverse voltage

6. Esaki diode

7. Gate

8. Negative resistance

9. h-parameter

10. hie, hre, hfe and hoe

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SUBJECT: ELECTRONIC DEVICES AND CIRCUITS

ASSIGNMENT- 1 :

1.	Derive the expression for transition capacitance of a PN junction diode?	(C211.1)	Creating, Applying
2.	Derive the expression for ripple factor for full wave rectifier with shunt capacitor	(C211.1)	Creating, Applying
3.	Write the statement of Clamping theorem and prove it?	(C211.1)	Creating, Analyzing
4.	Explain the input and out characteristics of CE configuration?	(C211.2)	Understanding, Applying
5.	Explain the construction and principle operation of N-channel JFET?	(C213.3)	Understanding, Applying
6.	Determine the ripple factor of a L-type choke input filter comprising a 10 Hz and 8μF capacitor used with a full wave rectifier. Compare with a simple 8μF capacitor input filter at a load current of 50 mA and 150mA.Assume that DC voltage of 50V.	(C211.1)	Applying
7.	Explain different methods of Biasing?	(C211.2)	Understanding
8.	CE transistor amplifier with voltage divider bias circuit, the quiescent point at V_{CE}=12V, I_C=2mA.If S=<5.1, V_{CC}=24V, V_{BE}=0.7V, β=50 and R_c=4.7KΩ. Determine the values of resistors R_E, R_1 and R_2 .	(C211.2)	(Knowledge, Synthesis)

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SUBJECT: ELECTRONIC DEVICES AND CIRCUITS

ASSIGNMENT- 2:

1.	Explain the working principle of Tunnel diode and explain how it works as an oscillator?	C211.3	Understanding, Evaluating
2.	What is UJT and draw the Construction, operation of a UJT along with its characteristics	C211.3	Understanding
3.	In the CE amplifier calculate the mid frequency voltage gain and lower 3-db point. The transistor has h-parameters h_{fe} =400 and hie=10KΩ, the circuit details are R_s = 600Ω, R_L =5KΩ, R_e =1KΩ, V_{cc} =12V, R1=15KΩ, R_2 = 2.2KΩ and C_e= 50µF	C211.4	Understanding, Applying
4.	Draw the circuit diagram of CB amplifier and explain its operation in detail.	C211.4	Understanding
5.	What are the values of I_D and g_m for V_{GS} = -0.8 V if I_{DSS} and V_P are given as 12.4 mA and -6V respectively. Sketch the circuit of CS amplifier and derive the expression for voltage gain at low frequencies.	C211.5	Understanding, Applying

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SUBJECT: ELECTRONIC DEVICES AND CIRCUITS

TUTORIAL TOPICS

S.NO.	UNIT	TOPIC	NUMBER OF SESSIONS PLANNED	TEACHING METHOD/AIDS
1.	1	A sinusoidal voltage whose Vm=26V is applied to half-wave rectifier. The diode may be considered to be ideal and RL=1.2 KΩ is connected as load. Find out peak value of current, RMS value of Current, DC value of current and Ripple factor	1	BB
2.		A half wave rectifier has a load of 3.5 KΩ. If the diode resistance and the secondary coil resistance together have a resistance of 800Ω and the input voltage has a signal voltage of 240 V, calculate i) Peak, average and rms value of current flowing. ii) dc power output. iii) ac power input iv) Efficiency of the rectifier.	1	BB
3.	2	In a Silicon transistor circuit with a fixed bias, VCC=9V, RC=3KΩ, RB=8KΩ, β = 50, VBE=0.7V. Find the operating point and Stability factor.	1	BB
4.		A transistor with β = 100 is to be used in Common Emitter Configuration with collector to base bias. The collector circuit resistance is RC = 1kΩ and VCC = 10V. Assume VBE = 0.	1	BB

5.	3	Derive the expression for the width of depletion region 'W' in the case of p-channel JFET.	1	BB
6.		A P-channel FET has VP = 4V and IDSS = 12mA. For the figure, determine RD and RS so that ID=4 mA and VDS=6V. VDD is 12 V.	1	BB
7.	4	Draw and explain h-parameter model of BJT.	1	BB
8.		The hybrid parameters for a transistor used in CE configuration are hie = 5kΩ; hfe = 180; hre = 1.25 × 10-4; hoe = 16 × 10-6 ohms. The transistor has a load resistance of 20 KΩ in the collector and is supplied from a signal source of resistance 5 KΩ. Compute the value of input impedance, output impedance, current gain and voltage gain...	1	BB
9.	5	Explain the MOSFET characteristics in enhancement mode	1	BB
10.		Explain the operation of Depletion mode MOSFET in detail.	1	BB
11.		Describe the operation of common drain FET amplifier and derive the equation for voltage gain.	1	BB

Course Title	ELECTRONIC DEVICES AND CIRCUITS
Course Code	EC301PC
Programme	B.Tech
Year & Semester	II year I-semester
Regulation	R18
Course Faculty	K.RAJENDER, Assistant Professor, ECE

Slow learners:

S. No.	Roll no.	No of backlogs	Internal-I Status	Internal-II Status
1	21X31A0402	3	14	14
2	21X31A0403	3	16	18
3	21X31A0408	3	18	18
4	21X31A0409	4	14	14
5	21X31A0412	3	20	14
6	21X31A0414	3	21	17
7	21X31A0417	3	18	15
8	21X31A0422	3	17	19
9	21X31A0433	3	17	18
10	21X31A0435	3	19	18
11	21X31A0436	3	14	19

Advanced learners:

S.No.	Roll no.	Gate Material
1.	21X31A0401	Electronic Devices and Circuits: Energy bands in intrinsic and extrinsic semiconductors, equilibrium carrier concentration, direct and indirect band-gap semiconductors. Carrier transport: diffusion current, drift current, mobility and resistivity, generation, and recombination of carriers, Poisson, and continuity equations. P-N junction, Zener diode, BJT, MOS capacitor, MOSFET, LED, photodiode, and solar cell. **DIODE CIRCUITS** Clipping, clamping, and rectifiers. **BJT AND MOSFET AMPLIFIERS** Biasing, ac coupling, small signal analysis, frequency response. Current mirrors and differential amplifiers.
2.	21X31A0405	
3.	21X31A0410	
4.	21X31A0413	
5.	21X31A0415	
6.	21X31A0418	
7.	21X31A0420	
8.	21X31A0421	
9.	21X31A0423	
10.	21X31A0424	
11.	21X31A0426	
12.	21X31A0427	
13.	21X31A0429	
14.	21X31A0431	
15.	21X31A0432	
16.	21X31A0434	
17.	21X31A0437	

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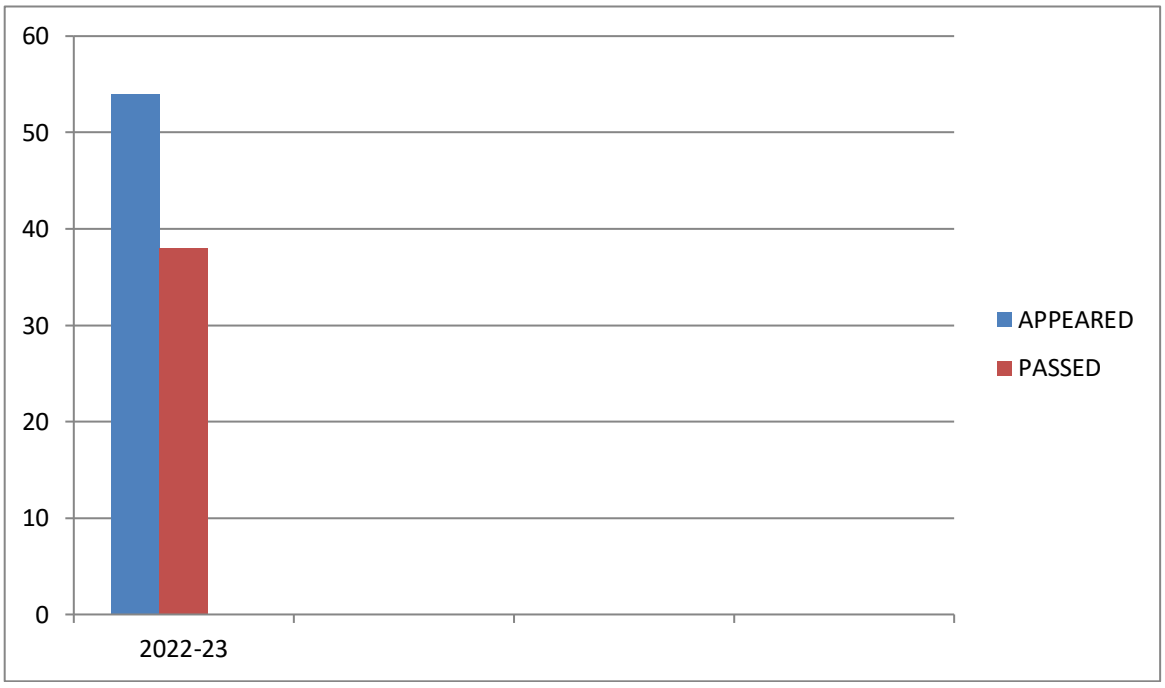
BATCH ECE-II BTECH I SEM ECE-A RESULT ANALYSIS

ACADAMIC YEAR	COURSE NAME	NUMBEROF STUDENTS		QUESTIONPAPER SETTING		PASS%
		APPEARED	PASSED	INTERNAL	EXTERNAL	
2022-23	ELECTRONIC DEVICESAND CIRCUITS	54	39	COURSE FACULTY	JNTUH	72.22

ELECTRONIC DEVICES AND CIRCUITS (C211) RESULTANALYSIS



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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

REMEDIAL CLASSES TIME TABLE

A.Y 2022-23 **SEMESTER-I**

BRANCH/ SEC	MON 4.00 PM-5.00 PM	TUE 4.00 PM-5.00 PM	WED 4.00 PM-5.00 PM	THUR 4.00 PM-5.00 PM	FRI 4.00 PM-5.00 PM
II ECE-A	EDC	NATL	DSD	PTSP	SS
II ECE-B	NATL	DSD	PTSP	SS	EDC
III ECE-A	MPMC	DCCN	CS	BEFA	EMI
III ECE-B	DCCN	CS	BEFA	EMI	MPMC
III ECE-C	CS	BEFA	EMI	MPMC	DCCN
IV ECE-A	MW&OC	DIP	PPLE	NS&C	JAVA
IV ECE-B	DIP	PPLE	NS&C	JAVA	MW&OC
IV ECE-C	PPLE	NS&C	JAVA	MW&OC	DIP

HOD Department
Head of the Department
Electronics and Communication Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH,
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510.

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R.R. Dist. Telangana -501 510.

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty: K. RAJENDER | Academic Year: 2022-23

Branch & Section: ECE - A | Examination: I Internal

Course Name: EDC | Year: II | Semester: I

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj4	A4
Max. Marks ==>		5		5		5		5		10	5
1	21X31A0401			5				2		10	5
2	21X31A0402	2								8	5
3	21X31A0403			2						9	5
4	21X31A0404	3		4						10	5
5	21X31A0405	4		5						10	5
6	21X31A0406			5						10	5
7	21X31A0407			4						10	5
8	21X31A0408			4						9	5
9	21X31A0409					2		3		5	5
10	21X31A0410			5						8	5
11	21X31A0412			5						10	5
12	21X31A0413			5				4		10	5
13	21X31A0414			5		2				9	5
14	21X31A0415			5						9	5
15	21X31A0416			3						10	5
16	21X31A0417			3						10	5
17	21X31A0418			5						10	5
18	21X31A0420			5				4		10	5
19	21X31A0421			1						10	5
20	21X31A0422					3				9	5
21	21X31A0423			5						9	5
22	21X31A0424			5						9	5
23	21X31A0425	3		3						10	5
24	21X31A0426	3		3						8	5
25	21X31A0427	3		5						10	5
26	21X31A0428	3		5						9	5
27	21X31A0429			4				2		8	5
28	21X31A0431			5						10	5
29	21X31A0432			4		2				7	5
30	21X31A0433			5						7	5
31	21X31A0434			5				2		9	5
32	21X31A0435			5						9	5
33	21X31A0436	4								5	5
34	21X31A0437					2		3		5	5
35	22X35A0401			5				5		10	5
36	22X35A0402			5				5		10	5
37	22X35A0403			5				4		10	5
38	22X35A0404			5						10	5
39	22X35A0405			5				4		10	5
40	22X35A0406			4				5		10	5
41	22X35A0407			5				5		10	5
42	22X35A0408			4				4		9	5
43	22X35A0409			5				5		9	5
44	22X35A0410			5				5		10	5

45	22X35A0411			5				5		10	5
46	22X35A0412			5				5		10	5
47	22X35A0413			5				5		9	5
48	22X35A0414			5				5		10	5
49	22X35A0415			4				5		10	5
50	22X35A0416			5				5		10	5
51	22X35A0417			5				5		10	5
52	22X35A0418			5				5		10	5
53	22X35A0419			5				4		10	5
54	22X35A0420			5				4		10	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		7	0	47	0	1	0	23	0	51	54
Number of students attempted		8	0	49	0	5	0	26	0	54	54
Percentage of students scored more than target		88%		96%		20%		88%		94%	100%

CO Mapping with Exam Questions:

CO - 1	Y		Y						Y	Y
CO - 2					Y				Y	Y
CO - 3							Y		Y	Y
CO - 4										
CO - 5										
CO - 6										

% Students Scored >Target %	88%		96%		20%		88%		94%	100%

CO Attainment based on Exam Questions:

CO - 1	88%		96%						94%	100%
CO - 2					20%				94%	100%
CO - 3							88%		94%	100%
CO - 4										
CO - 5										
CO - 6										

CO	Subj	obj	Asgn	Overall	Level
CO-1	92%	94%	100%	95%	3.00
CO-2	20%	94%	100%	71%	3.00
CO-3	88%	94%	100%	94%	3.00
CO-4					
CO-5					
CO-6					

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal Examination-1) **3.00**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-2)

Name of the faculty : K.RAJENDER | Academic Year: 2022-23

Branch & Section: ECE - A | Examination: II Internal

Course Name: EDC | Year: II | Semester: I

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj1	A1
Max. Marks ==>		5		5		5		5		10	5
1	21X31A0401	5		4						6	5
2	21X31A0402										5
3	21X31A0403	3		4						6	5
4	21X31A0404	3				4				6	5
5	21X31A0405							4		5	5
6	21X31A0406	5		4						7	5
7	21X31A0407			3		2				4	5
8	21X31A0408			4				4		5	5
9	21X31A0409	3		2						5	5
10	21X31A0410			1		4				4	5
11	21X31A0412					3		2		4	5
12	21X31A0413					4		5		9	5
13	21X31A0414	2		3						7	5
14	21X31A0415					3				7	5
15	21X31A0416	4								5	5
16	21X31A0417					3				7	5
17	21X31A0418			4						5	5
18	21X31A0420	2		5						6	5
19	21X31A0421			5						6	5
20	21X31A0422			4		3				7	5
21	21X31A0423	5				3				7	5
22	21X31A0424	4		3						7	5
23	21X31A0425	5		4						8	5
24	21X31A0426	5		4						7	5
25	21X31A0427	5		4						7	5
26	21X31A0428	5		4						7	5
27	21X31A0429	3		5						7	5
28	21X31A0431	5		4						8	5
29	21X31A0432							4		5	5
30	21X31A0433			3		3				7	5
31	21X31A0434					4		5		8	5
32	21X31A0435	4				3				6	5
33	21X31A0436	4		3						7	5
34	21X31A0437	5		3						6	5
35	22X35A0401	4		4						7	5
36	22X35A0402	5		4						7	5
37	22X35A0403			4		5				8	5
38	22X35A0404					5		5		7	5
39	22X35A0405			5		5				8	5
40	22X35A0406	5		4						7	5

41	22X35A0407	5		4						7	5
42	22X35A0408			3						8	5
43	22X35A0409	4								5	5
44	22X35A0410					5		5		8	5
45	22X35A0411	5						5		9	5
46	22X35A0412	5				5				9	5
47	22X35A0413			5				5		9	5
48	22X35A0414	5		5						8	5
49	22X35A0415					5		5		7	5
50	22X35A0416	5						5		9	5
51	22X35A0417	5				5				8	5
52	22X35A0418			5		5				8	5
53	22X35A0419	5						5		9	5
54	22X35A0420	5				5				9	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		29	0	30	0	20	0	12	0	43	54
Number of students attempted		31	0	32	0	21	0	13	0	53	54
Percentage of students scored more than target		94%		94%		95%		92%		81%	100%

CO Mapping with Exam Questions:

CO - 1										
CO - 2										
CO - 3										
CO - 4	Y								Y	Y
CO - 5			Y		Y				Y	Y
CO - 6							Y		Y	Y

% Students Scored >Target %	94%		94%		95%		92%		81%	100%

CO Attainment based on Exam Questions:

CO - 1										
CO - 2										
CO - 3										
CO - 4	94%								81%	100%
CO - 5			94%		95%				81%	100%
CO - 6							92%		81%	100%

CO	**Subj**	obj	Assign	Overall	Level
CO-1					
CO-2					
CO-3					
CO-4	94%	81%	100%	92%	3.00
CO-5	94%	81%	100%	92%	3.00
CO-6	92%	81%	100%	91%	3.00

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal Examination-2) **3.00**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty : K.RAJENDER Academic Year: 2022-23

Branch & Section: ECE - A Year / Semester: II / I

Course Name: EDC

S.No	Roll Number	Marks Secured
1	21X31A0401	29
3	21X31A0402	7
4	21X31A0403	26
5	21X31A0404	0
6	21X31A0405	29
7	21X31A0406	29
8	21X31A0407	6
9	21X31A0408	0
10	21X31A0409	4
11	21X31A0410	30
12	21X31A0412	6
13	21X31A0413	31
14	21X31A0414	5
15	21X31A0415	35
16	21X31A0416	26
17	21X31A0417	6
18	21X31A0418	32
19	21X31A0420	29
20	21X31A0421	32
21	21X31A0422	6
22	21X31A0423	30
23	21X31A0424	5
24	21X31A0425	14
25	21X31A0426	35
26	21X31A0427	38
27	21X31A0428	6
28	21X31A0429	33
30	21X31A0431	26
31	21X31A0432	26
32	21X31A0433	11
33	21X31A0434	35
34	21X31A0435	10
35	21X31A0436	26
Max Marks		75

S.No	Roll Number	Marks Secured
36	21X31A0437	27
38	22X35A0401	40
39	22X35A0402	29
40	22X35A0403	30
41	22X35A0404	29
42	22X35A0405	26
43	22X35A0406	30
44	22X35A0407	38
45	22X35A0408	15
46	22X35A0409	29
47	22X35A0410	42
48	22X35A0411	42
49	22X35A0412	33
50	22X35A0413	35
51	22X35A0414	32
52	22X35A0415	29
53	22X35A0416	44
54	22X35A0417	38
55	22X35A0418	30
56	22X35A0419	35
57	22X35A0420	32

Class Average mark	25
Number of students performed above the target	39
Number of successful students	54
Percentage of students scored more than target	72%
Attainment level	**3**

Attainment Level	% students
1	40%
2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment

Name of the faculty K.RAJENDER
Branch & Section: ECE - A
Course Name: EDC

Academic Yea 2022-23
Examination:
Year: II
Semester: I

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00		3.00	3.00	3.00
CO2	3.00		3.00	3.00	3.00
CO3	3.00		3.00	3.00	3.00
CO4		3.00	3.00	3.00	3.00
CO5		3.00	3.00	3.00	3.00
CO6		3.00	3.00	3.00	3.00
Internal & University Attainment:			3.00	3.00	
Weightage			25%	75%	
CO Attainment for the course (Internal, University			0.75	2.25	
CO Attainment for the course (Direct Method)			3.00		

Overall course attainment level **3.00**

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Program Outcome Attainment (from Course)

Name of Faculty:	K.RAJENDER	Academic Year:	2022-23
Branch & Section:	ECE - A	Year:	II
Course Name:	EDC	Semester:	I

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	3	1	1	1	-	2	2	3	3	3
CO2	-	1	3	-	-	1	1	1	-	2	2	2	3	3
CO3	1	3	-	-	2	1	1	1	-	2	2	-	3	3
CO4	2	-	2	2	-	1	1	1	-	2	2	3	3	3
CO5	2	3	3	-	3	1	1	1	2	2	2	2	3	3
CO6	3	3	-	-	3	1	1	1	2	2	2	3	3	3
Course	**2.20**	**2.40**	**2.67**	**2.00**	**2.75**	**1.00**	**1.00**	**1.00**	**2.00**	**2.00**	**2.00**	**2.60**	**3.00**	**3.00**

CO	**Course Outcome Attainment**
CO1	3.00
CO2	3.00
CO3	3.00
CO4	3.00
CO5	3.00
CO6	3.00
Overall course attainment level	**3.00**

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainment	**2.20**	**2.40**	**2.67**	**2.00**	**2.75**	**1.00**	**1.00**	**1.00**	**2.00**	**2.00**	**2.00**	**2.60**	**3.00**	**3.00**

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)

ASSIGNMENTS AND REGISTERS

Assignment 1 script link:

https://drive.google.com/file/d/1PW_Te18gztfY6nMcMewWU9JtUNhxOIim/view?usp=sharing

Assignment 2 script link:

https://drive.google.com/file/d/1jg0r8Cn7NBPTnu34kFMCuXbD8N5g4bKj/view?usp=sharing

Attendance register link:

https://drive.google.com/file/d/11t0VDLurO0TlhMp4PlXsXx67ffzkyWAp/view?usp=sharing