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COURSE FILE

ON

ELECTRONIC DEVICES AND CIRCUITS LAB

Course Code - EC306PC

II B.Tech I-SEMESTER A.Y.: 2022-2023

Prepared by

Mr. K. RAJENDER Assistant Professor

Head of the Department Electronics and Communication Engg. Dept SRI INDV INSTITUTE OF ENGG & TECH Sneriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL Sri Indu Institute of Engineering & Tech Sheriguda(Vill), Ibrahimpatnam

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year	2022-2023
Course Title	ELECTRONIC DEVICES AND CIRCUITS LAB
Course Code	EC306PC
Programme	B.Tech
Year & Semester	II year I-semester
Room Number	A-113
Name of the lab	Mrs.A.Sindhuja
incharge	
Name of the faculty	Mr. K.Rajender
incharge	

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INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

- IM1: To offer outcome-based education and enhancement of technical and practical skills.
- **IM2:** To Continuous assess of teaching-learning process through institute-industry collaboration.
- **IM3:** To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.
- **IM4:** To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

Head of the Department Electronics and Communication Engg. Dept SRI INDV INSTITUTE OF ENGG & TECH Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

- **DM1:** To facilitate an academic environment that enables student's centric learning.
- **DM2:** To provide state-of-the-art hardware and software technologies to meet industry requirements.
- DM3: To continuously update the Academic and Research infrastructure.
- **DM4:** To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

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PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

- **PEO1:** Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.
- **PEO2:** Graduates with ability to execute innovative ideas for Research and Development with continuous learning.
- PEO3: Graduates inculcated with industry based soft-skills to enable employability.
- **PEO4:** Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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PROGRAM OUTCOMES

1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

6. **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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JAWAHARLAL NEHRUTECHNOLOGICAL UNIVERSITY HYDERABAD B.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING COURSE STRUCTURE & SYLLABUS (R18)

ApplicableFrom2018-19AdmittedBatch

IIYEARI SEMESTER

S.No.	Course Code	Course Title		т	P	Credits
1	EC301PC	Electronic Devices and Circuits	3	1	0	4
2	EC302PC	Network Analysis and Transmission Lines	3	0	0	3
3	EC303PC	Digital System Design	3	1	0	4
4	EC304PC	Signals and Systems	3	1	0	4
5	EC305ES	Probability Theory and Stochastic Processes	3	0	0	3
6	EC306PC	Electronic Devices and Circuits Lab	0	0	2	1
1	EC307PC	Digital System Design Lab	U	U	2	1
8	EC308ES	Basic Simulation Lab	0	0	2	1
9	*MC309	Constitution of India		0	0	0
		Total Credits	18	3	6	21

IIYEARII SEMESTER

S.No.	Course Course Title		L	T	Р	Credits
1	MA401BS	1BS Laplace Transforms Numerical Methods& Complex Variables		1	0	4
2	EC402PC	Electromagnetic Fields and Waves	3	0	0	3
3	EC403PC	Analog and Digital Communications	3	1	0	4
4	EC404PC	Linear IC Applications	3	0	0	3
5	EC405PC	Electronic Circuit Analysis	3	0	0	3
6	EC406PC	Analog and Digital Communications Lab	0	0	3	1.5
7	EC407PC	IC Applications Lab	0	0	3	1.5
8	EC408PC	Electronic Circuit Analysis Lab	0	0	2	1
9	*MC409	Gender Sensitization Lab	0	0	2	0
		Total Credits	15	2	10	21

*MC-Satisfactory/Unsatisfactory

EC306PC: ELECTRONIC DEVICES AND CIRCUITS LAB

B.Tech. II Year I Sem.

L T P C 0 0 2 1

List of Experiments(Twelve experiments to be done):

Verify any twelve experiments in H/W Laboratory

- 1. PN Junction diode characteristics A) Forward bias B) Reverse bias.
- 2. Zener diode characteristics and Zener as voltage Regulator
- 3. Full Wave Rectifier with & without filters
- 4. Input and output characteristics of BJT in CE Configuration
- 5. Input and output characteristics of FET in CS Configuration
- 6. Common Emitter Amplifier Characteristics
- 7. Common Base Amplifier Characteristics
- 8. Common Source amplifier Characteristics
- 9. Measurement of h-parameters of transistor in CB ,CE, CC configurations
- 10. Switching characteristics of a transistor
- 11. SCR Characteristics.
- 12. Types of Clippers at different reference voltages
- 13. Types of Clampers at different reference voltages
- 14. The steady state output wave form of clampers for a square wave input

Major Equipment required for Laboratories:

- 1. RegulatedPowerSuppliers,0-30V
- 2. 20MHz, Dual Channel Cathode Ray Oscilloscopes.
- 3. Functions Generators- Sine and Square wave signals
- 4. Multimeters
- 5. Electronic Components



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Course: Electronic Devices And Circuits Lab (C216)

Class: II ECE-A

Course Outcomes

After completing this course the student will be able to:

C216.1	Construct and analyze the characteristics of PN junction	Creating, Applying,
	diode, Zener diode and Silicon Controlled Rectifier.	Analyzing
C216.2	Implement the rectifier circuits with and without filter and	Applying
	voltage regulator.	
C216.3	Implement the various types of clippers and clampers at	Applying
	different reference voltages.	
C216.4	Design and observe the switching characteristics of	Creating ,Understanding
	transistor.	and Applying
C216.5	Observe the characteristics of CE and CS configuration	Understanding,
	and calculate the h- parameters of transistors in CE, CB	Application
	and CC configuration.	
C216.6	Design and analyze the characteristics of CE, CB and CS	Understanding, Creating,
	amplifiers.	Applying

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO / CO	PO	PO	PO	PO	PO	PO	PO	PO	PO	PO	PO	PO	PSO	PSO
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
C216.1	3	2	-	-	1	1	1	1	2	2	2	3	3	3
C216.2	-	1	3	-	-	1	1	1	2	2	2	2	3	3
C216.3	1	3	-	-	1	1	1	1	2	2	2	-	3	3
C216.4	1	-	2	2	-	1	1	1	2	2	2	3	3	3
C216.5	1	-	3	-	1	1	1	1	2	2	2	2	3	3
C216.6	3	3	-	-	-	1	1	1	2	2	2	3	3	3
C216	1.8	2.3	2.7	2	1.0	1.0	1.0	1.0	2.0	2.0	2.0	2.6	3.00	3.00



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LIST OF EXPERIMENTS AND THEIR CO, PO/PSO MAPPING

S.No	Name of The Experiment	СО	PO/PSO
1	PN Junction diode characteristics A) Forward bias B) Reverse bias.	1	1,2,5,6,7,8,9,10,11,12/1,2
2	Zener diode V-I characteristics and Zener diode as voltage regulator.	1	1,2,5,6,7,8,9,10,11,12/1,2
3	Full wave rectifier with and without filters.	2	2,3,6,7,8,9,10,11,12/1,2
4	Input and output Characteristics of a BJT in CE configuration and calculation of h parameters.	5	1,3,5,6,7,8,9,10,11,12/1,2
5	Input and output characteristics of FET in CS Configuration	5	1,3,5,6,7,8,9,10,11,12/1,2
6	Common Emitter Amplifier Characteristics	6	1,2,6,7,8,9,10,11,12/1,2
7	Common Base Amplifier Characteristics	6	1,2,6,7,8,9,10,11,12/1,2
8	Common Source amplifier Characteristics	6	1,2,6,7,8,9,10,11,12/1,2
9	Switching characteristics of a transistor	4	1,3,4,6,7,8,9,10,11,12/1,2/1
10	Types of Clippers at different reference voltages	3	1,2,5,6,7,8,9,10,11/1,2
11	Types of Clampers at different reference voltages	3	1,2,5,6,7,8,9,10,11/1,2
12	The steady state output waveform of clampers for a square wave input	3	1,2,5,6,7,8,9,10,11/1,2



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING Class Timetable

CLASS: II-B.Tech ECE-A A.Y:2022-23 SEMESTER: I LH: C-101 TIME/ I II III IV V VI VII DAY 1:00-1:30 9:40-10:30 10:30 -11:20 11:20-12:10 12:10-1:00 1:30-2:20 2:20-3:10 3:10-4:00 MON EDC COI EDC LAB / DSD LAB DSD NATL SPORTS TUE PTSP NATL DSD COI EDC SS DSD(T)/SS(T) L WED SS PTSP U DSD LAB / BS LAB DSD SS(T)/EDC(T) EDC N THU NATL PTSP EDC(T)/DSD(T) COI С SS DSD COUN H FRI SS EDC COI PTSP LIB CO-CU/DAA SAT EDC DSD SS NATL PTSP BS LAB / EDC LAB

*(T) - Tutorial Concern Faculty

Course Code	Course Name	Name of the Faculty	Code	Course	Name of the
EC301PC	EDC-Electronic Devices and Circuits	K.Rajender	EC306PC	EDC LAB - Electronic Devices and Circuits Lab	K.Rajender/B.Ashwini/M.Srilatha
EC302PC	NATL-Network Analysis and Transmission Lines	M.Nagaraju	EC307PC	DSD LAB - Digital System Design Lab	G.Anusha/T.Divya/P.Krishna Rao
EC303PC	DSD-Digital System Design	G.Anusha	EC308ES	BS LAB - Basic Simulation Lab	P.Rajendra/T.Naresh
EC304PC	SS-Signals and Systems	P.Rajendra	LIB	Library	B.Ashwini/Dr K Sriniyasa Reddy
EC305ES	PTSP-Probability Theory and Stochastic Processes	T.Naresh	COUN	Counseling	K.Rajender/G.Anusha/G.Anitha
*MC309	COL-Constitution of India	C Current	CO-CU/DAA	Co-Curricular/Dept.Assc.Act.	K.Rajender/T.Naresh/D.Aruna
	the state of the s	5.Swapna	SPORTS	Sports	G.Anitha/P.Sumana
	Class Incharge		Headlocat	Bepartment .	PRINCIPAL Sri Indu Institute British Perlong & Tech Sheriguda (Vill), Ibrahimpatnam P. R. Dist Telangana -501 510

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Lab External Question Paper

Subject Name: Electronic Devices and Circuits Lab

Year & Semester: II-I A.Y:

A.Y:2022-2023

- 1. a) Plot Volt-Ampere Characteristics of P-N Diode A) Forward bias B) Reverse bias..
 - b) Find cut-in voltage for P-N Junction diode?
- 2. a) Plot Volt-Ampere Characteristics of Zener Diode.
 - b) Find Zener Breakdown Voltage in Reverse Biased conditions.
- 3. Find below parameters for Full- Wave Rectifier with and without filter.
 - a) Percentage Regulation
 - b) Ripple Factor
 - c) Efficiency
- 4. Draw input and output characteristics of a transistor in Common Source Configuration.
- 5. Draw input and output characteristics of a transistor in C.E Configuration.
- Plot frequency response of FET common source amplifier and find its cut off frequencies and Band width.
- 7. Plot frequency response of Common Emitter Amplifier and calculate its Bandwidth.
- 8. Plot frequency response of C.B Amplifier and calculate its Bandwidth.
- 9. Switching characteristics of a transistor.
- 10. Draw the input and output waveforms of Clippers at different reference voltages.
- 11. Draw the input and output wave forms of Clampers at different reference voltages for sine wave input.
- 12. Draw the input and output wave forms of clampers at different reference voltages for a square wave input.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

B.Tech II ECE Regular Lab External Exams Timetable

A.Y: 2022-23

SEM: I

S. N o.	Name of the Lab & Lab Number	Year/ Branch Section	Date & Time of the Lab Exam	Lab Internal Examiners Details
1	Electronic Devices	nic Devices II ECE-A (10:00 AM - 01:00 P)		Mr.K.Rajender
	(A-113)	II ECE-B	12.04.2023 (10:00 AM - 01:00 PM)	ه Mrs.G.Nirmala
2	Digital System	II ECE-A	12.04.2023 (10:00 AM - 01:00 PM)	Mrs.G.Anusha
	(A-313)	II ECE-B	13.04.2023 (10:00 AM - 01:00 PM)	ھ Mrs.P.Srilatha
3	Basic Simulation Lab	II ECE-A	13.04.2023 (10:00 AM - 01:00 PM)	Mr.T.Naresh &
3	(C-002)	II ECE-B	11.04.2023 (10:00 AM - 01:00 PM)	Mrs.S.Alekhya

HOD/ECE Head of the Department Electronics and Communication Engg. Dept SRI INDU INSTITUTE OF ENGG & TECH Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

B. Tech II ECE Regular Lab External Examiners from TKREC

A.Y: 2022-23

SEM: I

S. N o.	Name of the Lab & Lab No.	Year/ Branch Section	Date & Time of the Lab Exam	Lab Internal Examiners Details	Lab External Examiners Details
and the second	Electronic Devices	II ECE-A	11.04.2023 (10:00 AM - 01:00 PM)	Mr K Dajander	B.Sunitha
1	and Circuits Lab(A-113)	II ECE-B	12.04.2023 (10:00 AM - 01:00 PM)	8897756066	Dr.G.Sirisha
	Digital System	II ECE-A	12.04.2023 (10:00 AM – 01:00 PM)	Mrs.G.Anusha	V.Nageshwar Reddy
2	Design Lab (A-313)	II ECE-B	13.04.2023 (10:00 AM - 01:00 PM)	8639937510	V Lavanya
	Basic	II ECE-A	13.04.2023 (10:00 AM – 01:00 PM)	Mr.T.Naresh	V Amulya
3	Simulation Lab(C-002)	II ECE-B	11.04.2023 (10:00 AM - 01:00 PM)	8919911324	Y Prathyusha
		II CSE-A	15.04.2023 (10:00 AM - 01:00 PM)		B Rekha
	Analog and II	II CSE-B	11.04.2023 (10:00 AM - 01:00 PM)	Mrs.K.Padma 9030468759	B Nireesha
4	Digital Electronics	II CSE-C	12.04.2023 (01:00 PM - 04:00 PM)		V.Nageshwar Reddy
	(A-114)	II CSE (CS)	11.04.2023 (01:00 PM - 04:00 PM)	Mrs.P.Kavitha	B Sunitha
		II CSE (IOT)	12.04.2023 (10:00 AM - 01:00 PM)	8125250145	N Aravind

HOD/ECE

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LAB OCCUPANCY CHART

ELECTRONIC DEVICES AND CIRCUITS LAB

A.Y: 2022-23

SEM-I

	I 9:40-10:30	II 10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00-1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON			EDC Lab	II ECE-A				
TUE					U		EDC Lat	II ECE-B
WED	MAINT	ENANCE			C N			
THU					Н			
FRI			EDC Lab	II ECE-B				17
SAT		EECE I ECE					EDC Lat	I ECE-A

ARGE

HOD PRINCIPAL Head of the Department PRINCIPAL Electronics and Communication Engg. Defi Indu Institute of Engineering & Tr SRI INDU INSTITUTE OF ENGG & TECH heriguda(V), Ibrahimpatnam(I. Sheriguda(V), Ibrahimpatnam(M), R.R.Disi-501 510



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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Do's and Don'ts

- All students must observe the dress code while in the laboratory
- Foods, drinks and smoking are **NOT** allowed
- All bags must be left at the indicated place.
- The lab time table must be strictly followed.
- Be **PUNCTUAL** for your laboratory session.
- Experiment must be completed within the given time.
- Noise must be kept to minimum.
- Workspace must be kept clean and tidy at all time.
- Handle all apparatus with care.
- All students are liable for any damage to equipment due to their own negligence.
- All equipment, apparatus, tools and components must be **RETURNED** to their original place after use.
- Students are strictly **PROHIBITED** from taking out any items from the laboratory.
- Report immediately to the lab supervisor if any injury occurred.
- Report immediately to the lab supervisor if any damages to equipment.

BEFORE LIVING LAB

- Place the stools under the lab bench.
- Turn off the power to all instruments.
- Please check the laboratory notice board regularly for updates.



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ELECTRONIC DEVICES AND CIRCUITS LAB

PHSICAL LAB FLOOR PLAN

ROOM NO: 113

BLOCK: A

FLOOR: I



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Lab manual link:

https://drive.google.com/file/d/1yN_BALFIIsFhkUBpfIE8xRFbiQ7PTWdg/view?usp=sharing

Department of Electronics and Communication Engineering Course Outcome Attainment (Internal Examination-1)

Name of	f the faculty :	K.RAJENDER		Academic Year:	2022-23
Branch	& Section:	FCF - A	-	Examination:	I Internal
Brunen & Section.		ELECTRONIC	DEVICES	Examination.	1 miternar
Course Name:		&CIRCUITS LA	AB	Year/Semester:	II/I
S.No	HT No.	A+A+CD+MG	T+P+C+R	DDE]
Max. M	arks ==>	5	5	15	
1	21X31A0401	5	4	14	1
2	21X31A0402	5	5	13	1
3	21X31A0403	5	4	11	1
4	21X31A0404	5	5	13	1
5	21X31A0405	5	4	13	1
6	21X31A0406	5	4	14	1
7	21X31A0407	5	4	15	1
8	21X31A0408	4	4	12	
9	21X31A0409	4	3	10	1
10	21X31A0410	5	4	14	
11	21X31A0412	5	4	13	1
12	21X31A0413	5	5	14	
13	21X31A0414	5	4	11	1
14	21X31A0415	5	5	13	1
15	21X31A0416	4	3	10	
16	21X31A0417	5	4	12	1
17	21X31A0418	5	4	13	
18	21X31A0420	5	5	14	1
19	21X31A0421	5	5	13	1
20	21X31A0422	5	5	13	
21	21X31A0423	5	4	14	1
22	21X31A0424	4	4	14	1
23	21X31A0425	5	3	12	
24	21X31A0426	5	4	14	1
25	21X31A0427	5	5	14	
26	21X31A0428	4	4	14	1
27	21X31A0429	5	4	14	1
28	21X31A0431	5	4	14	1
29	21X31A0432	5	4	14	T
30	21X31A0433	5	4	14	T
31	21X31A0434	5	5	14	T
32	21X31A0435	5	4	14	Ţ
33	21X31A0436	4	3	7	T
34	21X31A0437	4	3	7	T
35	22X35A0401	5	4	14	1
36	22X35A0402	5	5	13]
37	22X35A0403	5	5	13]
38	22X35A0404	5	5	14]
39	22X35A0405	5	4	15]
40	22X35A0406	5	5	14]
41	22X35A0407	5	5	15]
42	22X35A0408	5	5	14	Ţ

43	22X35A0409	5	5	13
44	22X35A0410	5	5	14
45	22X35A0411	5	4	15
46	22X35A0412	5	4	15
47	22X35A0413	5	5	14
48	22X35A0414	5	5	13
49	22X35A0415	5	4	14
50	22X35A0416	5	5	14
51	22X35A0417	5	5	14
52	22X35A0418	5	5	14
53	22X35A0419	5	4	13
54	22X35A0420	5	5	14
Target so HoD	et by the faculty /	3.00	3.00	9.00
Number	of students			
performe	ed above the target	54	54	52
Number	of students	+ +		
attempte	d	54	54	54
Percenta	ae of students			
scored r	nore than target	100%	100%	96%
	noic than target	uestions:		
	CO - 1	V	V	V
	CO - 1	I V	I V	I V
	CO = 2	ř V	Y V	Y V
	CO - 4	Y	Y	Y
	CO - 5	Y	Y	Y
	CO - 6	Y	Y	Y
Va Stud	ents Noored N Lorget			
70 Studi	%	100%	100%	96%
CO Atte	ainment based on Fy	ram Questions.	10070	9070
<u>co mu</u>		100%	1009/	069/
	CO - 1	100%	100%	9076
	0-2	100%	100%	96%
	CO - 3	100%	100%	96%
	CO - 4	100%	100%	96%
	CO - 5	100%	100%	96%
	CO - 6	100%	100%	96%
	СО	Intrnal practic	DDE	Overall
	CO-1	100%	96%	98%
	CO-2	100%	96%	98%
	CO-3	100%	96%	98%
		10070	70/0	000/
	CU-4	100%	96%	98%
	CO-5	100%	96%	98%
	CO-6	100%	96%	98%

Attainm	Attainment Level					
1	40%					
2	50%					
3	60%					

Attainment (Internal 1 Examination) =

3.00 3.00

Level 3.00 3.00 3.00 3.00 3.00

NOTE:

A+A+CD+MG : AIM+APPARATUS+CIRCUIT DIAGRAM+MODEL GRAPH

T+P+C+R : THEORY+PROCEDURE+CALCULATION+RESULT

DDE : Day to Day Evaluation

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-2)										
Name o	f the faculty :	K.RAJENDER		Academic Year:	2022-23					
Branch	& Section:	ECE - A		Examination:	II Internal					
C	NT	ELECTRONIC I	DEVICES	V	TT /T					
Course	Name:	&CIRCUITS LA	В	Year/Semester:	11/1					
S.No	HT No.	A+A+CD+MG	T+P+C+R	DDE						
Max. M	arks ==>	5	5	15						
1	21X31A0401	5	4	14						
2	21X31A0402	5	5	13						
3	21X31A0403	5	4	11						
4	21X31A0404	5	5	13						
5	21X31A0405	5	4	13						
6	21X31A0406	5	4	14						
7	21X31A0407	5	4	15						
8	21X31A0408	4	4	12						
9	21X31A0409	4	3	10						
10	21X31A0410	5	4	14						
11	21X31A0412	5	4	13						
12	21X31A0413	5	5	14						
13	21X31A0414	5	4	11						
14	21X31A0415	5	5	13						
15	21X31A0416	4	3	10						
16	21X31A0417	5	4	12						
17	21X31A0418	5	4	13						
18	21X31A0420	5	5	14						
19	21X31A0421	5	5	13						
20	21X31A0422	5	5	13						
21	21X31A0423	5	4	14						
22	21X31A0424	4	4	14						
23	21X31A0425	5	3	12						
24	21X31A0426	5	4	14						
25	21X31A0427	5	5	14						
26	21X31A0428	4	4	14						
27	21X31A0429	5	4	14						
28	21X31A0431	5	4	14						
29	21X31A0432	5	4	14						
30	21X31A0433	5	4	14						
31	21X31A0434	5	5	14						
32	21X31A0435	5	4	14						
33	21X31A0436	4	3	7						
34	21X31A0437	4	3	7						
35	22X35A0401	5	4	14						
36	22X35A0402	5	5	13	1					
37	22X35A0403	5	5	13						
38	22X35A0404	5	5	14	1					
39	22X35A0405	5	4	15						
40	22X35A0406	5	5	14	1					
41	22X35A0407	5	5	15						
42	22X35A0408	5	5	14						

43	22X35A0409	5	5	13	
44	22X35A0410	5	5	14	
45	22X35A0411	5	4	15	
46	22X35A0412	5	4	15	
47	22X35A0413	5	5	14	
48	22X35A0414	5	5	13	
49	22X35A0415	5	4	14	
50	22X35A0416	5	5	14	
51	22X35A0417	5	5	14	
52	22X35A0418	5	5	14	
53	22X35A0419	5	4	13	
54	22X35A0420	5	5	14	
Target s	et by the faculty /	3.00	3.00	9.00	
HOD	af ata dan ta				
Number	of students	54	54	52	
Number	of students				
attempte	of students	54	54	54	
attempte					_
Percenta	ige of students	100%	100%	96%	
scored 1	nore than target				
<u>CO Ma</u>	pping with Exam Q	<u>uestions:</u>			
	CO - 1	Y	Y	Y	
	CO - 2	Y	Y	Y	
	CO - 3	Y	Y	Y	
	CO - 4	Y	Y	Y	
	CO - 5	Y	Y	Y	
	CO - 6	Y	Y	Y	
% Stude	ents Scored >Target				
	%	100%	100%	96%	
CO Atta	ainment based on E	xam Questions:		•	
	CO - 1	100%	100%	96%	
	CO - 2	100%	100%	96%	
	CO - 3	100%	100%	96%	
	CO - 4	100%	100%	96%	
	CO - 5	100%	100%	96%	
	CO - 6	100%	100%	96%	
		100/0	10070	7070	
	со	Intrnal practics	DDE	Overall	Level
	CO-1	100%	96%	98%	3
	CO-2	100%	96%	98%	3
	CO 2	100%	060/	080%	
	CU-3	100%	90%	9070	3
	CO-4	100%	96%	98%	3

Attainment Level									
1	40%								
2	50%								
3	60%								
	Attainmen 1 2 3								

3.00 3.00 3.00

3.00

3.00

3.00

3.00

98%

98%

CO-6 Attainment (Internal 2 Examination) = NOTE:

100%

100%

A+A+CD+MG : AIM+APPARATUS+CIRCUIT DIAGRAM+MODEL GRAPH

96%

96%

T+P+C+R : THEORY+PROCEDURE+CALCULATION+RESULT

DDE : Day to Day Evaluation

CO-5



Branch & Section:

Course Name: S.No Roll Number

Department of Electronics and Communication Engineering **Course Outcome Attainment (University Examinations)**

Academic Year:

Year / Semester:

1	21X31A0401	69		
2	21X31A0402	67		
3	21X31A0403	55		
4	21X31A0404	63		
5	21X31A0405	67		
6	21X31A0406	68		
7	21X31A0407			
8	21X31A0408			
9	21X31A0409	66		
10	21X31A0410	67		
11	21X31A0412	66		
12	21X31A0413	71		
13	21X31A0414	65		
14	21X31A0415	68		
15	21X31A0416	69		
16	21X31A0417	62		
17	21X31A0418	70		
18	21X31A0420	72		
19	21X31A0421	68		
20	21X31A0422	63		
21	21X31A0423	69		
22	21X31A0424	55		
23	21X31A0425	64		
24	21X31A0426	62		
25	21X31A0427	72		
26	21X31A0428	70		
27	21X31A0429	67		
28	21X31A0431	68		
29	21X31A0432	68		
30	21X31A0433	67		
31	21X31A0434	70		
32	21X31A0435	68		
33	21X31A0436	60		
34	21X31A0437	55		
Max M				
Class A	67			
Number	34			
Number	of successful st	udents	54	
Percent	age of students s	scored more than target	63%	
Attai	nment leve		3	

ECE - A

ELECTRONIC DEVICE	S &CIRCU	JITS LA	В	
Marks Secured		S.No	Roll Number	Marks Secured
69		35	22X35A0401	69
67		36	22X35A0402	75
55		37	22X35A0403	58
63		38	22X35A0404	69
67		39	22X35A0405	72
68		40	22X35A0406	71
66		41	22X35A0407	68
65		42	22X35A0408	70
66		43	22X35A0409	69
67		44	22X35A0410	72
66		45	22X35A0411	69
71		46	22X35A0412	70
65		47	22X35A0413	72
68		48	22X35A0414	71
69		49	22X35A0415	71
62		50	22X35A0416	71
70		51	22X35A0417	72
72		52	22X35A0418	72
68		53	22X35A0419	69
63		54	22X35A0420	68
69				
55				
64				
62				
72				
70				
67				
68				
68				
67				
70				
68				
60				
55				

2022-23

II-I

Attainment Level	% students
1	40%
2	50%
3	60%

A REAL PROPERTY AND A REAL

Department of Electronics and Communication Engineering

Course Outcome Attainment

Name of the faculty	K.RAJENDER	Academic Year:	2022-23
Branch & Section:	ECE - A	Year:	II
Course Name:	ELECTRONIC DEVICES & CIRCUITS LAB	Semester:	Ι

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00	3.00	3.00	3.00	3.00
CO2	3.00	3.00	3.00	3.00	3.00
CO3	3.00	3.00	3.00	3.00	3.00
CO4	3.00	3.00	3.00	3.00	3.00
CO5	3.00	3.00	3.00	3.00	3.00
CO6	3.00	3.00	3.00	3.00	3.00
Inter	nal & Unive	ersity Attainment:	3.00	3.00	
		Weightage	25%	75%	
CO Attainment for th	e course (In	ternal, University	0.75	2.25	
CO Attainment for	the course	(Direct Method)		3.00	

Overall course attainment level3.00



Department of Electronics and Communication Engineering

Program Outcome Attainment (from Course)

Name of Faculty:	K.RAJENDER	Academic Year:	2022-23
Branch & Section:	ECE - A	Year:	II
Course Name:	ELECTRONIC DEVICES &CIRCUITS LAB	Semester:	I

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	1	1	1	1	2	2	2	3	3	3
CO2	-	1	3	-	-	1	1	1	2	2	2	2	3	3
CO3	1	3	-	-	1	1	1	1	2	2	2	-	3	3
CO4	1	-	2	2	-	1	1	1	2	2	2	3	3	3
CO5	1	-	3	-	1	1	1	1	2	2	2	2	3	3
CO6	3	3	-	-	-	1	1	1	2	2	2	3	3	3
Course	1.8	2.3	2.7	2.0	1.0	1.0	1.0	1.0	2.0	2.0	2.0	2.6	3.0	3.0

со	Course Outcome Attainment								
CO1	3.00								
CO2	3.00								
соз	3.00								
CO4	3.00								
CO5	3.00								
CO6	3.00								
Overall course atta	inment level 3.00								

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainme nt	1.80	2.25	2.67	2.00	1.00	1.00	1.00	1.00	2.00	2.00	2.00	2.60	3.00	3.00

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)