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COURSE FILE

ON

EMBEDDED SYSTEM DESIGN

Course Code - EC613PC

III B.Tech II-SEMESTER
A.Y.: 2022-2023

Prepared by

Mrs. A.Vaani Assistant Professor

Head of the Department Electronics and Communication Engg. Dept SRI INDU INSTITUTE OF ENGG & TECH Sheriguda(V), ibrahimpatnam(M), R.R.Dist-501 510



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year	2022-2023
Course Title	EMBEDDED SYSTEM DESIGN
Course Code	EC613PC
Programme	B. Tech
Year & Semester	III year II-semester
Branch & Section	ECE-A
Regulation	R18
Course Faculty	Mrs.A. Vaani, Assistant Professor

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Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510. Campus Ph: 9640590999, 9347187999, 8096951507.



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INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To Continuous assess of teaching-learning process through institute-industry collaboration.

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.

IM4: To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

DM1: To facilitate an academic environment that enables student's centric learning.

DM2: To provide state-of-the-art hardware and software technologies to meet industry requirements.

DM3: To continuously update the Academic and Research infrastructure.

DM4: To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

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PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

PEO1: Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.

PEO2: Graduates with ability to execute innovative ideas for Research and Development with continuous learning.

PEO3: Graduates inculcated with industry based soft-skills to enable employability.

PEO4: Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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PROGRAM OUTCOMES

- 1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- 2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- 3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- 4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- 5. **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
- 6. **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- 7. **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- 8. **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- 9. **INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- 10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.
- 11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- 12. **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING

III YEAR COURSE STRUCTURE AND SYLLABUS (R18)

Applicable From 2018-19 Admitted Batch

III YEAR I SEMESTER

S. No.	Course	Course Title	L	T	P	Credits
	Code					
1	EC501PC	Microprocessors & Microcontrollers	3	1	0	4
2	EC502PC	Data Communications and Networks	3	1	0	4
3	EC503PC	Control Systems	3	1	0	4
4	SM504MS	Business Economics & Financial	3	0	0	3
		Analysis				
5		Professional Elective - I	3	0	0	3
6	EC505PC	Microprocessors & Microcontrollers Lab	0	0	3	1.5
7	EC506PC	Data Communications and Networks Lab	0	0	3	1.5
8	EN508HS	Advanced Communication Skills Lab	0	0	2	1
9	*MC510	Intellectual Property Rights	3	0	0	0
		Total Credits	18	3	8	22

III YEAR II SEMESTER

S.	Course	Course Title	${f L}$	T	P	Credit
No.	Code					S
1	EC601PC	Antennas and Propagation	3	1	0	4
2	EC602PC	Digital Signal Processing	3	1	0	4
3	EC603PC	VLSI Design	3	1	0	4
<mark>4</mark>	EC613PE	Professional Elective - II	3	0	0	3
5		Open Elective - I	3	0	0	3
6	EC604PC	Digital Signal Processing Lab	0	0	3	1.5
7	EC605PC	e – CAD Lab	0	0	3	1.5
8	EC606PC	Scripting Languages Lab	0	0	2	1
9	*MC609	Environmental Science	3	0	0	0
		Total Credits	18	3	8	22

*MC - Environmental Science - Should be Registered by Lateral Entry Students Only.

Note: Industrial Oriented Mini Project/ Summer Internship is to be carried out during the summer vacation between 6th and 7th semesters. Students should submit report of Industrial Oriented Mini Project/ Summer Internship for evaluation.

Professional Elective – I

EC511PE Computer Organization & Operating Systems			
EC512PE	Error Correcting Codes		
EC513PE	Electronic Measurements and Instrumentation		

Professional Elective – II

EC611PE	Object Oriented Programming through Java				
EC612PE	Mobile Communications and Networks				
EC613PE	Embedded System Design				

EC613PC: EMBEDDED SYSTEM DESIGN

B.Tech. III Year II Semester

L T P C

3 0 0 3

Prerequisite: Microprocessors and Microcontrollers; Computer Organization and Operating Systems

Course Objectives:

- 1. To provide an overview of Design Principles of Embedded System.
- 2. To provide clear understanding about the role of firmware.
- 3. To understand the necessity of operating systems in correlation with hardware systems.
- 4. To learn the methods of interfacing and synchronization for tasking.

Course Outcomes: Upon completing this course, the student will be able to

- 1. TounderstandtheselectionprocedureofProcessorsintheembeddeddomain.
- 2. Design ProcedureforEmbeddedFirmware.
- 3. To visualize the role of Real time Operating Systems in Embedded Systems.
- 4. ToevaluatetheCorrelationbetweentasksynchronizationandlatencyissues

UNIT-I:

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT-II:

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT-III:

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT-IV:

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT-V:

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, **Task Synchronization**: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, Methods to Choose an RTOS.

TEXTBOOKS:

1. Introduction to Embedded Systems-ShibuK.V,McGrawHill.

REFERENCEBOOKS:

- 2. Embedded Systems-Raj Kamal, MH.
- 3. Embedded System Design-FrankVahid, TonyGivargis, JohnWiley.
- 4. Embedded Systems–Lyla, Pearson,2013
 An Embedded Software Primer-David E.Simon, Pearson Education



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Website: https://siiet.ac.in/

COs and Mapping with PO/PSO

Class: III ECE-A

Course: EMBEDDED SYSTEMS DESIGN (C324)

Course Outcomes

Aftercompletingthiscourse, the student will be able to:

C324.1: Describe the basics of an embedded system (Knowledge)

C324.2:Interpretthetypeofmemoryandinterfacingtoexternalworld(Application)

C324.3: Analyze the embedded firmwaredesign approaches (Analysis)

C324.4: Design the RTOS based embedded system for multitasking

(Synthesis)

C324.5:Expressthetaskcommunication/synchronizationissues

(Comprehension)

C324.6: Assesthemethodofdesigning an embedded system for any type of application (Evaluation)

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO	PO1	PO	PO	PO4	PO5	PO6	PO7	PO8	PO9	PO	PO1	PO	PS	PS
/C		2	3							10	1	12	01	O2
0														
C324.1	2	-	2	-	-	=	ı	-	-	=	-	ı	3	2
C324.2	2	-	3	-	-	-	-	-	-	-	2	-	2	3
C324.3	2	-	2	-	-	-	-	-	-	-	-	2	3	2
C324.4	3	-	3	-	-	-	ı	-	-	-	3	ı	2	3
C324.5	2	-	2	-	-	-	-	-	-	-	-	2	2	3
C324.6	2	-	3	-	-	-	-	-	-	-	-	3	3	2
AVG	2.17	-	2.5	-	-	-	-	-	-	-	2.5	2.3	2.5	2.5



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CO- PO/PSO Mapping - Justification

Course: EMBEDDED SYSTEM DESIGN (C324) Class: III ECE-A

P01.ENGINEERING KNOWLEDGE: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

P02.PROBLEM ANALYSIS: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

P03. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet t h e specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO11. PROJECT MANAGEMENT AND FINANCE: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

CO-PO mapping Justification

C324.1: Describe the basics of an embedded system (Knowledge)

	Justification			
PO1	Studentscandefinetheembeddedsystem, history and purpose.			
PO3	Basicsarethekeyfactorsindesigninganyapplications.			
PSO1	Embeddedsystemsengineercancreateasystemthatnotonlymeetsthespecified			
	requirements.			
PSO12	Embeddedsystemsenhancestheefficiency,accuracy,andcollaborationaspectsofthe			
	designprocess.			

C324.2:Interpretthetypeofmemoryandinterfacingtoexternalworld(Application)

	Justification
PO1	Students acqire knowledge on the core of embedded system with communication interfaces.
PO3	Studentscandesignapplicationwithknowledgeofprogrammemoryanddatamemory with
	interfacing circuitry.
PO11	Applyingtheseprinciplesensuresthesuccessfuldevelopmentofembeddedsystemsthat
	meetbothtechnicalandfinancialobjectives.
PSO1	understandingmemorytypes,optimizingmemory usage,andeffectiveinterfacingwith the
	externalworldalignskills.
PSO2	Enablingengineerstodevelopeffectivesolutionsintheembeddedsystemsdomain.

C324.3Analyze the embedded firmware design approaches (Analysis)

	Justification	
PO1	Studentsgettheknowledgeonresetcircuitandoscillatorunit.	
PO3	Studentscandotheembeddedfirmwaredesignapproaches.	
PO12	Abilitytointegrateengineeringandmanagementprinciplesiscrucialforsuccessful	
	embedded firmware design projects in multidisciplinar yen vironments.	
PS01	Embeddedfirmwaredesignapproachimpactsthedesign, analysis, and development of	
	economical systems in the domains of both Embedded Systems and VLSIDe sign.	
PSO2	Firmware design under consideration and the engineering problems being addressed.	

C324.4 Design the RTOS based embeddedsystem formultitasking (Synthesis)

	Justification
PO1	Studentsgettheknowledgeonoperatingsystem.
PO3	Operatingsystem, multiprocessing and multitasking plays an important role indesigning
	anyapplication.
PO11	RTOS-basedembeddedsystemformultitaskinginvolvesadheringtoengineeringprinciples
	relatedtotask.
PSO1	Developmentofaneconomicalyethighlyfunctionalembeddedsystem
PSO2	Realtimeresponsiveness, efficients our ceutilization, and robust multitasking capabilities.

C324.5 Express the task communication/synchronization issues(Comprehension)

	Justification			
PO1	Studentsgettheknowledgehowto choosearealtimeoperating systemforembedded			
	systemapplication.			
PO3	Hardandsoftrealtimeoperatingsystemsconsideredbasedondesignmethodologies.			
PO12	Techniqueandadapttotheever-			
	evolvinglandscapeoftechnologicalchallengesinembeddedsystem.			
PSO1	Approachthatoptimizesbothsystemperformanceandcost-effectiveness.			
PSO2	Theintegration of these tools allows for a comprehensive and multidisciplinary approach to			
	optimizesystem.			

$C324.5 \ \ Asses the method of designing an embedded system for any type of application (Evaluation)$

	Justification
PO1	Studentsgettheknowledgehowtochooseapplicationsbasedoncurrenttrendytechnology.
PO3	The application areas and the products in the embedded system domain are countless.
PO12	This optimization involves incorporating the latest technologies, minimizing resource usage.
PSO1	Emphasizingthedesign, analysis, and development tools of economical system in the field of Embedded System.
PSO2	Processcontributetoaefficientapproach, allowing for optimization, thoroughtesting, iterative of the
	system.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD <u>ACADEMIC CALENDAR 2022-23</u>

B. Tech./B. Pharm. III YEAR I & II SEMESTERS

I SEM

S. No	8	Duration		
	Description	From	То	
1	Commencement of I Semester classwork	1	09.09.2022	
2	1 st Spell of Instructions (including Dussehra Recess)	09.09.2022	10.11.2022 (9 Weeks)	
3	Dussehra Recess	03.10.2022	08.10.2022 (1 Week)	
4	First Mid Term Examinations	11.11.2022	17.11.2022 (1 Week)	
5	Submission of First Mid Term Exam Marks to the University on or before		24.11.2022	
6	2 nd Spell of Instructions	18.11.2022	12.01.2023 (8 Weeks)	
7	Second Mid Term Examinations	16.01.2023	21.01.2023 (1 Week)	
8	Preparation Holidays and Practical Examinations	23.01.2023	28.01.2023 (1 Week)	
9	Submission of Second Mid Term Exam Marks to the University on or before	,	30.01.2023	
10	End Semester Examinations	30.01.2023	11.02.2023 (2 Weeks)	

Note: No. of Working/instructional days: 92

II SEM

		Duration		
S. No	Description	From	To	
1	Commencement of II Semester classwork	13.02.2023		
2	1 st Spell of Instructions	13.02.2023	08.04.2023 (8 Weeks)	
3	First Mid Term Examinations	10.04.2023	15.04.2023 (1 Week)	
4	Submission of First Mid Term Exam Marks to the University on or before	22.04.2023		
5	2 nd Spell of Instructions (including Summer Vacation)	17.04.2023	24.06.2023 (10 Weeks)	
6	Summer Vacation	15.05.2023	27.05.2023 (2 Weeks)	
7	Second Mid Term Examinations	26.06.2023	01.07.2023 (1 Week)	
8	Preparation Holidays and Practical Examinations	03.07.2023	08.07.2023 (1 Week)	
9	Submission of Second Mid Term Exam Marks to the University on or before	08.07.2023		
10	End Semester Examinations	10.07.2023	22.07.2023 (2 Weeks)	

Note: No. of Working/instructional days: 90

REGISTRAR



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING Class Timetable

-	-	Contract of the Contract of th	1.2022-23		SEMESTER: II	L	H: C-201
9:40-10:30	10:30 -11:20	The state of the s	IV 12:10-1:00	1:00-	V	VI	VII
A&P	Г			1:30		2:20-3:10	3:10-4:00
IM			in the same of		VLSID	ESD	LIB
	10/22/1	FAI	ESD	T.	DSP(T)/VLSID(T)	A&P	SPORTS
ESD	IM	A&P	A&P(T)/DSP(T)			District Co.	SPORTS
IM	DSP	VISID		N	FAI	DSP	COUN
FAI	Deb			C	e-CAI	LAB / DSP LA	В
200000		A&P	VLSID	н			
		VLSII	D(ADIUNCT)		LUD	CO-C	U/DAA
֡	A&P IM ESD IM FAI VLSID	A&P D IM DSP ESD IM IM DSP FAI DSP VLSID ESD	I II III 9:40-10:30 10:30-11:20 11:20-12:10 A&P DSP LAB/e-CA IM DSP FAI ESD IM A&P IM DSP VLSID FAI DSP A&P	9:40-10:30 10:30 -11:20 11:20-12:10 12:10-1:00 A&P DSP LAB / e-CAD LAB IM DSP FAI ESD ESD IM A&P A&P(T)/DSP(T) IM DSP VLSID VLSID(T)/A&P(T) FAI DSP A&P VLSID VLSID VLSID VLSID	I	I	I

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the	
EC601PC	A&P-Antennas and Propagation	P.Krishna Rao	EC604PC	DSP LAB-Digital Signal Processing Lab	Faculty Y.Raju/Dr.T.Ramakrishna/ Dr.S.Anjaneyulu	
EC602PC	Den District	1.0	EC605PC	e-CAD LAB-e - CAD Lab	S.Alekhya/P.Rajendra/P.Krishna	
ZCOOZIC	DSP-Digital Signal Processing	Y.Raju	EC606PC	SL LAB-Scripting	D.Nagaraju/P.Krishna Rao/	
EC603PC	VLSID-VLSI Design	S.Alekhya		Languages Lab FAI-Fundamentals of	K.Bhaskar Reddy	
EC613PE	ESD-Embedded System			Artificaial Intelligence	P.Meena	
VLSID	Design(Professional Elective-II)	A.Vaani	COUN	Counseling	V Pain/V Pada /O C	
ADJUNCT)	VLSID(ADJUNCT)	G.Chandrasekhar	SPORTS	Sports	Y.Raju/K.Padma/G.Swathi	
	E IM-Industrial Management (Open Elective-I) K.V.I	K.V.Nagamani	CO-	A CONTRACTOR OF THE PROPERTY O	P.Srilatha/B.Ashwini	
MT600OE			con Elective-I) K.V.Nagamani CU/DAA Assoc. Activities	Co-Curricular/Dept, Assoc.Activities	S.Alekhya/S.Naresh/K.Bhaskar	
	Class Incharge		LIB	Library	G.Nirmala/A Swetha	
	стазэ кимпагус		of the Deport the Depo	Partification Engg. Dept ENGG & TECH	Principal Course So Indu Institute of Engineerin Sheriguda(VIII), Ibrahimpa	

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LESSONPLAN

Programme:B.Tech	AcademicYear:2022-23
Year: III	Semester:II
Course Title: EMBEDDED SYSTEM DESIGN	CourseCode:EC613PE
NameofFaculty: A.VAANI	

Unit-I Syllabus

Introduction toEmbedded Systems: Definition of Embedded System, Embedded Systems VsGeneral Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

.

No.ofSe ssions Planned	Topics	Reference	Teaching Method/ Aids
1	DefinitionofEmbedded Systems	T1,R1	BB
1	EmbeddedSystems/Generalcomputingsystems	T1	BB
1	HistoryofEmbeddedsystems	T1,R1	BB
2	Classification	T1,R1	BB,PPT
2	Majorapplicationsareas	T1	BB
1	PurposeofEmbeddedsystems	T1,R1	BB
2	Characteristics and quality attributes of embedded systems	T1	BB
Gap beyo	ndsyllabus(ifany):	•	•

Gapwithinthesyllabus(ifany)

Course Outcome 1: Describe the basics of an embedded system.

^{*}SessionDuration:50minutes

^{*}TotalNumberofHours/Unit:10

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Unit-II Syllabus

Typical Embedded System: Core of the Embedded System: General Purpose and DomainSpecific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and ExternalCommunicationInterfaces.

No.of	Topics	Reference	Teaching		
Sessions	_		Method/		
Planned			Aids		
1	Coreofthe Embedded Systems	T1	BB		
1	GeneralpurposeandDomainspecificprocessors	T1, R1	BB		
1	ASIC'S	T1	BB		
1	PLD'S	T1,R 1	BB		
1	CommercialOfftheshelfcomponents(COTS)	T1	BB		
1	Memory:ROM,RAM	T1,R1	BB,PPT		
1	Memoryaccordingtothe typeofInterface	T1	BB		
1	Memoryshadowing	T1	BB		
1	MemoryselectionforEmbeddedsystems	T1,R1	BB		
1	SensorsandActuators	T1, R2	BB		
2	CommunicationInterface:Onboardand External communicationinterface	T1, R1	BB,PPT		
Gapbeyondsyllabus(ifany):					
Gap withinthesyllabus(ifany)					
CourseO	utcome1:Interpret thetypeofmemoryandinterfacingtoexterna	alworld			

^{*}SessionDuration:50minutes

^{*}TotalNumberofHours/Unit:12



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Unit-IVSyllabus

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

No.ofSe ssions Planned	Topics	Reference	Teaching Method/ Aids
3	Ope rating System Basics	T1	BB
1	Types of operating Systems	T1, R1	BB
2	Tasks, Process, and Threads	T1, R1	BB
1	Multi-processing and Multitasking	T1, R3	BB
3	Task scheduling	T1, R2	BB, PPT

Gap beyond syllabus (if any):

Gap within the syllabus (if any)

CourseOutcome1: Express the task communication/synchronization issues

^{*}SessionDuration:50minutes

^{*}Total Number of Hours/Unit:10

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Unit-V Syllabus

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, Methods to Choose an RTOS.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Shared Memory	T1, R1	BB
2	Message passing	T1, R1	BB
1	Remote procedure call and Sockets	T1, R1	BB
1	Task synchronization.	T1	BB
2	Task Communication/Synchronization issues	T1, R3	BB, PPT
2	Task synchronization Techniques	T1, R1	BB
1	Device drivers.	T1, R3	BB
2	How to choose an RTOS	T1, R1	BB

Gap beyond syllabus (If any):

Gap within the syllabus (if any)

CourseOutcome1: Asses the method of designing an embedded system for any type of application

TEXTBOOKS:

T1. Introduction to Embedded Systems- Shibu K.V, McGraw-Hill.

REFERENCEBOOKS:

- R1. Embedded Systems-Raj Kamal, MH.
- R2. Embedded System Design-Frank Vahid, TonyGivargis, JohnWiley.
- R3. Embedded Systems-Lyla, Pearson, 2013
- R4. An Embedded Software Primer-David E.Simon.PearsonEducation

^{*}SessionDuration:50minutes

^{*}Total Number of Hours/Unit:12

WEBREFERENCES:

- W-1. Real Time Applications of Embedded Systems-Elprocus
- W-2. Peripheral Devices-java t point
- W-3. https://iqramali.medium.com/role-of-rtc-real-time-clock-in-embedded-devices-35dbd2e8f9e7
- W-4. <u>Difference Between Sensors and Actuators (with Comparison Chart) -Tech Differences</u>
- W-5 https://www.tutorialspoint.com/operating-system/index.htm

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Lecture notes

Unit 1 link:

https://drive.google.com/file/d/1nUIFO4Cqzgo2zz0_SFSN8mEWi1XnlouD/view?usp=drive_link

Unit 2 link:

https://drive.google.com/file/d/1FSyMyp4h6ZuyPWhCYPQrquJzaSgMSiGT/view?usp=drive link

Unit 3 link:

https://drive.google.com/file/d/1xIAtJZuKkXuw9CBID4aZmWyNhkS5qaiN/view?usp=drive link

Unit 4 link:

https://drive.google.com/file/d/1iGpre70lhEHXCI1Bv7dMziT-wZqsGtM/view?usp=drive_link

Unit 5 link:

https://drive.google.com/file/d/1nXT4OLmeiUmcC7fm1n0xzJjdWmMnjq_m/view?usp=drive_link



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Power point presentation

PPT link:

https://drive.google.com/file/d/1viOmtEg7R4umffv7LGO7G9pMA3l97q8j/view?usp=sharing

Code No: 156AV

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech III Year II Semester Examinations, February - 2023 EMBEDDED SYSTEM DESIGN

(Electronics and Communication Engineering) **Time: 3 Hours** Max. Marks: 75 **Note:** i) Question paper consists of Part A, Part B. ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions. iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions. PART - A **(25 Marks)** 1.a) What is fourth generation embedded system? Give an example. [2] Mention the significance of prototype development. b) [3] List the components of a typical embedded system. c) [2] What is memory shadowing? What is the advantage of it? d) [3] What is the difference between static and global functions? e) [2] Mention the advantages of assembly language based ES firmware. f) [3] List different types of operating systems. g) [2] Write about preemptive scheduling. h) [3] Differentiate between stream sockets and datagram sockets. i) [2] Write about message queue. **i**) [3] PART - B **(50 Marks)** Illustrate the various purposes of embedded system with relevant examples. 2. [10] 3.a) What is non-operational quality attribute? Discuss the important non-operational quality attributes examined in any design of embedded systems. Explain the different classification of embedded systems by giving example for each. b) [5+5]What is the significance of onboard communication interface? Explain the difference 4. a) between I²C and SPI communication interface. Expand the terms RISC and CISC. Compare RISC vs CISC processor. b) [5+5]OR Discuss the classification of working memory with implementation sketches. 5. a) Write a short notes on ASICs and COTs by citing their drawbacks. b) [5+5]

6. a)	Explain the role of Watchdog timer in embedded system.	
b)	What is the difference between 'Super loop' based and 'OS' based embedded firm	mware
	design? Which one is the better approach?	[5+5]
	OR	
7.a)	What is Interrupt Vector Address and Interrupt Service Routine (ISR)? How are related?	they
b)	What is function pointer? Explain the use of function pointers.	[5+5]
8. a)	What are the differences between multitasking and multiprocessing? Explain.	
b)	Give a detail structure of task and a process.	[5+5]
	OR	
9.	Discuss the basic functions performed by a Real-Time kernel.	[10]
10. a)	What is priority inversion? What are the different techniques adopted for hapriority inversion?	ndling
b)	Explain the architecture of device drivers.	[5+5]
ŕ	OR	
11.	Describe different functional and non-functional requirements needed in the sele of RTOS.	ction [10]
	of RTOS.	[10]
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Code No: 156AV

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech III Year II Semester Examinations, August - 2022 EMBEDDED SYSTEM DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours

Max.Marks:75

Answer any five questions All questions carry equal marks

- - -

1.a) b)	Define an embedded system. Explain the characteristics of Embedded Systems. List out the major application areas of embedded systems.	[7+8]
2.a) b)	Distinguish about portability and reliability in embedded system design. What are the various purposes of embedded systems with illustrative examples?	[8+7]
3.a) b)	Explain the role of sensors in embedded system design. What are the different factors that needs to be considered in the selection of memore embedded systems?	ry for [7+8]
4.a) b)	Illustrate the differences between general purpose and domain specific processors. Discuss about on-board communication interfaces in brief.	[8+7]
5.a) b)	What is the need of an embedded firmware? Discuss. Narrate about the embedded firmware development languages.	[7+8]
6.a) b)	Explain the functions of Watchdog timer in an embedded system. Describe the purpose of a Real Time Clock in an embedded system, and explain.	[8+7]
7.a) b)	How different thread binding models, used for user and kernel level threads? Define starvation in the process of scheduling context. Explain how starvation can effectively tackled?	be [8+7]
8.a) b)	How the concept of Shared memory is used in task communication? Explain message-passing communication system in detail.	[8+7]

Code No: 156AV

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech III Year II Semester Examinations, February/March - 2022 EMBEDDED SYSTEM DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours Max. Marks: 75

Answer any five questions All questions carry equal marks

- - -

1.	Explain the different classification of embedded systems with an example.	[15]
2.a) b)	What are the operational attributes of an embedded system? Explain. What are the different present technologies used in embedded systems.	[10+5]
3.a) b)	Differentiate Harvard and Von-Neumann architectures. What are the advantages of PLDs over fixed logic devices? Explain.	[8+7]
4.a) b)	Classify the program storage memory and explain. Explain the different external communication interfaces in brief.	[8+7]
5.	Explain the advantages and drawbacks of Assembly language based emb firmware development.	edded [15]
6.a) b)	Explain the embedded firmware design. Explain the following: (i) Brown-out protection circuit (ii) Real-time clock	[8+7]
7.a) b)	Differentiate process and thread. Write some examples. What are the different types of multitasking? Explain.	[8+7]
8.a) b)	What are the different conditions favoring a deadlock situation? Explain. Explain the role of device driver in embedded OS based products.	[8+7]

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Code No: 156AV

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech III Year II Semester Examinations, August/September - 2021 EMBEDDED SYSTEM DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours Max. Marks: 75

Answer any five questions All questions carry equal marks

	All questions carry equal marks	
1.a) b)	Describe the general characteristics of embedded systems in detail. Relate the Application Specific Embedded system with an example.	[7+8]
2.a) b)	Narrate various purposes of embedded systems with illustrative examples. What are different current technologies used for embedded system design briefly.	? Explain [8+7]
3.a)	What are different types of memories used in embedded systems? Explain	n with
b)	examples. Explain the different on-board communication interfaces in brief.	[8+7]
4.a) b)	With a neat diagram, explain the architecture of a general purpose processor. Explain about ASICs, PLDs and COTs.	[8+7]
5.a) b)	Justify the need of brown out protection circuit in Embedded systems. Discuss the significance of Watchdog timer in an Embedded System.	[7+8]
6.a)	What is the need of an embedded firmware? Briefly explain the embedded development languages.	firmware
b)	Write a short note on Real Time Clock.	[10+5]
7.a) b)	What is task scheduling? Explain Round Rabin scheduling algorithm. What is a process? With a neat representation explain the process states transition.	and state [7+8]
8.a) b)	Explain message passing technique for inter process communication in detail. Explain how semaphores are used for task synchronization.	[8+7]

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I - Mid Examinations, MAY -2023

Year & Branch: III -ECE (A, B)

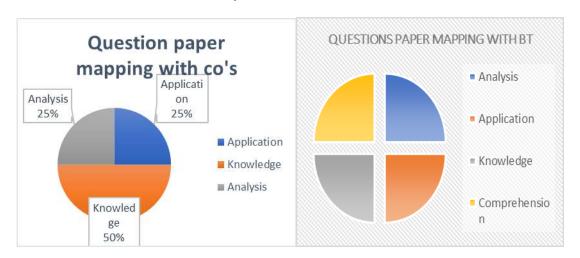
Subject: **ESD** Max. Marks: 10

Date: 09/05/23(AN) -

Time: 60 mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

- 1.Write about the Brown-Out protection circuit and explain about Realtime clock. (5M) (C324.3)(Knowledge)
- 2) Explain the different On-board communication interfaces in brief. (5M) (C324.2) (Application)
- 3) Discuss about various application area of embedded system and give example for each application area. (5M) (C324.1) (Knowledge)
- 4) Whatarethedifferent types of Memories used in Embedded system designed explain each role in detail. (5M) (C324.2) (Analysis)



Set -I

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II - Mid Examinations, JUNE -2023

Year & Branch: III -ECE (A,B)

Subject: **ESD**

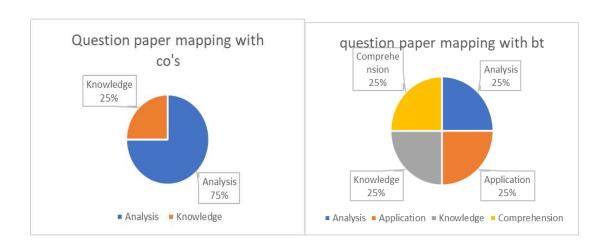
Max. Marks: 10

Date: 27/06/23(AN) Time: 60 mins

Answer any **TWO** Questions. All Question Carry Equal Marks

2*5=10 marks

- 1) Explain about the embedded firmware design approaches and embedded firmware development languages (5M) (C324.3) (**Analysis**).
- 2) What is a process? With a neat representation explain the process states and state transition. (5M) (C324.3) (**Knowledge**)
- 3) Explain message passing technique for inter process communication in detail. (5M) (C324.5) (Analysis)
- 4). Explain about the different types of multi-tasking models in the OS context (5M) (C324.4) (Analysis).



Set -I

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501510

B-Tech I - Mid Examinations, MAY-2023

Objective Type Exam

Year &Branch: III -ECE-A, B&C Date: 09-05-2023(AN)

Subject: ESDMax. Marks: 10Time: 20 minsName:Roll No

I. Choose the correct alternative: 1. The first recognized modern embedded system is () a) Apple computer b) Apollo guidance computer c)Calculator d) Radio navigation system **2.** Which of the following is not an example of small-scale embedded system? a) Electronic Barbie doll b) simple calculator () c)cellphone d) electronic toy car **3.** Whichofthefollowingistheexampleoffourthgenerationembeddedsystem? b) electronic toy car a) smart phone devices ()c) simple calculator d) SCADA device **4.** A digital multimeter is an example of embedded system for ()a) data communication b)monitoring) control d)none of these 5 Whichof the following is an example of embedded system For data communication.) b) network router a) music player c) digital camera d) none of these 6. Which of the following is an example of on-board communication interface. a) I2C b) SPI c) UART d) all of these) 7. Which of the following is an example of external communication interface? a) Bluetooth b) wi-fi c) GPRS d) all of these) 8. Serial Peripheral Interface supports the () a) half duplex synchronous protocol b) full duplex synchronous protocol c) both a and b d) none of these 9. What is the work of oscillator unit in embedded system.) a) Reference for time b) Reset the circuit

d) none of these

c)generate clock pulses

10. Brown-out protection circuit turn off the system when the voltage of the	
Embedded system is	()
a) Below the specified level b) above the specified level	
c)both a and b d) none of these	
I. Fill In the Blanks:	
11. Embedded system is a combination of bothand	
12. First generation embedded systems built aroundbit microprocessor.	
13. Expand the ASIC	
14. Watch dog timer is used tosystem if the system gets stuck somewhere in middle of the program.	
15Whatis thefullformofI2C	
16. What is the full form of UART	
17. GPRS is a packet orientedserviceon2G &3Gcellularsystems.	
18. ROMistype of memory.	
19. Expand the EEPROM	
20. Firm ware is also called as	

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 **B-Tech II - Mid Examinations, June-2023**<u>Objective Type Exam</u>

Year &Branch: III -ECE-A, B Date: 27-06-2023(AN)

Subject: ESD Max. Marks: 10 Time: 20 mins

Name:Roll No.....

T	. Choose	the	correct	alterr	ative.
1	. CHOOSE	uic	COLLECT	anten	ialive.

1. Translation of assembly code to machine code is performed by the a) assembler b) compiler c) linker d) locater	()		
 2. Assembly language is the human read able notation of? a) Machine language b) high level language c)both a and b d) none of these 	()		
3. Interrupt which occur in sync with the currently executing task are known as	s?()	
a) asynchronous interruptsb) synchronous interruptsc)external interruptsd) none of these				
4. Aprocesshas. a) stack memory b) program memory c) data memory d) All of these				
5. Whatarethedifferenttypesofmultitaskingpresentinoperatingsystem.a) co-operativeb) preemptivec) non-emptived) all of these	()		
6. Who determines which task/process is to execute data given point of time. (a) Context paper c) scheduler d) none of these.)		
7. Which of the following techniques issued by operating systems for inter process () communication?				
a)shared memory b)messaging c)signaling d)all of these				
8)Which among the following techniques is used for sharing data between process()				
a) semaphoresb) shared memory c) messages d) both b and c				
8. Which among the following is a shared memory technique for IPC. ()				
a)pipes b) memory mapped object c)message blocksd) both a and b				

9. Process/Task synchronization is essential for. ()					
a) avoiding conflicts in resource access in multi-tasking environment b)ensuring proper sequence of operation across processes					
c)communicating between processes d)all of these					
I. FillInTheBlanks:					
10. Translation of assembly code to machine code is performed by					
11.Super loop based approach require an operating system(yes or no)					
13.A process can have any threads of execution(True or False)					
14. The ability of a system to execute multiple processes simultaneously is known as					
15.Missing deadline for tasks are acceptable in real time systems.					
16.For a good scheduling algorithm the CPU utilization is					
17. Shared memory techniques for IPC are and 18In which a process does not get the CPU or system resources required to continue its execution for a long time is called as					
19 is a piece of software that acts as a bridge between the operating system and					
hardware.					
20.IPC full form					

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 **B-Tech I - Mid Examinations, MAY-2023**

Year &Branch: III -ECE-A, B&C Date: 09-05-2023(AN)

Subject: ESD

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1zXaKtgVMADpPcKxgLhVnSR D9KDJ cKLE/view?usp=sharing

Objective Key Paper

T	Chanse	the	correct	altern	ative
				<i>~</i> 111.4.1 1	

1.a
2.c
3.a
4.c
5.c
6.d
7.d
8.b
9.c

Fill in the blanks:

- 11. S/wand H/w
- 12. 8bits
- 13. Yes
- 14. Applicationspecificintegratedcircuit.
- 15. InterIntegratedCircuitBus.
- 16. Universal Asynchronous receiver and transmitter.
- 17. Wirelessdatacommunication.
- 18. Non-volatilenature.
- 19. electrically erasable program read only memory.
- 20. software.

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 **B-Tech II - Mid Examinations, June-2023**

Year &Branch: III -ECE-A, B Date: 27-06-2023(AN)

Subject: ESD

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1K11g0OZ9g9GZoqgBIDhv OycO_B33naio/view?usp=sharing

Objective Key Paper

I. Choose the correct alternative:

1.a	
2.b.	
3.d	
4. b	
5.b	
6.c	
7.d	
8.d	
9.b	
10.a	

Fill in the blanks:

- 11. Assembler
- 12. No
- 13. Yes
- 14. Multitasking
- 15. Realtimesystem
- 16. Scheduling-0-100
- 17. memorysharedbetweentwoor moreprocessors
- 18. Schedulingforoperatingsystem
- 19. kernel
- 20. Inter process communication

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ASSIGNMENT-1

SUBJECT: ESD

- 1)Write about the Brown-Out protection circuit and explain about Real time clock. (C324.3) (Knowledge)
- 2) Explain the different On-board communication interfaces in brief. (C324.2) (Application)
- 3) Discuss about the various applications on area of embedded system and give the examples of an application area. (C324.1) (Knowledge)
- 4) What are the different types of memories used in embedded system and explain in details (C324.2) (Analysis)
- 5) Difference between general computing system and embedded system. (C324.1) (Analysis)
- 6) Difference between SRAM and DRAM.

(C324.2) (Analysis)

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ASSIGNMENT- 2

SUBJECT: ESD

- 1) Explain about the embedded firmware design approaches and embedded firmware development languages. (C324.3) (Analysis)
- 2) What is a process? With a neat diagram explain about the process state and state transition. (C324.3) (Knowledge)
- 3)Explain the message passing technique for inter process communication in detail. (C324.5) (Analysis)
- 4)Explain about the different multitasking models in the OS context. (C324.4) (Analysis.)
- 5) Explain about the device drivers (C324.3) (Analysis)



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CourseTitle	Embedded system design (professional elective-II)
CourseCode	EC613PE
Programme	B.Tech
Year&Semester	IIIyearI-semester, Asec
Regulation	R18
CourseFaculty	A.VAANI,AssistantProfessor,ECE

Slowlearners:

SNo	Rollno	Noofbacklogs	Internal-IStatus	Internal-IIStatus
1	20X31A0401	4	21	21
2	20X31A0403	5	14	14
3	20X31A0406	4	21	22
4	20X31A0407	3	20	20
5	20X31A0408	3	19	20
6	20X31A0410	5	14	14
7	20X31A0411	4	24	24
8	20X31A0412	5	19	14
9	20X31A0413	4	22	22
10	20X31A0418	8	14	14
11	20X31A0419	4	21	21
12	20X31A0423	3	22	22
13	20X31A0427	3	20	21
14	20X31A0428	4	20	21
15	20X31A0430	4	24	24
16	20X31A0431	5	21	21
17	20X31A0433	3	14	22
18	20X31A0435	3	22	22
19	20X31A0436	5	19	20

20	20X31A0440	4	23	22
22	20X31A0445	4	24	22
23	20X31A0447	3	24	23
24	20X31A0450	4	23	23
25	20X31A0453	4	24	22
26	20X31A0454	5	14	14
27	20X31A0455	4	21	18
28	20X31A0456	5	22	14
30	20X31A0458	3	22	22
31	20X31A0462	3	21	22

Advancedlearners:

S.NO	ROLL.NO.	SeminarTopics
1	20X31A0404	1.EmbeddedSystems.
_		2.Purpose ofEmbedded
2	20X31A0409	Systems.
		3.Coreof theEmbedded
3	20X31A0415	3.coreor incliniocuded
3	20A31A0413	Cristan
4	20X31A0416	System. 4.DomainSpecific
 4	20X31A0416	<u>*</u>
		Processors.
5	20X31A0420	5.ASICs, PLDs, Commercial
		Off-The-ShelfComponents
6	20X31A0421	(COTS).
		6.Onboardand External
7	20X31A0422	CommunicationInterfaces.
,	20A31A0422	
		7.Brown-out Protection
8	20X31A0425	Circuit.
		0.5.1.11.15
		8.Embedded Firm ware
9	20X31A0432	5
1.0		Design Approaches.
10	20X31A0434	9.OperatingSystemBasics.
		10.Multiprocessingand
11	20X31A0437	Multitasking.
		11.Remote ProcedureCall and
12	20X31A0438	Sockets.
	201131110130	
- 10		12. TaskSynchronization.
13	20X31A0439	13. MethodstoChoose an
14	203/21 4 0 4 4 2	DTOS
14	20X31A0442	RTOS.
15	20X31A0444	
	20/131/10777	
16	20X31A0449	

17	20X31A0452
18	20X31A0459
19	20X31A0459



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BATCH ECE-III BTECH II SEM ECE-A RESULT ANALYSIS

ACADAMIC	CADAMIC COURSE		R OF NTS	QUESTIO SETI		
YEAR	NAME	APPEARED	PASSED	INTERNAL	EXTERNAL	PASS%
2022-23	EMBEDDED SYSTEM DESIGN	60	49	COURSE FACULTY	JNTUH	81.16

EMBEDDED SYSTEM DESIGN (C324) RESULT ANALYSIS





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Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING REMEDIAL CLASSES TIME TABLE

A.Y 2022-23

SEMESTER-II

BRANCH/ SEC	MON 4.00 PM- 5.00 PM	TUE 4.00 PM- 5.00 PM	WED 4.00 PM- 5.00 PM	THUR 4.00 PM- 5.00 PM	FRI 4.00 PM- 5.00 PM
II ECE-A	EMF&W	LTNM	A&DC	LICA	ECA
II ECE-B	LICA	A&DC	EMF&W	ECA	LTNM
III ECE-A	DSP	VLSID	A&P	ESD	IM
III ECE-B	A&P	ESD	DSP	IM	VLSID
III ECE-C	IM	A&P	ESD	VLSID	DSP
IV ECE-A	WSN	ML	LPVLSID	-	-
IV ECE-B	ML	LPVLSID	WSN	-	-
IV ECE-C	LPVLSID	WSN	ML	L	-

Head of the Department

Head of the Department

Electronics and Communication Eng. 5 TECH

Electronics and TITUTE OF ENG. 8 TECH

SRI INDU INSTITUTE OF ENG. 8. R. Disk-501 519

Sheriguda(V), Ibrahimpaham(M), R.R. Disk-501 519

Sheriguda(V), Ibrahimpaham(M), R.R. Disk-501 519

PRINCIPAL
Sin Indu Institute of Engineering & Technology
Sheriguda(Vill), Ibrahimpatham
R R Dist Telangana 501 510



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Website: https://siiet.ac.in/

ASSIGNMENTS AND REGISTERS

Assignment 1 script link:

https://drive.google.com/file/d/17auxtQB00K7Obr8ULH7w9eLJ3fRpsB7t/view?usp=sharing

Assignment 2 script link:

https://drive.google.com/file/d/1hvNfBQOwhNhxvKd5ytZS7dGCYgs7YM1n/view?usp=sharing

Attendance register link:

 $\underline{https://drive.google.com/file/d/1pQNLwrmlhUMpVDqUyhlcbsr06LUsHDjN/view?}_{usp=sharing}$

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty :A.VAANIAcademic Year:2022-2023Branch & Section:ECE - AExamination:I InternalCourse Name:ESDYear: IIISemester: II

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj	A
Max.	Marks ==>	5		5		5		5		10	5
1	20X31A0401	5		2						9	5
2	20X31A0402	3		4						9	5
3	20X31A0403					2		2		5	5
4	20X31A0404	3				5				9	5
5	20X31A0405			5		4				9	5
6	20X31A0406			4		4				8	5
7	20X31A0407			4		3				8	5
8	20X31A0408			3		3				8	5
9	20X31A0409	5		5						10	5
10	20X31A0410	2						2		5	5
11	20X31A0411					5		5		9	5
12	20X31A0412			3		3				8	5
13	20X31A0413			4		4				9	5
14	20X31A0414	5				5				9	5
15	20X31A0415	5						5		9	5
16	20X31A0416					4		4		8	5
17	20X31A0417	5		5						9	5
18	20X31A0418	2						2		5	5
19	20X31A0419			4		4				8	5
20	20X31A0420			4		3				8	5
21	20X31A0421			4		4				8	5
22	20X31A0422	4		4						9	5
23	20X31A0423			4		4				9	5
24	20X31A0424			4		4				8	5
25	20X31A0425			5		4				8	5
26	20X31A0426			5		5				8	5
27	20X31A0427			3		4				8	5
28	20X31A0428			3		4				8	5
29	20X31A0429			4		4				8	5
30	20X31A0430	5				5				9	5
31	20X31A0431	4		4						8	5
32	20X31A0432	5		5						9	5
33	20X31A0433					4		4		9	5
34	20X31A0434			5		5				9	5
35	20X31A0435			4		4				8	5
36	20X31A0436			3		3				8	5
37	20X31A0437			5				5		8	5
38	20X31A0438	5		5						9	5
39	20X31A0439			5		5				9	5
40	20X31A0440			5		4				9	5

											_
41	20X31A0441			4				5		8	5
42	20X31A0442			5		5				9	5
44	20X31A0444	5				5				8	5
45	20X31A0445	5		5						9	5
46	20X31A0446					5		5		9	5
47	20X31A0447	5		5						9	5
48	20X31A0448					4		5		8	5
49	20X31A0449	5		5						9	5
50	20X31A0450			5		4				9	5
51	20X31A0451			5		5				9	5
52	20X31A0452	5				5				9	5
53	20X31A0453	5				5				9	5
54	20X31A0454	2						2		5	5
55	20X31A0455			5		4				7	5
56	20X31A0456			4		4				9	5
58	20X31A0458			4		5				8	5
59	20X31A0459			5				5		9	5
60	20X31A0460			4		4				8	5
61	20X31A0461	5				5				9	5
62	20X31A0462			4		4				8	5
Targ	et set by the faculty	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Num	ber of students	19	0	42	0	41	0	9	0	56	60
Num	ber of students	22	0	43	0	42	0	13	0	60	60
atten	npted	22	U	43	U	42	U	13	U	60	60
	entage of students	86%		98%		98%		69%		93%	100%
score	ed more than target										

CO Mapping with Exam Questions:

CO - 1	Y			Y	Y	Y
CO - 2		Y			Y	Y
CO - 3			Y		Y	Y
CO - 4						
CO - 4 CO - 5 CO - 6						
CO - 6						

	% Students Scored	86%		98%	98%	69%	93%	100%
,	CO Attainment based o	n Exam	Questio	ns:				
	CO - 1	86%				69%	93%	100%
	CO - 2			86%			93%	100%
	CO - 3				98%		93%	100%
	CO - 4							
	CO - 5							
	CO - 6							

СО	Subj	obj	Asgn	Overall	Level
CO-1	78%	93%	100%	90%	3.00
CO-2	86%	93%	100%	93%	3.00

۱tt	ainment L	evel	
	1	40%	
	2	50%	

CO-3	98%	93%	100%	97%	3.00
CO-4					
CO-5					
CO-6					

3	60%	

Attainment (Internal 1 Examination) = 3.00



Course Outcome Attainment (Internal Examination-1)

Name of the faculty :A.VAANIAcademic Year:2022-2023Branch & Section:ECE - AExamination:II InternalCourse Name:ESDYear: IIISemester: II

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj4	A
Max. N	Marks ==>	5		5		5		5		10	5
1	20X31A0401			4		4				8	5
2	20X31A0402			5		4				9	5
3	20X31A0403	2						2		5	5
4	20X31A0404			5		4				8	5
5	20X31A0405			4		5				8	5
6	20X31A0406			4		5				8	5
7	20X31A0407			4		4				7	5
8	20X31A0408			4		4				7	5
9	20X31A0409			5		5				9	5
10	20X31A0410			5						4	5
11	20X31A0411			5		5				9	5
12	20X31A0412					5				4	5
13	20X31A0413			4		4				9	5
14	20X31A0414			5		5				9	5
15	20X31A0415			5		5				9	5
16	20X31A0416			4		4				8	5
17	20X31A0417			5		5				9	5
19	20X31A0418							5		4	5
20	20X31A0419			4		4				8	5
21	20X31A0420			3		4				8	5
22	20X31A0421			4		4				8	5
23	20X31A0422			5		4				8	5
24	20X31A0423			5		4				8	5
25	20X31A0424			4		5				8	5
26	20X31A0425			5		5				8	5
27	20X31A0426			4		5				8	5
28	20X31A0427			4		4				8	5
29	20X31A0428			4		5				7	5
30	20X31A0429			3		5				8	5
31	20X31A0430			5		5				9	5
32	20X31A0431			3		5				8	5
33	20X31A0432			5		5				9	5
34	20X31A0433	4								5	5
35	20X31A0434			5		5				9	5
36	20X31A0435			3		5				9	5
37	20X31A0436			4		4				7	5
38	20X31A0437			5		5				9	5
39	20X31A0438			5		5				9	5
40	20X31A0439			5		5				9	5
41	20X31A0440			4		5				8	5
42	20X31A0441			5		4				9	5
43	20X31A0442			5		5				9	5
44	20X31A0444			5		5				9	5
45	20X31A0445			4		5				8	5

Percentage of students scored more than target	3		100%		100%		33%		88%	100%
	33%									
CO Mapping with Exam	33%		1				1			
							I		1	
CO - 1	,									ļ!
CO - 1 CO - 2										
CO - 2							Y		Y	Y
CO - 2 CO - 3	Y		Y				Y		Y Y	Y
CO - 2 CO - 3 CO - 4	Y		Y		Y		Y			
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6	Y								Y Y	Y Y
CO - 2 CO - 3 CO - 4 CO - 5	Y		Y 100%		Y 100%		Y 33%		Y	Y
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6									Y Y	Y Y
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6									Y Y	Y Y
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored									Y Y	Y Y
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on									Y Y	Y Y
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2									Y Y	Y Y
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on									Y Y	Y Y
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3							33%		Y Y 88%	Y Y
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3 CO - 4	33%		100%						Y Y 88%	100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3 CO - 4 CO - 5					100%		33%		88% 88% 88%	100% 100% 100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3 CO - 4	33%		100%				33%		Y Y 88%	100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6	33%		100%		100%		33%		88% 88% 88% 88%	100% 100% 100% 100% 100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 CO - 6	33%	obj	100%	Ov	100%	Le	33%	Att	88% 88% 88% 88%	100% 100% 100% 100% 100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6	33%	obj	100%	Ov	100%	Le	33%	Atta	88% 88% 88% 88%	100% 100% 100% 100% 100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 CO - 6	33%	obj	100%	Ov	100%	Le	33%	Atta	88% 88% 88% 88%	100% 100% 100% 100% 100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 CO - 6	33%	obj	100%	Ov	100%	Le	33%	Atta	88% 88% 88% 88% ainment I 1 2	100% 100% 100% 100% 100% 100% 100% 100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 CO CO - 1 CO - 2 CO - 3	33%		100% 100% Asgn		100% 100% verall		33% 33% evel	Atta	88% 88% 88% 88%	100% 100% 100% 100% 100% 100% 100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 CO CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6	33% 33% Subj	88%	100% 100% Asgn	9	100% 100% verall		33%	Atta	88% 88% 88% 88% ainment I 1 2	100% 100% 100% 100% 100% 100% 100% 100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 CO CO - 1 CO - 2 CO - 3	33%		100% 100% Asgn	9	100% 100% verall	3.	33% 33% evel	Atta	88% 88% 88% 88% ainment I 1 2	100% 100% 100% 100% 100% 100% 100% 100%
CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 % Students Scored CO Attainment based on CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6 CO CO - 1 CO - 2 CO - 3 CO - 4 CO - 5 CO - 6	33% 33% Subj	88%	100% 100% Asgn	9	100% 100% verall	3.	33% 33% evel	Atta	88% 88% 88% 88% ainment I 1 2	100% 100% 100% 100% 100% 100% 100% 100%



Department of Electronics and Communication Engineering Course Outcome Attainment (University Examinations)

Name of the faculty: A.VAANI A.Y: 2022-2023

Branch & Section: ECE - A Year / Semester: III-II

Course Name: ESD

Course Name:		ESD			
S.No	Roll Number	Marks Secured			
1	20X31A0401	42			
2	20X31A0402	35			
3	20X31A0403	-1			
4	20X31A0404	51			
5	20X31A0405	41			
6	20X31A0406	41			
7	20X31A0407	40			
8	20X31A0408	30			
9	20X31A0409	41			
10	20X31A0410	10			
11	20X31A0411	28			
12	20X31A0412	1			
13	20X31A0413	27			
14	20X31A0414	43			
15	20X31A0415	48			
16	20X31A0416	20			
17	20X31A0417	40			
18	20X31A0418	-1			

S.No	Roll Number	Marks Secured
36	20X31A0436	9
37	20X31A0437	29
38	20X31A0438	36
39	20X31A0439	44
40	20X31A0440	26
41	20X31A0441	26
42	20X31A0442	47
43	20X31A0444	40
44	20X31A0445	15
45	20X31A0446	26
46	20X31A0447	29
47	20X31A0448	26
48	20X31A0449	36
49	20X31A0450	9
50	20X31A0451	34
51	20X31A0452	42
52	20X31A0453	30
53	20X31A0454	-1

		-	_
19	20X31A0419	33	
20	20X31A0420	32	
21	20X31A0421	39	
22	20X31A0422	44	
23	20X31A0423	11	
24	20X31A0424	35	
25	20X31A0425	42	
26	20X31A0426	33	
27	20X31A0427	31	
28	20X31A0428	36	
29	20X31A0429	35	
30	20X31A0430	27	
31	20X31A0431	18	
32	20X31A0432	35	
33	20X31A0433	21	
34	20X31A0434	46	
35	20X31A0435	27	
Max Ma	Ī		
Class A	verage mark		31
		med above the target	35
Number	of successful stud	ents	60

54	20X31A0455	36
55	20X31A0456	26
56	20X31A0458	31
57	20X31A0459	46
58	20X31A0460	32
59	20X31A0461	34
60	20X31A0462	42

Attainment level	2
Percentage of students scored more than target	58%
Number of successful students	60
Number of students performed above the target	35
Class Average mark	31
IVIAA IVIAIKS	

31	Attainment Level				
35	1	40%			
60	2	50%			
58%	3	60%			
2					



Department of Electronics and Communication Engineering

Course Outcome Attainment

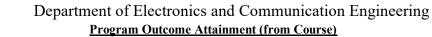
Name of the faculty: A.VAANI Academic Year: 2022-2023

Branch & Section: ECE - A Year: III
Course Name: ESD Semester: II

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00		3.00	2.00	2.25
CO2	3.00		3.00	2.00	2.25
CO3	3.00		3.00	2.00	2.25
CO4		3.00	3.00	2.00	2.25
CO5		3.00	3.00	2.00	2.25
CO6		3.00	3.00	2.00	2.25
Inter	Internal & University Attainment:			2.00	
Weightage			25%	75%	
CO Attainment for the	ernal, University)	0.75	1.50	1	
CO Attainment for	Direct Method)		2.25		

Overall course attainment level

2.25



Name of Faculty: A.VAANI Academic Year: 2022-2023

Branch & Section: ECE - A Year: III
Course Name: ESD Semester: II

CO-PO mapping

PO /CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C324.1	2	-	2	-	-	-	ı	-	-	-	-	-	3	2
C324.2	2	-	3	-	-	-	ı	-	-	-	2	-	2	3
C324.3	2	-	2	-	-	-	ı	-	-	-	-	2	3	2
C324.4	3	-	3	-	-	-	ı	-	-	-	3	-	2	3
C324.5	2	-	2	-	-	-	ı	-	-	-	-	2	2	3
C324.6	2	-	3	-	-	-	ı	-	-	-	-	3	3	2
AVG	2.17	-	2.5	-	-	-	-	-	-	-	2.5	2.3	2.5	2.5

со	Course Outcome Attainment	
CO1	2.25	
CO2	2.25	
CO3	2.25	
CO4	2.25	
CO5	2.25	
CO6	2.25	

Overall course attainment level 2.25

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainmen t	2	2	3	2							2.3	2.3	1.67	1.25

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)