Sri Indu Institute of Engineering & Technology

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COURSE FILE

ON

LOW POWER VLSI DESIGN

Course Code – EC823PE

IV B.Tech II-SEMESTER

A.Y.: 2022-2023

Prepared by

Mr. M. GANESH
Assistant Professor

Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year	2022-2023
Course Title	LOW POWER VLSI DESIGN
Course Code	EC823PE
Programme	B.Tech
Year & Semester	IV year II-semester
Branch & Section	ECE-A
Regulation	R18
Course Faculty	Mr. M GANESH, Assistant Professor

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INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To Continuous assess of teaching-learning process through institute-industry collaboration.

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.

IM4: To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

DM1: To facilitate an academic environment that enables student's centric learning.

DM2: To provide state-of-the-art hardware and software technologies to meet industry requirements.

DM3: To continuously update the Academic and Research infrastructure.

DM4: To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

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PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

PEO1: Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.

PEO2: Graduates with ability to execute innovative ideas for Research and Development with continuous learning.

PEO3: Graduates inculcated with industry based soft-skills to enable employability.

PEO4: Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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PROGRAM OUTCOMES

1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

6. **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE STRUCTURE & SYLLABUS (R18)

Applicable From 2018-19 Admitted Batch

IV YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC701PC	Microwave and Optical Communications	3	0	0	3
2		Professional Elective – III	3	0	0	3
3		Professional Elective – IV	3	0	0	3
4		Open Elective - II	3	0	0	3
5	SM702MS	Professional Practice, Law & Ethics	2	0	0	2
6	EC703PC	Microwave and Optical Communications Lab	0	0	2	1
7	EC704PC	Industrial Oriented Mini Project/ Summer Internship	0	0	0	2*
8	EC705PC	Seminar	0	0	2	1
9	EC706PC	Project Stage - I	0	0	6	3
		Total Credits	**14**	**0**	**10**	**21**

IV YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1		Professional Elective – V	3	0	0	3
2	EC823PE	Professional Elective – VI	3	0	0	3
3		Open Elective - III	3	0	0	3
4	EC801PC	Project Stage - II	0	0	14	7
		Total Credits	**9**	**0**	**14**	**16**

Note: Industrial Oriented Mini Project/ Summer Internship is to be carried out during the summer vacation between 6th and 7th semesters. Students should submit report of Industrial Oriented Mini Project/ Summer Internship for evaluation.

Professional Elective – V

EC811PE	Satellite Communications
EC812PE	Radar Systems
EC813PE	Wireless Sensor Networks

Professional Elective – VI

EC821PE	System on Chip Architecture
EC822PE	Test and Testability
EC823PE	Low Power VLSI Design

EC823PE: LOW POWER VLSI DESIGN (PE – VI)

B.Tech. IV Year II Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

Prerequisite: VLSI Design

Course Objectives:

- Known the low power low voltage VLSI design
- Understand the impact of power on system performances.
- Known about different Design approaches.
- Identify suitable techniques to reduce power dissipation in combinational and sequential circuits.

Course Outcomes: Upon completing this course, the student will be able to

- Understand the need of Low power circuit design.
- Attain the knowledge of architectural approaches.
- Analyze and design Low-Voltage Low-Power combinational circuits.
- Known the design of Low-Voltage Low-Power Memories

UNIT - I:

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT - II:

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, and Mask level Measures.

UNIT - III:

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low- Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low- Voltage Low-Power Logic Styles.

UNIT - IV:

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT - V:

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
3. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
4. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, Anatha Chandrakasan, Springer, 2005.

COURSE : LOW POWER VLSI DESIGN (C422)

CLASS: IV- ECE A

Course Outcomes:

After completing this course the student will be able to:

C422.1: Able to carry out research and development in the area of Low Power VLSI circuits. (Analysis)

C422.2: Apply techniques to improve power consumption of VLSI circuits. (Knowledge and Analysis)

C422.3: Utilize logic simulation methods to design Low Power VLSI circuits (Knowledge)

C422.4: Apply logic-level, architecture-level and system-level techniques in various designs to optimize power consumption of the VLSI circuits (Analysis)

C422.5: Known the design of Low-Voltage Low-Power Memories (Knowledge and Analysis)

C422.6: Implement practical and state of the art Low Power VLSI design, suitable for real life and Industry applications. (Evaluation)

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C422.1	3	3	3	2	-	-	-	-	-	-	-	3	2	2
C422.2	3	3	3	2	-	-	-	-	-	-	-	3	2	2
C422.3	3	-	3	2	-	-	-	-	-	-	-	3	2	2
C422.4	3	-	-	3	-	-	-	-	-	-	-	3	2	2
C422.5	3	-	3	3	-	-	-	-	-	-	-	3	3	3
C422.6	3	-	3	3	-	-	-	-	-	-	-	3	2	2
C422	3	3	3	2.5	-	-	-	-	-	-	-	3	2.16	2.16

CO-PO mapping Justification

PO1.	**ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2.	**PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3.	**DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations
PO4.	**CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions
PO12.	**LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.
PSO 1	**Design Skills:** Design, analysis and development a economical system in the area of Embedded system & VLSI design.
PSO 2	**Software Usage:** Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

C422.1: Able to carry out research and development in the area of Low Power VLSI circuits. (Analysis)

	Justification
PO1	Students get the knowledge on area of Low Power VLSI circuits (level 3)
PO2	Students solve & analyze the complex vlsi circuits (level 3)
PO3	Students can Implement and design the practical low power vlsi circuits(level 3)
PO4	Students can do research based experiments in low power vlsi (level 2)
PO12	Students can learn the need of low power circuit design (level 3)
PSO1	By combining your design, analysis, and development skills with a focus on economical systems in Embedded Systems and VLSI design, you are well-equipped to engage in research and development in the area of Low Power VLSI circuits. (level 2)
PSO2	MATLAB is particularly useful for algorithm development and signal processing, which are critical aspects of low power design. (level 2)

C422.2: Apply techniques to improve power consumption of VLSI circuits. (Knowledge and Analysis)

	Justification
PO1	Gain the knowledge to improve the power consumption of vlsi circuits (level 3)
PO2	Students solve & analyze the complex problems on power consumption of VLSI circuits (level 3)
PO3	Able to design the circuits to reduce the overall power consumption (level 3)
PO4	Applying the techniques and methodologies to reduce the overall static and dynamic power (level 2)
PO12	Students can learn the different power consumption techniques of vlsi circuits(level 3)
PSO1	Your ability to develop economical systems is directly applicable to the practical aspects of optimizing power consumption. (level 2)
PSO2	your proficiency in software tools such as MATLAB, Keil, and Xilinx provides a strong foundation for applying techniques to improve the power consumption of VLSI circuits. (level 2)

C422.3: Utilize logic simulation methods to design Low Power VLSI circuits (Knowledge)

	Justification
PO1	Students get the knowledge of simulation methods to design Low Power VLSI circuits(level 3)
PO3	Students can able to design and develop the low power vlsi circuits (level 3)
PO4	Students can use research based methods to design low power CMOS Adders(level 2)
PO12	Students can clearly understand the different types CMOS adders (level 3)
PSO1	The utilization of logic simulation methods in designing Low Power VLSI circuits is well-justified by the Design Skills outlined in the provided PSO. (level 2)
PSO2	Xilinx tools are essential for FPGA development, and FPGA-based solutions play a significant role in VLSI design. Proficiency in Xilinx tools allows for hardware-level simulation and investigation of power-related issues. (level 2)

C422.4: Apply logic-level, architecture-level and system-level techniques in various designs to Optimize power consumption of the VLSI circuits. (Analysis)

	Justification
PO1	Students get the knowledge of low voltage low power (level 3)
PO4	Students can use the research based methods to design the low voltage low power multipliers (level 3)
PO12	Students acquire continuous knowledge about low power multipliers (level 3)
PSO1	The application of logic-level, architecture-level, and system-level techniques to optimize power consumption in VLSI circuits is well-justified by the specified Design Skills related to designing economical systems in the area of Embedded Systems and VLSI design. (level 2)
PSO2	The combination of MATLAB, Keil, and Xilinx represents a comprehensive set of software tools that covers the entire spectrum of VLSI design, from algorithmic considerations to low-level software development and hardware implementation. (level 2)

C422.5: Known the design of Low-Voltage Low-Power Memories. (Knowledge and Analysis)

	Justification
PO1	Students get the knowledge of Low-Voltage Low-Power Memories (level 3)
PO3	Students can able to design and develop the memory cells, RAM,AOM (level 3)
PO4	Students can use the research based methods on low power memories(level 3)
PO11	The knowledge of designing Low-Voltage Low-Power Memories aligns well with the specified PO related to Project Management and Finance.
PO12	Students can gain the knowledge on types of memory cells ,RAM,ROM. (level 3)
PSO1	Memories are integral components in embedded systems, and their design significantly impacts the overall system's efficiency. (level 3)
PSO2	The combination of MATLAB, Keil, and Xilinx represents a comprehensive set of software tools covering different aspects of memory design, from algorithmic considerations to low-level software and hardware development. (level 3)

C422.6: Implement practical and state of the art Low Power VLSI design, suitable for real life and Industry applications. (Evaluation)

	Justification
PO1	Get the knowledge of Need for Low Power VLSI design (level 3)
PO3	Students can able to design and develop the low power vlsi circuits (level 3)
PO4	Students can use the research based methods on low power CMOS circuits(level 3)
PO12	Students can gain the knowledge on low power consumption(level 3)
PSO1	Implementing practical and state-of-the-art Low Power VLSI design, suitable for real-life and industry applications, aligns perfectly with the specified PSO related to Design Skills. (level 2)
PSO2	The ability to implement practical and state-of-the-art Low Power VLSI design, suitable for real-life and industry applications, is well-justified by the specified PSO related to Software Usage. (level2)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

ACADEMIC CALENDAR 2022-23

B. Tech./B. Pharm. IV YEAR I & II SEMESTERS

I SEM

S. No	Description	Duration	
		From	To
1	Commencement of I Semester classwork	**29.08.2022**	
2	1st Spell of Instructions (including Dussehra Recess)	29.08.2022	31.10.2022 (9 Weeks)
3	Dussehra Recess	03.10.2022	08.10.2022 (1 Week)
4	First Mid Term Examinations	01.11.2022	07.11.2022 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	12.11.2022	
6	2nd Spell of Instructions	09.11.2022	03.01.2023 (8 Weeks)
7	Second Mid Term Examinations	04.01.2023	10.01.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	11.01.2023	19.01.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	17.01.2023	
10	End Semester Examinations	*20.01.2023*	02.02.2023(2 Weeks)

Note: No. of Working/instructional days: 94

II SEM

S. No	Description	Duration	
		From	To
1	Commencement of II Semester classwork	**03.02.2023**	
2	1st Spell of Instructions	03.02.2023	31.03.2023 (8 Weeks)
3	First Mid Term Examinations	01.04.2023	08.04.2023 (1 Week)
4	Submission of First Mid Term Exam Marks to the University on or before	15.04.2023	
5	2nd Spell of Instructions	10.04.2023	17.06.2023 (10 Weeks)
6	**Summer Vacation**	15.05.2023	27.05.2023 (2 Weeks)
7	Second Mid Term Examinations	19.06.2023	24.06.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	26.06.2023	01.07.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	01.07.2023	
10	End Semester Examinations	03.07.2023	15.07.2023 (2 Weeks)

Note: No. of Working/ instructional days: 91

REGISTRAR

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

UGC Autonomous, Accredited by NAAC A+ Grade, Recognized under 2(f) of UGC Act 1956.
(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana – 501 510
https://siiet.ac.in/

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Class Timetable

CLASS: IV-B.Tech ECE-A **A.Y:2022-23** **SEMESTER: II** **LH: B-205**

TIME/ DAY	I 9:40-10:30	II 10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00-1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON	LPVLSID	ML	ML	COUN	LUNCH	WSN	ML	INT
TUE	WSN	LPVLSID	CO-CU/DAA			ML	WSN	LIB
WED	LPVLSID	ML	WSN	ML		WSN	LPVLSID	SPORTS
THU	LPVLSID	WSN	ML	WSN		ML	LPVLSID	LPVLSID
FRI	PROJECT STAGE-II					PROJECT STAGE-II		
SAT	PROJECT STAGE-II					PROJECT STAGE-II		

*(T) – Tutorial Concern Faculty

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the Faculty
EC813PE	WSN-Wireless Sensor Networks (Professional Elective-V)	Dr.S.Anjaneyulu	COUN	Counseling	M.Ganesh/K.Rajender/P.Kavitha
EC823PE	LPVLSID-Low Power VLSI Design (Professional Elective-VI)	M.Ganesh	SPORTS	Sports	P.Srilatha/S.Naresh
CS800OE	ML-Machine Learning (Open Elective-III)	G.Swapna	CO-CU/ DAA	Co-Curricular/ Dept.Assoc.Activities	Y.Raju/B.Jyothirmai/K.Bhaskar Reddy
EC801PC	PROJECT STAGE-II	A.Sindhuja/ K.Mallaiah Dr.K.Srinivasa Reddy/ Dr.D.Lakshmaiah	LIB	Library	K.Padma
			INT	Internet	K.Bhaskar Reddy

Class Incharge

Head of the Department
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Principal
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LESSON PLAN

Programme: B.Tech	Academic Year: 2022-23
Year: IV	Semester: II
Course Title: LOW POWER VLSI DESIGN	Course Code: EC823PE
Name of Faculty: M GANESH	

Unit-I Syllabus

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching PowerDissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation,Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	**Fundamentals:** Need for Low Power Circuit Design	T2, R 1	BB
1	Sources of Power Dissipation	T2, R 1	BB
1	Switching PowerDissipation,	T2, R 2	BB
1	Short Circuit Power Dissipation	T2, R 2	BB
1	Leakage Power Dissipation	T1, R2	BB
1	Glitching Power Dissipation	T1, R2	BB
1	Short Channel Effects	T1	BB
2	Drain Induced Barrier Lowering and Punch Through	T1, R1	BB
2	Surface Scattering	T1, R1	BB
1	Velocity Saturation	T1	BB
2	Impact Ionization	T1	BB
1	Hot Electron Effect.	T1, R2	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Able to carry out research and development in the area of Low Power VLSI circuits.(Analysis)			

*Session Duration: 50 minutes

*Total Number of Hours/Unit: 15

Unit-II Syllabus:

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures,and Mask level Measures.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
2	**Low-Power Design Approaches**	T1, R 2	BB
2	Low-Power Design through Voltage Scaling	T2,R 2	BB
1	VTCMOS circuits	T2,R 2	BB
1	MTCMOS circuits	T2,R 1	BB
1	Architectural Level Approach	T2	BB
1	Pipelining and Parallel Processing Approaches	T2,R1	BB
2	**Switched Capacitance Minimization Approaches**	T2,R2	BB
1	System Le Circuit Level Measures	T1	BB
1	Circuit Level Measures	T2	BB
1	Mask level Measures	T1, R 2	BB
Gap beyond syllabus (if any):			
Gap within the syllabus (if any)			
Course Outcome 1 Apply techniques to improve power consumption of VLSI circuits. (Knowledge and Analysis)			

*Session Duration: 50 minutes

*Total Number of Hours/Unit: 13

Unit-III Syllabus:

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low- Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low- Voltage Low-Power Logic Styles.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	**Low-Voltage Low-Power Adders**	T1,R1	BB
2	Introduction, Standard Adder Cells	T1	BB
2	CMOS Adder's Architectures Ripple Carry Adders	T1, R 1	BB
2	Carry Look- Ahead Adders	T1, R 1	BB
2	Carry Select Adders	T1, R 1	BB
1	Carry Save Adders	T1, R 2	BB
1	Low- Voltage Low-Power Design Techniques	T1, R 1	BB
2	Trends of Technology and Power Supply Voltage	T1, R2	BB
1	Low- Voltage Low-Power Logic Styles.	R1	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome: : Utilize logic simulation methods to design Low Power VLSI circuits (Knowledge)			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 14

Unit-IV Syllabus

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace TreeMultiplier.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
2	**Low-Voltage Low-Power Multipliers**	T2,R2	BB
1	Introduction, Overview of Multiplication	R2	BB
2	Types of Multiplier Architectures	T2,R1	BB
1	Braun Multiplier	T2, R2	BB
2	Baugh- Wooley Multiplier	T2, R 1	BB
2	Booth Multiplier	T2	BB
2	Introduction to Wallace TreeMultiplier.	T2	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome: Apply logic-level, architecture-level and system-level techniques in various designs to optimize power consumption of the VLSI circuits (Analysis)			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 12

Unit-V Syllabus

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
2	**Low-Voltage Low-Power Memories**	T2,R2	BB
1	Basics of ROM, Low-Power ROM Technology	T2,R2	BB
1	Future Trend andDevelopment of ROMs	T2	BB
1	Basics of SRAM, Memory Cell	T1, R 1	BB
2	Precharge and Equalization Circuit	T1, R 1	BB
2	Low-PowerSRAM Technologies	T1	BB
1	Basics of DRAM	T2	BB
1	Self-Refresh Circuit	T1, R 1	BB
2	Future Trend and Development of DRAM.	T2, R 1	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: : Known the design of Low-Voltage Low-Power Memories (Knowledge and Analysis) **Course Outcome 2:** Implement practical and state of the art Low Power VLSI design, suitable for real life and Industry applications. (Evaluation)			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 13

Text Books	
Text 1	CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
Text 2	Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering

Reference Books	
Ref 1	Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
Ref 2	Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
Ref 3	Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
Ref 4	Leakage in Nanometer CMOS Technologies – Siva G. Narendran, Anatha Chandrakasan, Springer, 2005.

WEB REFERENCES:

Websites	
W1	https://www.physicaldesign4u.com/2020/01/sources-of-power-dissipation-in-cmos.html
W2	http://www.faadooengineers.com/online-study/post/ece/vlsi-design/1829/variable-threshold-cmos-vtcmos-circuits
W3	https://www.ece.uvic.ca/~fayez/courses/ceng465/lab_465/project1/adders.pdf
W4	https://www.electronics-notes.com/articles/electronic_components/semiconductor-ic-memory/dynamic-ram-how-does-dram-work-operation.php
W5	https://ikarthikmb.github.io/wallace-tree/

Lecture notes

Unit 1 link:

https://drive.google.com/file/d/1EOn2dbK97jZrwzgIae8XVGIa9jazua6x/view?usp=sharing

Unit 2 link:

https://drive.google.com/file/d/1bU44ws7cIUdSuUwaIQnrnbM7zcCfLzoF/view?usp=sharing

Unit 3 link:

https://drive.google.com/file/d/1ICBRdgcFM9ehjicookfdaCPElWN8gter/view?usp=sharing

Unit 4 link:

https://drive.google.com/file/d/1txCr34lUwJ9b5C7Wkanqx4mJLo-IU3Ir/view?usp=sharing

Unit 5 link:

https://drive.google.com/file/d/15qmXx9e15eYLNyLBU1os1ClUSl2UCsL1/view?usp=sharing

Power point presentation

PPT link:

https://drive.google.com/file/d/1LDa-bqPkRPXmHhReRlipFe9W-AAPooTq/view?usp=sharing

Code No: 158BH **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, July/August - 2022
LOW POWER VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max.Marks:75**

Answer any five questions
All questions carry equal marks
- - -

1. a) Discuss the need of a low power designs in VLSI circuits.
   b) Derive the equation for threshold voltage of a MOSFET and discuss the factors involved in it.
   c) Explain how the V_{th} and V_{dd} influences the power dissipation. [5+5+5]

2. Discuss with a suitable figure (i) Switching Power Dissipation (ii) Short Circuit Power Dissipation (iii) Glitching Power Dissipation. [15]

3. Discuss the two basic architectural level measures to reduce the power in VLSI circuits and explain with suitable examples. [15]

4. Discuss about power reduction by
   a) One hot coding b) CG granularity. [8+7]

5.a) Write down the differences between carry select adders and carry save adders.
   b) Discuss two types of low voltage low power logic styles with suitable examples. [5+10]

6.a) Draw the logic circuit of the conventional CMOS full adder and explain about it.
   b) Explain the basic theory, operation and performance evaluation of carry look-ahead Adder. [7+8]

7.a) Discuss the types of multiplier architectures and compare them.
   b) Explain about Booth multiplier with neat architectures. [5+10]

8.a) Write down differences between 6T and 4T static RAM cells.
   b) With a neat diagram, explain the block diagram of DRAM architecture. [6+9]

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Code No: 158BH **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, September - 2022
LOW POWER VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max.Marks:75**

Answer any five questions
All questions carry equal marks
- - -

1. What are the different sources of power dissipation in VLSI circuits and explain them in detail? [15]

2.a) Describe about short channel effect.
b) What is hot electron effect in low power VLSI design?
c) What is velocity saturation in MOS FET? [5+5+5]

3.a) How VTCMOS circuits reduce efficiently the overall power dissipation?
b) Compare the VTCMOS and MTCMOS circuits. [9+6]

4.a) Explain any one method of minimizing the switched capacitance at circuit level measure.
b) Explain how a simple mask level measures reduce power dissipation and parasitic capacitance? [8+7]

5.a) Design a standard adder circuit and modify it for low power and low voltage .
b) Draw the architecture of low voltage low power carry save adder and explain its working with truth table. [6+9]

6. What are the different low power, low voltage logic styles and explain them with some examples. [15]

7.a) Design a Braun multiplier and what modifications are required to use in low power VLSI circuits
b) What are advantages and limitations of Wallace tree multiplier with respect to low power VLSI design? [10+5]

8.a) Draw the 6T static RAM structure and explain how it stores the data.
b) Why Refresh circuit is needed in DRAM and draw such a circuit and explain its working. [7+8]

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SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Shereguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 **Set – I**

I - Mid Examinations, May -2023

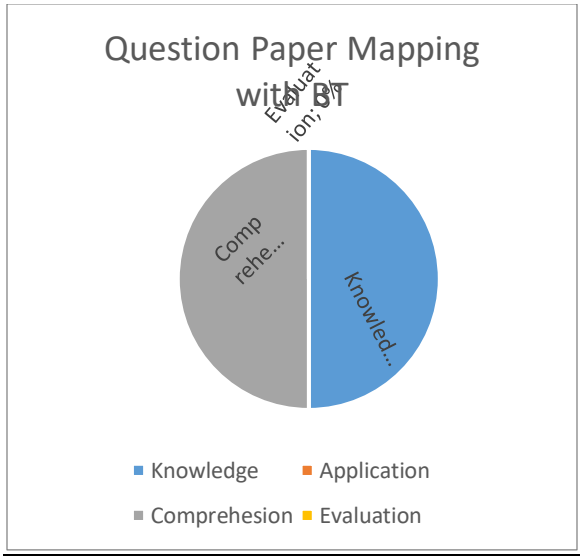
Year &Branch: IV ECE-A,B&C Date:08 -05-2023

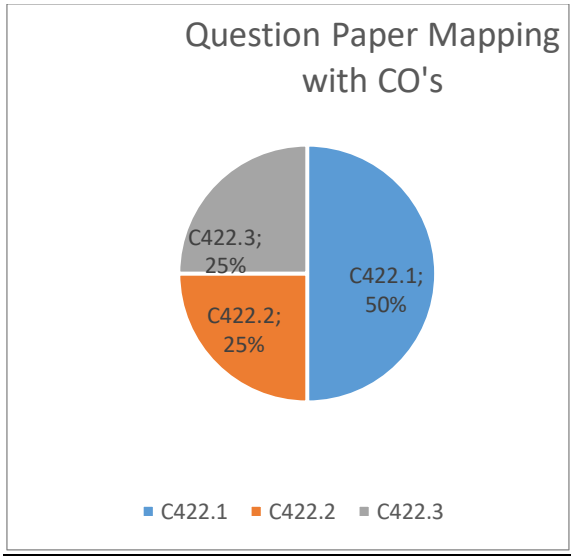
Subject: LPVLSID Max. Marks: 10 Time: 60 mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

1	Write short notes on need for low power circuit design	(5)	C422.1	(Knowledge)
2.	Explain the switching power dissipation	(5)	C422.1	(Comprehension)
3	Explain the operation of Multiple threshold CMOS (MTCMOS)?	(5)	C422.2	(Comprehension)
4	What are the standard adder cells, and describe the Half Adder with diagram?	(5)	C422.3	(Knowledge)





SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Shereguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 **Set – I**

II - Mid Examinations, June -2023

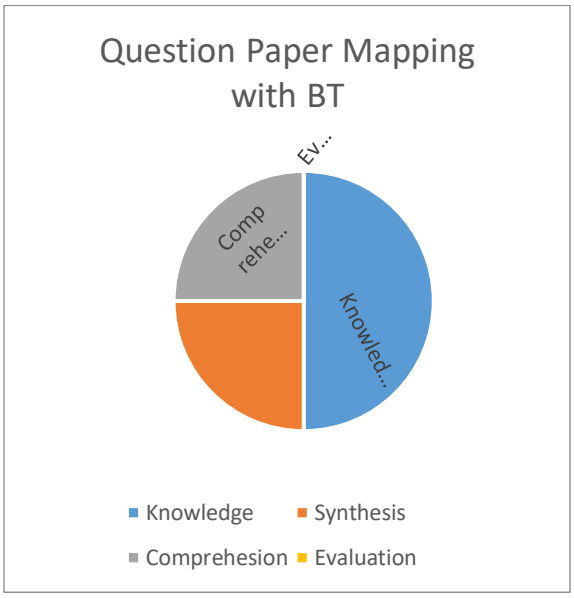
Year &Branch: IV ECE-A,B&C Date: 19-06-2023 (AN)

Subject: LPVLSID Max. Marks: 10 Time: 60 mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

1	Design the different logic styles of XOR/XNOR gate.	(5)	C422.3	(Synthesis)
2	Draw the structure of Booth Encoder and Explain it	(5)	C422.4	(Knowledge)
3	Explain different types of Multiplier architectures	(5)	C422.4	(Comprehension)
4	Write about the future trend and development of ROM	(5)	C422.5	(Knowledge)



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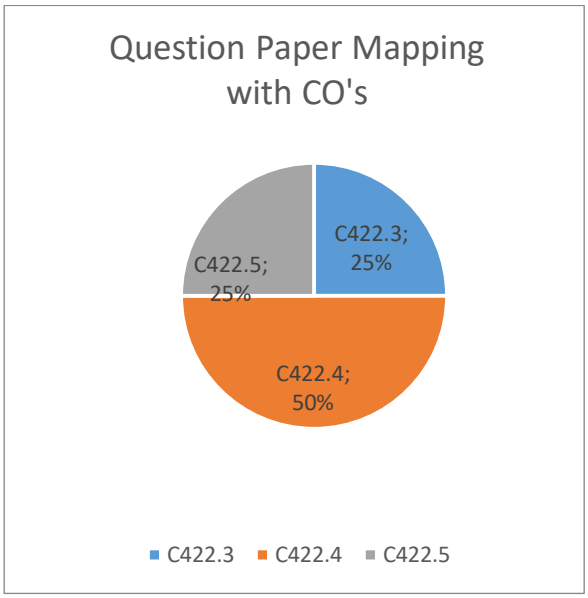

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ECE

B.Tech IV Year II Sem I Mid –Term Examination, May-2023

LPVLSI Design

(Objective Exam)

DATE: 08 /05/2023 **TIME: 20 Min** **MAX.MARKS: 10**

NAME : | **ROLL NO:** | **MARKS:**

I. Choose The Correct Alternative:

1. To reduce the overall power dissipation in CMOS logic circuits supply voltage should be [ ]

a) high b) low c) medium d) none

2. High performance microprocessor chips operate at clock frequency in the range of [ ]

a) 100-300 MHZ b) 200-300 MHZ c) 300-400 MHZ d) none

3. The threshold voltage Vt of a MOS transistor is a function of [ ]

a) source-to-substrate voltage b) substrate-to-source voltage c) Source-to-Drain Voltage d) none

4 In CMOS Logic NMOS network is called [ ]

a) Pull-Up b) Pull-down c) both d) none

5. Short channel effects are [ ]

a) Surface scattering b) Velocity saturation c) impact ionization d) all

6. The disadvantage of Parallel processing approach is [ ]

a) increased area b) increased latency c) both d) none

7. Different levels in switched capacitance minimization approaches are [ ]

a) System level b) Circuit level c) Physical design level d) all

8. As the technology developed the channel length was scaled from 1989-2002 is [ ]

a) 0.17µm - 0.13 µm b) 0.27µm - 0.23 µm c) 0.17µm - 0.11 µm d) none

9. As the technology developed the power supply voltage has undergone from 1989-2002 is [ ]

a) 1.5V- 1.2V b) 2V- 1V c) 1.5V- 1V d) none

10. Which type of MOSFET exhibits no current at zero gate voltage [ ]

a) Enhancement mode MOSFET b) Depletion mode MOSFET

c) both d) none

II. Fill in the blanks

11. In conventional CMOS logic circuits, the substrate terminals of all nMOS transistors are connected to _____.

12. In VTCMOS circuit technique, on the other hand, the transistors are designed inherently with a low _____.

13. In CMOS Logic PMOS network is called _____

14. In NMOS & PMOS transistors used in CMOS logic gate have _____reverse leakage and sub threshold currents.

15. Drain –Induced barrier lowering and punch through is _____ effect.

16. What is MTCMOS_____.

17. _____ technique is used to automatically control the threshold voltages.

18. In Pipeline approach the dynamic power consumption of structure is P_{ref}= _____

19. In conventional CMOS logic circuits the substrate terminals of all pMOS transistors are connected to _____

20. Typical power consumption is in between _____

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ECE

B.Tech IV Year II Sem II Mid –Term Examination, June-2023

LPVLSI Design

(Objective Exam)

DATE: 19 /06/2023 (AN) **TIME: 20 Min** **MAX.MARKS: 10**

NAME : | **ROLL NO:** | **MARKS:**

I. Choose The Correct Alternative:

1. CMOS logic styles have used to implement the low power___ cells [ ]

   a) 8-bit adder cells b) 2-bit adder cells c) 1-bit adder cells d) 4-bit adder cells

2. The 4-T cell consist of ___ NMOS transistors [ ]

   a) 2 b) 4 c) 6 d) 8

3. The mass storage memory is a serial or sequential memory such as found in [ ]

   a) Hard disks b) CD-ROM c) both d) RAM

4. ROM chip architecture contains [ ]

   a) Standard ROM b) Mask –Programmed ROM c) PROM d) all

5. The DRAM access time is [ ]

   a) 60ns b) 100ns c) 10ns d) none

6. The power supply is reduced to ___Volts by year 2016 [ ]

   a) 0.5v b) 0.6v c) 0.7v d) 0.9v

7. CSA stands for [ ]

   a) Carry select adders b) Carry save adders

   b) Complementary save adders d) none

8. The basic unit of Ripple carry adder is [ ]

   a) Full adder b) Half adder c) n-bit adder d) none

9. The hardware implementation of parallel multipliers advances in improved [ ]

a) Accuracy b) Size c) Dynamic range d) none

10. The two main categories of a binary arithmetic multiplication involves they are [ ]

a) Computing unsigned numbers b) Computing signed numbers

c) both d) none

II. Fill in the blanks

11.The final step in the fabrication process of manufacture is called _____

12. Low power techniques at the circuit level is used to determine the _____

13. The hardware implementation of parallel multipliers advances in improved _____ and _____.

14.The main specification of multiplier is _____

15. The serial multiplier uses a _____algorithm.

16. In ROM bank the memory access system includes separate _____ and _____ circuits for each bit lines .

17. Low power high performance SRAM s are usefull in _____ device and high performance processor.

18. _____ method result in reduction of the capacitance AND/OR switching activity of bit and row lines.

19.Multiplication is considered as a series of repeated _____ .

20. In Multiplication of signed numbers, the negative numbers is first converted to its _____ representation

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ECE

B.Tech IV Year II Sem I Mid –Term Examination, May-2023

LPVLSI Design

(Objective Exam) **DATE: 08 /05/2023**

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/17sYTcOVXiwQep0e3uAqwWhiXPiJw6SrZ/view?usp=sharing

Objective/Quiz Key Paper

I. Choose The Correct Alternative:

1. b
2. a
3. a
4. b
5. d
6. c
7. d
8. a
9. a
10. a

II. Fill in the blanks

11. Ground potential
12. Threshold voltage
13. Pull-Up Network
14. Non zero
15. Short channel
16. Multiple Threshold CMOS
17. VTCMOS
18. $C_{total}.V_{DD}^2.f_{clk}$
19. V_{DD}
20. 20-50W

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ECE

B.Tech IV Year II Sem II Mid –Term Examination, June-2023

LPVLSI Design

(Objective Exam)

DATE: 19 /06/2023 (AN)

Descriptive paper key link:

https://drive.google.com/file/d/1vY5Ls1SLhrFdbeQ21tW4HoY8tIIk39wI/view?usp=sharing

Objective/Quiz Key Paper

I. Choose The Correct Alternative:

1. c
2. b
3. c
4. d
5. a
6. b
7. b
8. a
9. b
10. c

II. Fill in the blanks

11. Mask programming

12. Short circuit current

13. Speed, Size

14. Size or Speed

15. Successive addition

16. Pre-Charge and pre-discharge

17. Hand-held

18. Cascade sensing or Difference Encoding

19. Additions

20. 2's Complement

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Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

ASSIGNMENT- 1 SUBJECT: LOW POWER VLSI DESIGN

1	What are the sources of power dissipation, and explain the switching power dissipation	C422.1	(Comprehension)
2	Define what is Architectural level approach, and Explain about pipeline approach?	C422.3	(Knowledge)
3	Write notes on what are the trends of technology?	C422.2	(Knowledge)
4	Write about leakage power dissipation	C422.1	(Knowledge)
5	Explain the switching power dissipation	C422.2	(Comprehension)
6	Write short notes on need for low power circuit design	C422.1	(Knowledge)
7	Explain the operation of Multiple threshold CMOS (MTCMOS)?	C422.1	(Knowledge)
8	What are the standard adder cells, and describe the Half Adder with diagram?	C422.3	(Knowledge)

ASSIGNMENT- 2 SUBJECT: LOW POWER VLSI DESIGN

1	Design the different logic styles of XOR/XNOR gate.	(5)	C422.3	(Synthesis)
2.	Draw the structure of Booth Encoder and Explain it	(5)	C422.4	(Knowledge)
3	Explain different types of Multiplier architectures	(5)	C422.4	(Comprehension)
4	Write about the future trend and development of ROM	(5)	C422.5	(Knowledge)
5	Differentiate the different types of SRAM Memory cells and note down its limitations.	(5)	C422.5	(Analysis)
6	Explain the Architecture of Braun Multiplier	(5)	C422.4	(Comprehension)
7	Explain the design techniques for low power circuit development.	(5)	C422.5	Comprehension)

Course Title	LOW POWER VLSI DESIGN
Course Code	EC823PE
Programme	B.Tech
Year & Semester	IV year II-semester, A sec
Regulation	R18
Course Faculty	M GANESH, Assistant Professor, ECE

Slow learners:

S No	Roll no	No of backlogs	Internal-I Status	Internal-II Status
1	19X31A0404	3	22	22
2	19X31A0410	4	21	21
3	19X31A0412	3	19	23
4	19X31A0416	4	19	21
5	19X31A0417	4	17	23
6	19X31A0423	4	17	21
7	19X31A0424	4	20	21
8	19X31A0428	4	19	20
9	19X31A0441	3	20	21
10	19X31A0448	3	14	17

Advanced learners:

S.NO	ROLL.NO.	Assigned work
1	19X31A0401	Advanced concepts material is provided for advanced learners, subject seminars are presented by advanced learners in the class, and advanced learners are encouraged to support slow learners
2	19X31A0403	
3	19X31A0407	
4	19X31A0408	
5	19X31A0411	
6	19X31A0413	
7	19X31A0414	
8	19X31A0420	
9	19X31A0421	
10	19X31A0422	
11	19X31A0427	
12	19X31A0429	
13	19X31A0430	
14	19X31A0431	
15	19X31A0435	
16	19X31A0437	
17	19X31A0440	
18	19X31A0442	
19	19X31A0443	
20	19X31A0444	
21	19X31A0446	
22	19X31A0447	
23	19X31A0450	
24	20X35A0402	
25	20X35A0403	
26	20X35A0404	

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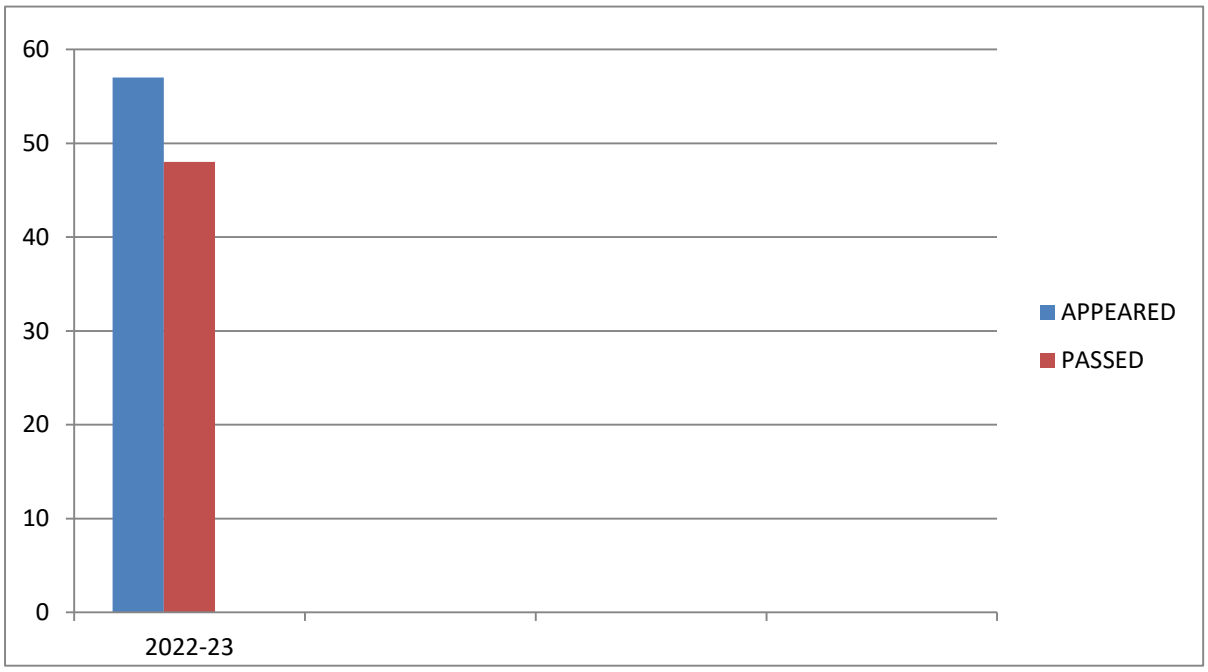
Website: https://siiet.ac.in/

B.TECH III – I-ECE -A RESULT ANALYSIS

ACADAMIC YEAR	COURSE NAME	NUMBER OF STUDENTS		QUESTION PAPER SETTING		PASS%
		APPEARED	PASSED	INTERNAL	EXTERNAL	
2022-23	LOW POWER VLSI DESIGN	57	48	COURSE FACULTY	JNTUH	84.21

LOW POWER VLSI DESIGN (422) RESULT ANALYSIS



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Website: https://siiet.ac.in/

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

REMEDIAL CLASSES TIME TABLE

A.Y 2022-23 **SEMESTER-II**

BRANCH/ SEC	MON 4.00 PM- 5.00 PM	TUE 4.00 PM- 5.00 PM	WED 4.00 PM- 5.00 PM	THUR 4.00 PM- 5.00 PM	FRI 4.00 PM- 5.00 PM
II ECE-A	EMF&W	LTNM	A&DC	LICA	ECA
II ECE-B	LICA	A&DC	EMF&W	ECA	LTNM
III ECE-A	DSP	VLSID	A&P	ESD	IM
III ECE-B	A&P	ESD	DSP	IM	VLSID
III ECE-C	IM	A&P	ESD	VLSID	DSP
IV ECE-A	WSN	ML	LPVLSID	-	-
IV ECE-B	ML	LPVLSID	WSN	-	-
IV ECE-C	LPVLSID	WSN	ML	-	-

HOD
Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL
PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R R Dist Telangana -501 510

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty : M.GANESH Academic Year: 2022-23

Branch & Section: ECE - A Examination: I Internal

Course Name: LOW POWER VLSI DESIGN Year: IV Semester: II

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj1	A1
Max. Marks ==>		5		5		5		5		10	5
1	19X31A0401			5		4				8	5
2	19X31A0402			4		3				8	5
3	19X31A0403	3		4						8	5
4	19X31A0404	4		5						8	5
5	19X31A0405	4		4						8	5
6	19X31A0406	3				4				9	5
7	19X31A0407									5	5
8	19X31A0408	3						5		9	5
9	19X31A0409	3		3						8	5
10	19X31A0410	3		5						8	5
11	19X31A0411	4		4						9	5
12	19X31A0412	1				4				8	5
13	19X31A0413			5		3				8	5
14	19X31A0414			5		3				8	5
15	19X31A0415			4		4				8	5
16	19X31A0416			3		3				8	5
17	19X31A0417			3		2				7	5
18	19X31A0420			5		4				8	5
19	19X31A0421			4		4				9	5
20	19X31A0422			3		4				9	5
21	19X31A0423	2		3						7	5
22	19X31A0424	3				5				7	5
23	19X31A0425	3		4						8	5
24	19X31A0426	3		2						9	5
25	19X31A0427	4		4						9	5
26	19X31A0428	4		1						9	5
27	19X31A0429	5				5				9	5
28	19X31A0430	4		3						9	5
29	19X31A0431	3						5		9	5
30	19X31A0432					3		4		8	5
31	19X31A0433			4						5	5
32	19X31A0434							4		5	5
33	19X31A0435	4		2						7	5
34	19X31A0436	3						4		9	5
35	19X31A0437	3						4		9	5
36	19X31A0438	3				4				9	5
37	19X31A0439					4				5	5
38	19X31A0440	5								9	5
39	19X31A0441					3		3		9	5
40	19X31A0442					5		4		9	5

41	19X31A0443	3		4						10	5
42	19X31A0444	5		5						10	5
43	19X31A0445	4		3						9	5
44	19X31A0446	4				5				8	5
45	19X31A0447			5		5				8	5
46	19X31A0448							4		5	5
47	19X31A0449	3				4				9	5
48	19X31A0450	3				4				9	5
49	20X35A0401	3								7	5
50	20X35A0402					5				9	5
51	20X35A0403					5		5		9	5
52	20X35A0404	3		4						9	5
53	20X35A0405	3		3						9	5
54	20X35A0407	2								8	5
55	20X35A0408									6	5
56	20X35A0409	3				4				9	5
57	20X35A0410	3				2				7	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		32	0	27	0	25	0	10	0	52	57
Number of students attempted		35	0	30	0	27	0	10	0	57	57
Percentage of students scored more than target		91%		90%		93%		100%		91%	100%

CO Mapping with Exam Questions:

CO - 1	Y		Y						Y	Y
CO - 2					Y				Y	Y
CO - 3							Y		Y	Y
CO - 4										
CO - 5										
CO - 6										

% Students Scored >Target %	91%		90%		93%		100%		91%	100%

CO Attainment based on Exam Questions:

CO - 1	91%		90%						91%	100%
CO - 2					93%				91%	100%
CO - 3							100%		91%	100%
CO - 4										
CO - 5										
CO - 6										

CO	**Subj**	obj	Asgn	Overall	Level
CO-1	91%	91%	100%	94%	3.00
CO-2	93%	91%	100%	95%	3.00
CO-3	100%	91%	100%	97%	3.00
CO-4					

Attainment Level	
1	40%
2	50%
3	60%

CO-5					
CO-6					

Attainment (Internal 1 Examination) - **3.00**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-2)

Name of the faculty : M.GANESH Academic Year: 2022-23

Branch & Section: ECE - A Examination: II Internal

Course Name: LOW OWER VLSI DESIGN Year: IV Semester: II

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj4	A4
Max. Marks ==>		5		5		5		5		10	5
1	19X31A0401	5				4				8	5
2	19X31A0402	4		3						8	5
3	19X31A0403			4		5				8	5
4	19X31A0404					4		4		9	5
5	19X31A0405					3		5		9	5
6	19X31A0406			4		5				9	5
7	19X31A0407	5								8	5
8	19X31A0408			5						8	5
9	19X31A0409					3		3		8	5
10	19X31A0410					3		4		8	5
11	19X31A0411	5		3						9	5
12	19X31A0412	3		3						9	5
13	19X31A0413			5						8	5
14	19X31A0414			5		4				9	5
15	19X31A0415			4		5				9	5
16	19X31A0416			4		4				9	5
17	19X31A0417					5		4		8	5
18	19X31A0420	3						5		8	5
19	19X31A0421	4		4						9	5
20	19X31A0422			4		4				9	5
21	19X31A0423			4				4		8	5
22	19X31A0424					4		4		8	5
23	19X31A0425	5				5				9	5
24	19X31A0426	5		4						8	5
25	19X31A0427			5		4				9	5
26	19X31A0428							5		8	5
27	19X31A0429			5				5		9	5
28	19X31A0430	4		5						8	5
29	19X31A0431	5		4						8	5
30	19X31A0432					3		3		8	5
31	19X31A0433							3		4	5
32	19X31A0434					3		3		5	5
33	19X31A0435	4		5						4	5
34	19X31A0436	4		3						9	5
35	19X31A0437			4		4				9	5
36	19X31A0438					4				9	5
37	19X31A0439			4		5				4	5
38	19X31A0440			5				5		9	5
39	19X31A0441							5		9	5
40	19X31A0442	5						5		8	5
41	19X31A0443	5								8	5
42	19X31A0444			5		5				9	5
43	19X31A0445					5				9	5
44	19X31A0446					4		5		9	5

45	19X31A0447			5		5				8	5
46	19X31A0448			5						9	5
47	19X31A0449	3		4						8	5
48	19X31A0450	4		4						8	5
49	20X35A0401			4		4				8	5
50	20X35A0402					5		4		8	5
51	20X35A0403			2				5		9	5
52	20X35A0404			4		4				8	5
53	20X35A0405					4		4		8	5
54	20X35A0407							5		9	5
55	20X35A0408					3		5		1	5
56	20X35A0409			3		4				8	5
57	20X35A0410	3		4						8	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		18	0	32	0	30	0	22	0	52	57
Number of students attempted		18	0	33	0	30	0	22	0	57	57
Percentage of students scored more than target		100%		97%		100%		100%		91%	100%

CO Mapping with Exam Questions:

CO - 1										
CO - 2										
CO - 3										
CO - 4	Y								Y	Y
CO - 5			Y		Y				Y	Y
CO - 6							Y		Y	Y

% Students Scored >Target %	100%		97%		100%		100%		91%	100%

CO Attainment based on Exam Questions:

CO - 1										
CO - 2										
CO - 3										
CO - 4	100%								91%	100%
CO - 5			97%		100%				91%	100%
CO - 6							100%		91%	100%

CO	**Subj**	obj	Asgn	Overall	Level
CO-1					
CO-2					
CO-3					
CO-4	100%	91%	100%	97%	3.00
CO-5	98%	91%	100%	97%	3.00
CO-6	100%	91%	100%	97%	3.00

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal Examination-2) **3.00**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty : M.GANESH Academic Year: 2022-23

Branch & Section: ECE - A Year / Semester: IV/II

Course Name: LOW POWER VLSI DESIGN

S.No	Roll Number	Marks Secured	S.No	Roll Number	Marks Secured
1	19X31A0401	33	36	19X31A0438	37
2	19X31A0402	28	37	19X31A0439	48
3	19X31A0403	39	38	19X31A0440	56
4	19X31A0404	38	39	19X31A0441	30
5	19X31A0405	40	40	19X31A0442	45
6	19X31A0406	43	41	19X31A0443	51
7	19X31A0407	31	42	19X31A0444	45
8	19X31A0408	48	43	19X31A0445	34
9	19X31A0409	48	44	19X31A0446	32
10	19X31A0410	8	45	19X31A0447	47
11	19X31A0411	51	46	19X31A0448	18
12	19X31A0412	12	47	19X31A0449	30
13	19X31A0413	41	48	19X31A0450	37
14	19X31A0414	34	49	20X35A0401	40
15	19X31A0415	34	50	20X35A0402	35
16	19X31A0416	27	51	20X35A0403	38
17	19X31A0417	2	52	20X35A0404	33
18	19X31A0420	46	53	20X35A0405	43
19	19X31A0421	51	54	20X35A0407	29
20	19X31A0422	37	55	20X35A0408	34
21	19X31A0423	20	56	20X35A0409	35
22	19X31A0424	12	57	20X35A0410	33
23	19X31A0425	42			
24	19X31A0426	42			
25	19X31A0427	51			
26	19X31A0428	3			
27	19X31A0429	53			
28	19X31A0430	40			
29	19X31A0431	45			
30	19X31A0432	46			
31	19X31A0433	AB			
32	19X31A0434	AB			
33	19X31A0435	40			
34	19X31A0436	39			
35	19X31A0437	41			
Max Marks		75			

Class Average mark	33
Number of students performed above the target	40
Number of successful students	57

Attainment Level	% students
1	40%
2	50%

Percentage of students scored more than target	70%
Attainment level	**3**

3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment

Name of the faculty : M.GANESH
Academic Year: 2022-23
Branch & Section: ECE - A
Year: IV
Course Name: LOW POWER VLSI DESIGN
Semester: II

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00		3.00	3.00	3.00
CO2	3.00		3.00	3.00	3.00
CO3	3.00		3.00	3.00	3.00
CO4		3.00	3.00	3.00	3.00
CO5		3.00	3.00	3.00	3.00
CO6		3.00	3.00	3.00	3.00
Internal & University Attainment:			3.00	3.00	
Weightage			25%	75%	
CO Attainment for the course (Internal, University)			0.75	2.25	
CO Attainment for the course (Direct Method)			3.00		

Overall course attainment level **3.00**

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Program Outcome Attainment (from Course)

Name of Faculty:	M.GANESH	Academic Year:	2022-23
Branch & Section:	ECE - A	Year:	IV
Course Name:	LOW PWER VLSI DESIGN	Semester:	II

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	2	-	-	-	-	-	-	-	3	2	2
CO2	3	3	3	2	-	-	-	-	-	-	-	3	2	2
CO3	3	-	3	2	-	-	-	-	-	-	-	3	2	2
CO4	3	-	-	3	-	-	-	-	-	-	-	3	2	2
CO5	3	-	3	3	-	-	-	-	-	-	-	3	3	3
CO6	3	-	3	3	-	-	-	-	-	-	-	3	2	2
Course	**3**	**3**	**3**	**2.5**	-	-	-	-	-	-	-	**3**	**2.167**	**2.17**

CO	**Course Outcome Attainment**
CO1	3.00
CO2	3.00
CO3	3.00
CO4	3.00
CO5	3.00
CO6	3.00
Overall course attainment level	**3.00**

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainment	**3.00**	**3.00**	**3.00**	**2.50**							**#####**	**3.00**	**2.17**	**2.17**

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)

ASSIGNMENTS AND REGISTERS

Assignment 1 script link:

https://drive.google.com/file/d/1aVL6b4zS56WUxNIRd3C3Ci08EuwhGsBV/view?usp=sharing

Assignment 2 script link:

https://drive.google.com/file/d/1i2eRdthTERiycJwWsoKbSQzKL_NB3MYX/view?usp=sharing

Attendance register link:

https://drive.google.com/file/d/15X4F7iFKVH9UbDxu2zqubU97kiXXuxNe/view?usp=sharing