Sri Indu Institute of Engineering & Technology

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Approved by AICTE, New Delhi
Affiliated to JNTUH, Hyderabad.

COURSE FILE

ON

MICROPROCESSORS & MICRO CONTROLLERS

Course Code - EC501PC

III B.Tech I-SEMESTER

A.Y.: 2022-2023

Prepared by

Mr. I.VENU
Assistant Professor

Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year	2022-2023
Course Title	MICROPROCESSORS & MICROCONTROLLERS
Course Code	EC501PC
Programme	B.Tech
Year & Semester	III year I-semester
Branch & Section	ECE-A
Regulation	R18
Course Faculty	Mr. I.VENU, Assistant Professor

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INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To Continuous assess of teaching-learning process through institute-industry collaboration.

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.

IM4: To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a recognized center in the field of Electronics and Communication Engineering by producing creative engineers with social responsibility and address ever-changing global challenges.

Mission:

DM1: To facilitate an academic environment that enables student's centric learning.

DM2: To provide state-of-the-art hardware and software technologies to meet industry requirements.

DM3: To continuously update the Academic and Research infrastructure.

DM4: To Conduct Technical Development Programs for overall professional caliber of Stake Holders.

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PROGRAM EDUCATIONAL OBJECTIVES

Program Educational objectives are to Promote:

PEO1: Graduates with a strong foundation in Electronics and Communication Engineering, Science and Technology to become successful in the chosen professional career.

PEO2: Graduates with ability to execute innovative ideas for Research and Development with continuous learning.

PEO3: Graduates inculcated with industry based soft-skills to enable employability.

PEO4: Graduates demonstrate with ability to work in interdisciplinary teams and ethical professional behavior.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

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PROGRAM OUTCOMES

1. **ENGINEERING KNOWLEDGE**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

6. **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

11. **PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING

III YEAR COURSE STRUCTURE AND SYLLABUS (R18)

Applicable From 2018-19 Admitted Batch

III YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	EC501PC	Microprocessors & Microcontrollers	3	1	0	4
2	EC502PC	Data Communications and Networks	3	1	0	4
3	EC503PC	Control Systems	3	1	0	4
4	SM504MS	Business Economics & Financial Analysis	3	0	0	3
5		Professional Elective - I	3	0	0	3
6	EC505PC	Microprocessors & Microcontrollers Lab	0	0	3	1.5
7	EC506PC	Data Communications and Networks Lab	0	0	3	1.5
8	EN508HS	Advanced Communication Skills Lab	0	0	2	1
9	*MC510	Intellectual Property Rights	3	0	0	0
		Total Credits	18	3	8	22

III YEAR II SEMESTER

S. No.	**Course Code**	**Course Title**	**L**	**T**	**P**	**Credits**
1	EC601PC	Antennas and Propagation	3	1	0	4
2	EC602PC	Digital Signal Processing	3	1	0	4
3	EC603PC	VLSI Design	3	1	0	4
4		Professional Elective - II	3	0	0	3
5		Open Elective - I	3	0	0	3
6	EC604PC	Digital Signal Processing Lab	0	0	3	1.5
7	EC605PC	e – CAD Lab	0	0	3	1.5
8	EC606PC	Scripting Languages Lab	0	0	2	1
9	*MC609	Environmental Science	3	0	0	0
		Total Credits	**18**	**3**	**8**	**22**

***MC - Environmental Science – Should be Registered by Lateral Entry Students Only.**

Note: Industrial Oriented Mini Project/ Summer Internship is to be carried out during the summer vacation between 6th and 7th semesters. Students should submit report of Industrial Oriented Mini Project/ Summer Internship for evaluation.

Professional Elective – I

EC511PE	Computer Organization & Operating Systems
EC512PE	Error Correcting Codes
EC513PE	Electronic Measurements and Instrumentation

Professional Elective – II

EC611PE	Object Oriented Programming through Java
EC612PE	Mobile Communications and Networks
EC613PE	Embedded System Design

EC501PC: MICROPROCESSORS AND MICROCONTROLLERS

B.Tech. III Year I Semester **L T P C**

3 1 0 4

Prerequisite:

Course Objectives:

1. To familiarize the architecture of microprocessors and micro controllers
2. To provide the knowledge about interfacing techniques of bus & memory.
3. To understand the concepts of ARM architecture
4. To study the basic concepts of Advanced ARM processors

Course Outcomes: Upon completing this course, the student will be able to

1. Understands the internal architecture, organization and assembly language programming of 8086 processors.
2. Understands the internal architecture, organization and assembly language programming of 8051/controllers
3. Understands the interfacing techniques to 8086 and 8051 based systems.
4. Understands the internal architecture of ARM processors and basic concepts of advanced ARM processors.

UNIT -I:

8086 Architecture: 8086 Architecture-Functional diagram, Register Organization, Memory Segmentation, Programming Model, Memory addresses, Physical Memory Organization, Architecture of 8086, Signal descriptions of 8086, interrupts of 8086.

Instruction Set and Assembly Language Programming of 8086: Instruction formats, Addressing modes, Instruction Set, Assembler Directives, Macros, and Simple Programs involving Logical, Branch and Call Instructions, Sorting, String Manipulations.

UNIT -II:

Introduction to Microcontrollers: Overview of 8051 Microcontroller, Architecture, I/O Ports, Memory Organization, Addressing Modes and Instruction set of 8051.

8051 Real Time Control: Programming Timer Interrupts, Programming External Hardware Interrupts, Programming the Serial Communication Interrupts, Programming 8051 Timers and Counters

UNIT –III:

I/O And Memory Interface: LCD, Keyboard, External Memory RAM, ROM Interface, ADC,

DAC Interface to 8051.

Serial Communication and Bus Interface: Serial Communication Standards, Serial Data Transfer Scheme, On board Communication Interfaces-I2C Bus, SPI Bus, UART; External Communication Interfaces-RS232,USB.

UNIT –IV:

ARM Architecture: ARM Processor fundamentals, ARM Architecture – Register, CPSR, Pipeline, exceptions and interrupts interrupt vector table, ARM instruction set – Data processing, Branch instructions, load store instructions, Software interrupt instructions, Program status register instructions, loading constants, Conditional execution, Introduction to Thumb instructions.

UNIT – V:

Advanced ARM Processors: Introduction to CORTEX Processor and its architecture, OMAP Processor and its Architecture.

TEXT BOOKS:

1. Advanced Microprocessors and Peripherals – A. K. Ray and K. M. Bhurchandani, TMH, 2nd Edition 2006.

2. ARM System Developers guide, Andrew N SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier, 2012

REFERENCE BOOKS:

1. The 8051 Microcontroller, Kenneth. J. Ayala, Cengage Learning, 3rd Ed, 2004.

2. Microprocessors and Interfacing, D. V. Hall, TMGH, 2nd Edition 2006.

3. The 8051 Microcontrollers, Architecture and Programming and Applications -K. Uma Rao, Andhe Pallavi, Pearson, 2009.

4. Digital Signal Processing and Applications with the OMAP- L138 Experimenter, Donald Reay, WILEY 2012.

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Website: https://siiet.ac.in/

COs and Mapping with PO/PSO

Course: MICROPROCESSORS AND MICROCONTROLLERS (C311) Class: III ECE-A

Course Outcomes

After completing this course, the student will be able to:

C311.1: Basic understanding of 8086 microprocessor architectures and its functionalities. [Knowledge]

C311.2: Design and Develop 8086 based systems for real time applications using low level language like ALP. [Synthesis]

C311.3: Basic understanding of 8051 microcontrollers architectures and its functionalities [Knowledge]

C311.4: Discuss the input/output memory interface serial communication and Bus interface device.[Evaluation]

C311.5:Analyze the internal architecture of ARM processor [Analysis]

C311.6: Classify the internal architecture of CORTEX ARM processor and MAP ARM processor [Analysis]

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C311.1	3	2	2	2	-	-	-	-	-	-	-	2	2	1
C311.2	3	2	2	3	-	-	-	-	-	-	-	2	2	1
C311.3	3	3	2	3	-	-	-	-	-	-	2	2	3	3
C311.4	3	3	2	3	-	-	-	-	-	-	2	2	3	3
C311.5	3	3	2	2	-	-	-	-	-	-	-	2	3	3
C311.6	2	2	2	1	-	-	-	-	-	-	3	2	3	3
	2.83	**2.50**	**2.00**	**2.33**	-	-	-	-	-	-	**2.33**	**2.00**	**2.67**	**2.33**

CO- PO/PSO Mapping - Justification

Course: MICROPROCESSORS AND MICROCONTROLLERS (C311) Class: III ECE-A

P01.ENGINEERING KNOWLEDGE: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

P02.PROBLEM ANALYSIS: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

P03. **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet t h e specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO11. PROJECT MANAGEMENT AND FINANCE: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PSO 1: Design Skills: Design, analysis and development a economical system in the area of Embedded system & VLSI design.

PSO 2: Software Usage: Ability to investigate and solve the engineering problems using MATLAB, Keil and Xilinx.

CO-PO mapping Justification

C311.1: Basic understanding of 8086 microprocessor architectures and its functionalities. [Knowledge]

	Justification
PO1	Thorough understanding of the 8086 microprocessor and its applications requires a solid foundation in mathematics, science, and engineering fundamentals. Applying this knowledge to solve complex engineering problems involves designing efficient systems, optimizing code, and interfacing with various components to meet specific requirements in

	diverse applications(Level-3)
PO2	Basic understanding of the 8086 microprocessor and its functionalities is essential for problem analysis in engineering. This involves identifying and formulating problems, conducting thorough literature research, applying first principles of mathematics and sciences, and reaching substantiated conclusions that contribute to the effective resolution of engineering challenges related to 8086 microprocessor-based systems.(Level-2)
PO3	Basic understanding of the 8086 microprocessor architecture is essential for designing and developing solutions to complex engineering problems. This knowledge enables engineers to address specific needs, consider public health and safety, accommodate cultural and societal factors, and be mindful of environmental considerations throughout the design process.(Level-2)
PO4	Basic understanding of the 8086 microprocessor architecture is crucial for conducting investigations of complex problems. This knowledge facilitates the design of experiments, analysis and interpretation of data, synthesis of information, and the formulation of valid conclusions based on research-based knowledge and methods.(Level-1)
PO12	Basic understanding of the 8086 microprocessor architecture serves as a foundational platform for life-long learning by nurturing independent learning skills, adaptability to technological changes, and a continuous pursuit of knowledge in the ever-evolving field of microprocessor technology.(Level-3)
PSO1	Basic understanding of the 8086 microprocessor architecture serves as a foundational platform for life-long learning by nurturing independent learning skills, adaptability to technological changes, and a continuous pursuit of knowledge in the ever-evolving field of microprocessor technology.(Level-2)
PSO2	Basic understanding of the 8086 microprocessor architecture is essential for designing and developing solutions to complex engineering problems. This knowledge enables engineers to address specific needs, consider public health and safety, accommodate cultural and societal factors, and be mindful of environmental considerations throughout the design process.(Level-2)

C311.2: Design and Develop 8086 based systems for real time applications using low level language like ALP. [Synthesis]

	Justification
PO1	Designing and developing 8086-based systems for real-time applications using low-level language aligns with engineering knowledge by applying mathematical, scientific, and engineering fundamentals. This includes optimizing code, managing resources, and addressing the unique challenges posed by real-time constraints, demonstrating a comprehensive approach to solving complex engineering problems. (Level-3)
PO2	Designing and developing 8086-based systems for real-time applications using ALP aligns with problem analysis by addressing complex engineering challenges through the identification, formulation, literature research, and analysis of problems using foundational principles of mathematics, natural sciences, and engineering sciences. This approach ensures that substantiated conclusions are reached in the design process, contributing to the effective resolution of engineering challenges in real-time systems. (Level-2)
PO3	Designing and developing 8086-based systems for real-time applications using ALP aligns with the design and development of solutions for complex engineering problems. This involves addressing specified needs while considering public health and safety, cultural, societal, and environmental considerations, ultimately leading to the creation of effective and responsible solutions. (Level-3)

PO4	Designing and developing 8086-based systems for real-time applications using ALP aligns with conducting investigations of complex problems. This involves leveraging research-based knowledge, employing research methods such as literature reviews and experiments, and synthesizing information to provide valid conclusions that guide the effective design of real-time systems. (Level-3)
PO12	Designing and developing 8086-based systems for real-time applications using ALP aligns with life-long learning by recognizing the need for continuous skill enhancement, adaptability to technological changes, exploration of advanced concepts, and the ability to independently learn and apply new knowledge throughout one's engineering career. (Level-2)
PSO1	Designing and developing 8086-based systems for real-time applications using ALP aligns with life-long learning by recognizing the need for continuous skill enhancement, adaptability to technological changes, exploration of advanced concepts, and the ability to independently learn and apply new knowledge throughout one's engineering career. (Level-2)
PSO2	Designing and developing 8086-based systems for real-time applications using ALP aligns with conducting investigations of complex problems. This involves leveraging research-based knowledge, employing research methods such as literature reviews and experiments, and synthesizing information to provide valid conclusions that guide the effective design of real-time systems. (Level-2)

C311.3: Basic understanding of 8051 microcontrollers architectures and its functionalities [Knowledge]

	Justification
PO1	Basic understanding of 8051 microcontroller architectures and functionalities demonstrates the application of mathematics, science, and engineering fundamentals. Engineers leverage this knowledge to design solutions, address complex problems, and specialize in areas such as embedded systems or control systems, showcasing a comprehensive approach to engineering challenges. (Level-3)
PO2	Basic understanding of 8051 microcontroller architectures and functionalities facilitates problem analysis through the identification and formulation of complex engineering problems. Engineers leverage research-based knowledge, apply first principles of mathematics and natural sciences, and reach substantiated conclusions to effectively address challenges within the constraints of the 8051 microcontroller. (Level-3)
PO3	Basic understanding of 8051 microcontroller architectures and functionalities facilitates the design and development of solutions for complex engineering problems. Engineers leverage this knowledge to create systems that meet specified needs while considering public health and safety, cultural, societal, and environmental considerations, contributing to the responsible and effective deployment of technology. (Level-2)
PO4	Basic understanding of 8051 microcontroller architectures and functionalities facilitates the ability to conduct investigations of complex problems. Engineers leverage research-based knowledge and research methods, including design of experiments, analysis, and synthesis of information, to provide valid conclusions and contribute to the continuous improvement of solutions using the 8051 microcontroller. (Level-3)
PO11	Basic understanding of 8051 microcontroller architectures and functionalities aligns with project management and finance principles by enabling engineers to apply engineering and management knowledge in project planning, lead multidisciplinary teams, and make informed financial decisions throughout the project lifecycle. (Level-2)
PO12	Basic understanding of 8051 microcontroller architectures justifies the commitment to life-

	long learning by acknowledging the need to continuously adapt, explore, and engage in independent learning in the broader context of technological change. This commitment ensures that individuals remain agile, adaptable, and relevant in a rapidly evolving technological landscape. (Level-2)
PSO1	Basic understanding of 8051 microcontroller architectures and functionalities facilitates the ability to conduct investigations of complex problems. Engineers leverage research-based knowledge and research methods, including design of experiments, analysis, and synthesis of information, to provide valid conclusions and contribute to the continuous improvement of solutions using the 8051 microcontroller. (Level-3)
PSO2	Basic understanding of 8051 microcontroller architectures and functionalities demonstrates the application of mathematics, science, and engineering fundamentals. Engineers leverage this knowledge to design solutions, address complex problems, and specialize in areas such as embedded systems or control systems, showcasing a comprehensive approach to engineering challenges. (Level-3)

C311.4: Discuss the input/output memory interface serial communication and Bus interface device.[Evaluation]

	Justification
PO1	The design and implementation of I/O memory interfaces, serial communication, and bus interface devices require the application of engineering knowledge encompassing mathematics, science, engineering fundamentals, and specialized expertise. Engineers draw upon this knowledge to address complex engineering problems, ensuring the reliable and efficient interaction between microcontrollers and external devices in various embedded systems and applications. (Level-3)
PO2	Engineers employ problem analysis principles to identify, formulate, research literature, and analyze complex engineering problems related to I/O memory interfaces, serial communication, and bus interface devices. The application of first principles in mathematics, natural sciences, and engineering sciences ensures a systematic and substantiated approach to problem-solving in these areas. (Level-3)
PO3	Engineers design solutions for complex engineering problems related to I/O memory interfaces, serial communication, and bus interface devices. The design process includes considerations for public health and safety, as well as cultural, societal, and environmental factors, ensuring that the engineered systems meet specified needs responsibly and sustainably. (Level-2)
PO4	Engineers conduct investigations of complex problems related to I/O memory interfaces, serial communication, and bus interface devices. They employ research-based knowledge and methods, design experiments, analyze and interpret data, and synthesize information to provide valid conclusions. This rigorous investigative approach allows engineers to gain insights into the underlying challenges, propose effective solutions, and contribute to the continuous improvement of these critical components in complex engineering systems. (Level-3)
PO11	Engineers involved in I/O memory interface, serial communication, and bus interface device projects demonstrate a holistic understanding of both engineering and management principles. They navigate multidisciplinary environments, apply finance principles for budgeting and cost estimation, and leverage project management techniques to ensure the successful execution of projects while meeting specified needs. This integrated approach facilitates efficient project management and financial stewardship in the development of complex engineering solutions. (Level-3)

PO12	Engineers engaged in I/O memory interfaces, serial communication, and bus interface device projects demonstrate a commitment to life-long learning. They recognize the need for continuous education, prepare for independent learning, and apply their knowledge to adapt to technological changes, ensuring that their projects benefit from the latest advancements in the field. Life-long learning becomes a cornerstone for innovation, adaptability, and sustained excellence in engineering practice. (Level-3)
PS01	Engineers involved in I/O memory interface, serial communication, and bus interface device projects demonstrate a holistic understanding of both engineering and management principles. They navigate multidisciplinary environments, apply finance principles for budgeting and cost estimation, and leverage project management techniques to ensure the successful execution of projects while meeting specified needs. This integrated approach facilitates efficient project management and financial stewardship in the development of complex engineering solutions. (Level-3)
PSO2	The design and implementation of I/O memory interfaces, serial communication, and bus interface devices require the application of engineering knowledge encompassing mathematics, science, engineering fundamentals, and specialized expertise. Engineers draw upon this knowledge to address complex engineering problems, ensuring the reliable and efficient interaction between microcontrollers and external devices in various embedded systems and applications. (Level-3)

C311.5: Analyze the internal architecture of ARM processor [Analysis]

	Justification
PO1	The analysis of the internal architecture of an ARM processor requires the application of engineering knowledge across various domains. Mathematics, science, engineering fundamentals, and engineering specialization are integrated into the design process to address complex engineering problems. This includes optimizing instruction sets, leveraging semiconductor physics, applying digital logic design principles, and specializing in areas like VLSI design or embedded systems to create efficient and high-performance ARM processors for diverse applications. (Level-3)
PO2	The problem analysis of the internal architecture of an ARM processor involves identifying, formulating, researching, and analyzing complex engineering problems. The application of first principles of mathematics, natural sciences, and engineering sciences ensures a systematic and substantiated approach to understanding and optimizing the ARM processor's internal architecture for specific performance objectives. (Level-3)
PO3	The design and development of solutions for the internal architecture of ARM processors involve a holistic approach. Engineers consider public health and safety, cultural and societal impact, and environmental sustainability while optimizing for specific needs. This comprehensive design process ensures that ARM processors meet specified requirements while aligning with broader considerations for responsible and sustainable engineering practices. (Level-3)
PO4	Conducting investigations of complex problems related to the internal architecture of an ARM processor involves a rigorous application of research-based knowledge and research methods. Engineers design experiments, collect and analyze data, synthesize information, and draw valid conclusions, contributing to an in-depth understanding of the ARM processor's behavior and performance characteristics. This investigative approach guides informed decision-making and continuous refinement of ARM processor designs. (Level-2)
PO12	Analyzing the internal architecture of an ARM processor is deeply connected to the principle of life-long learning. Recognizing the need for continuous education, engaging in

	independent exploration, and staying updated with the broadest context of technological change are foundational elements that contribute to a comprehensive understanding of ARM processor internals. Life-long learning ensures that engineers remain adaptive, innovative, and well-prepared to navigate the dynamic landscape of semiconductor design and processor technology. (Level-2)
PSO1	The design and development of solutions for the internal architecture of ARM processors involve a holistic approach. Engineers consider public health and safety, cultural and societal impact, and environmental sustainability while optimizing for specific needs. This comprehensive design process ensures that ARM processors meet specified requirements while aligning with broader considerations for responsible and sustainable engineering practices. (Level-3)
PSO2	The design and development of solutions for the internal architecture of ARM processors involve a holistic approach. Engineers consider public health and safety, cultural and societal impact, and environmental sustainability while optimizing for specific needs. This comprehensive design process ensures that ARM processors meet specified requirements while aligning with broader considerations for responsible and sustainable engineering practices. (Level-3)

C311.6: Classify the internal architecture of CORTEX ARM processor and MAP ARM processor [Analysis]

	Justification
PO1	The classification of Cortex ARM processors and MAP ARM processors is justified by their shared ARM architecture foundation and their specific optimizations for different applications. The application of engineering knowledge, spanning mathematics, science, engineering fundamentals, and specialization, is evident in the design choices made to address complex engineering problems in diverse domains. The classification reflects the versatility and adaptability of ARM processors in addressing a broad range of engineering challenges. (Level-2)
PO2	The classification of Cortex ARM processors and MAP ARM processors is justified by a thorough problem analysis that involves applying first principles of mathematics, natural sciences, and engineering sciences. The analysis reveals distinct features and optimizations tailored to address complex engineering problems in diverse domains, showcasing the adaptability and problem-solving capabilities of ARM processors. (Level-2)
PO3	The classification of Cortex ARM processors and MAP ARM processors is justified by their design and development approach to solving complex engineering problems. Cortex processors demonstrate versatility, scalability, and consideration for energy efficiency to meet diverse application needs. MAP ARM processors showcase application-specific optimizations, customized features, and real-time capabilities, addressing specific engineering challenges with a targeted design. Both classifications align with the broader principles of design and development, considering public health, safety, and environmental impact, and demonstrating an awareness of cultural and societal considerations. (Level-1)
PO4	The classification of Cortex ARM processors and MAP ARM processors is substantiated by the rigorous application of research-based knowledge and research methods, including the design of experiments, analysis, interpretation of data, and synthesis of information to provide valid and informed conclusions about their respective internal architectures(Level-3)

PO11	The classification of Cortex ARM processors and MAP ARM processors is substantiated by the rigorous application of research-based knowledge and research methods, including the design of experiments, analysis, interpretation of data, and synthesis of information to provide valid and informed conclusions about their respective internal architectures(Level-3)
PO12	The classification of Cortex ARM processors and MAP ARM processors is justified by the inherent commitment to life-long learning in the field of processor architecture and design. This commitment ensures that engineers and developers recognize the need for continuous education, preparation, and adaptation in the broadest context of technological change. (Level-2)
PSO1	The classification of Cortex ARM processors and MAP ARM processors is justified by their shared ARM architecture foundation and their specific optimizations for different applications. The application of engineering knowledge, spanning mathematics, science, engineering fundamentals, and specialization, is evident in the design choices made to address complex engineering problems in diverse domains. The classification reflects the versatility and adaptability of ARM processors in addressing a broad range of engineering challenges. (Level-3)
PSO2	The classification of Cortex ARM processors and MAP ARM processors is justified by their design and development approach to solving complex engineering problems. Cortex processors demonstrate versatility, scalability, and consideration for energy efficiency to meet diverse application needs. MAP ARM processors showcase application-specific optimizations, customized features, and real-time capabilities, addressing specific engineering challenges with a targeted design. Both classifications align with the broader principles of design and development, considering public health, safety, and environmental impact, and demonstrating an awareness of cultural and societal considerations. (Level-3)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

ACADEMIC CALENDAR 2022-23

B. Tech./B. Pharm. III YEAR I & II SEMESTERS

I SEM

S. No	Description	Duration	
		From	To
1	Commencement of I Semester classwork	**09.09.2022**	
2	1st Spell of Instructions (including Dussehra Recess)	09.09.2022	10.11.2022 (9 Weeks)
3	Dussehra Recess	03.10.2022	08.10.2022 (1 Week)
4	First Mid Term Examinations	11.11.2022	17.11.2022 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	24.11.2022	
6	2nd Spell of Instructions	18.11.2022	12.01.2023 (8 Weeks)
7	Second Mid Term Examinations	16.01.2023	21.01.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	23.01.2023	28.01.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	30.01.2023	
10	End Semester Examinations	30.01.2023	11.02.2023 (2 Weeks)

Note: No. of Working/ instructional days: 92

II SEM

S. No	Description	Duration	
		From	To
1	Commencement of II Semester classwork	**13.02.2023**	
2	1st Spell of Instructions	13.02.2023	08.04.2023 (8 Weeks)
3	First Mid Term Examinations	10.04.2023	15.04.2023 (1 Week)
4	Submission of First Mid Term Exam Marks to the University on or before	22.04.2023	
5	2nd Spell of Instructions (including Summer Vacation)	17.04.2023	24.06.2023 (10 Weeks)
6	**Summer Vacation**	15.05.2023	27.05.2023 (2 Weeks)
7	Second Mid Term Examinations	26.06.2023	01.07.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	03.07.2023	08.07.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	08.07.2023	
10	End Semester Examinations	10.07.2023	22.07.2023 (2 Weeks)

Note: No. of Working/ instructional days: 90

REGISTRAR

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC)

Accredited by NAAC A+ Grade, Recognized under 2(f) of UGC Act 1956.

(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana – 501 510

https://siiet.ac.in/

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Class Timetable

CLASS: III-B.Tech ECE-A **A.Y:2022-23** **SEMESTER: I** **LH: C-201**

TIME/ DAY	I 9:40-10:30	II 10:30 -11:20	III 11:20-12:10	IV 12:10-1:00	1:00-1:30	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON	DCN	IPR	CS	LIB	LUNCH	MPMC LAB / DCN LAB		
TUE	CS	MPMC	EMI	DCN		CYB	BEFA	SPORTS
WED	CYB	MPMC(T)/DCN(T)	CS	EMI		DCN LAB / MPMC LAB		
THU	EMI	DCN	CO-CU/DAA			IPR	MPMC	CS(T)/MPMC(T)
FRI	CS	BEFA	EMI	MPMC		DCN(T)/CS(T)	ACS LAB	
SAT	MPMC	IPR	MPMC(ADJUNCT)			BEFA	DCN	COUN

*(T) – Tutorial Concern Faculty

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the Faculty
EC501PC	MPMC- Microprocessors & Microcontrollers	I.Venu	EC505PC	MPMC LAB- Microprocessors & Microcontrollers Lab	I.Venu/K.Srikanth/P.Srilatha
EC502PC	DCN-Data Communications and Networks	Y.Raju	EC506PC	DCN LAB- Data Communications and Networks Lab	J.Anand Rao/ M.Ganesh/Y.Raju
EC503PC	CS-Control Systems	K.Srikanth	EN508HS	ACS LAB- Advanced Communication Skills Lab	D.Ananda Rao
SM504MS	BEFA- Business Economics & Financial Analysis	K V Nagamani	*MC510	IPR-Intellectual Property Rights	S.Srinivas
			MPMC(ADJUNCT)	G.Chandrasekhar	
EC513PE	EMI-Electronic Measurements and Instrumentation (PE-I)	M.Ganesh	LIB	Library	B.Jyothirmai/S.Alekhya
			COUN	Counseling	Dr.S.Suresh/S.Alekhya/M.Ganesh
*CYB	Cyber Security	T.Divya	CO-CU/DAA	Co-Curricular/Dept.Assc.Act.	M.Ganesh/S.Naresh/P.KrishnaRao
			SPORTS	Sports	M.Ganesh/K.Padma

Class Incharge

Head of the Department

PRINCIPAL

Sri Indu Institute of Engineering & Tech.
Sheriguda(V), Ibrahimpatnam
R R Dist. Telangana-501 510

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

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Website: https://siiet.ac.in/

LESSON PLAN

Programme: B.Tech	Academic Year: 2022-23
Year: III	Semester: I
Course Title: MICROPROCESSORS & MICROCONTROLLERS	Course Code: EC501PC
Name of Faculty: Mr.I.VENU	

UNIT -I:

8086 Architecture: 8086 Architecture-Functional diagram, Register Organization, Memory Segmentation, Programming Model, Memory addresses, Physical Memory Organization, Architecture of 8086, Signal descriptions of 8086, interrupts of 8086.

Instruction Set and Assembly Language Programming of 8086: Instruction formats, Addressing modes, Instruction Set, Assembler Directives, Macros, and Simple Programs involving Logical, Branch and Call Instructions, Sorting, String Manipulations.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Introduction to microprocessors and microcontrollers	T1	BB
1	**8086 architecture**	T1	BB
1	**Function diagram of 8086**	R1	BB
1	Register organization and flag register organization of 8086	R1	BB
1	Memory segmentation and memory address of 8086	R1	BB
1	Physical memory organization and pin diagram of 8086	R1	BB
1	Interrupts of 8086 and instruction format of 8086	R1	BB
1	Addressing modes of 8086	R1	BB
1	Addressing modes, instruction set 8086	R1	BB
2	Instruction set of 8086	R1	BB
1	Assembler directives	R1	BB
1	Macros and simple programs of logical branch	R1	BB
1	Simple programs of call instruction ,sorting and string instruction	R1	BB
1	Simple programs of call instruction ,sorting and string instruction	R1	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course outcome 1:student will able design and implement programs on 8086 microprocessor			

*Session Duration: 50 minutes

*Total Number of Hours/Unit: 15

UNIT -II:

Introduction to Microcontrollers: Overview of 8051 Microcontroller, Architecture, I/O Ports, Memory Organization, Addressing Modes and Instruction set of 8051.

8051 Real Time Control: Programming Timer Interrupts, Programming External Hardware Interrupts, Programming the Serial Communication Interrupts, Programming 8051 Timers and Counters.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Introduction to microcontrollers	T1	BB
1	Overview of 8051 microcontroller	T1	BB
1	Architecture of 8051 microcontroller	R1	BB
1	Pin diagram of 8051 microcontroller	R1	BB
1	Memory organization of 8051	R1	BB
1	Addressing mode of 8051	R1	BB
2	Instruction set of 8051	R1	BB
2	Programming timer interrupts	R1	BB
1	Programming external hardware interrupts	R1	BB
1	Serial communication interrupts	R1	BB
1	8051 timers and counters	R1	BB
1	Programs	R1	BB
Gap beyond syllabus (if any):			
Gap within the syllabus (if any)			
Course Outcome 1 student will able design and implement programs on 8086 microprocessor.			

*Session Duration: 50 minutes

*Total Number of Hours/Unit: 14

UNIT –III:

I/O And Memory Interface: LCD, Keyboard, External Memory RAM, ROM Interface, ADC, DAC Interface to 8051.

Serial Communication and Bus Interface: Serial Communication Standards, Serial Data Transfer Scheme, On board Communication Interfaces-I2C Bus, SPI Bus, UART; External Communication Interfaces-RS232,USB.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Introduction to interfacing of various devices	T1	BB
1	Interfacing of LCD to 8051	T1	BB
1	External memory|(RAM&ROM) interface	T1	BB
1	ADC,DAC interface to 8051	T1	BB
1	Serial communication standrads	R1	BB
1	Serial data transfer scheme	T1	BB
2	On board interfaces-12C Bus,SPI and UART	T1	BB
1	External communication interdfaces-RS232,USB	T1	BB
1	PROGRAMS	R1	BB
1	Introduction to interfacing of various devices	T1	BB
1	Interfacing of LCD to 8051	T1	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: student will able design and implement programs on 8086 Microprocessor			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 12

UNIT –IV:

ARM Architecture: ARM Processor fundamentals, ARM Architecture – Register, CPSR, Pipeline, exceptions and interrupts interrupt vector table, ARM instruction set – Data processing, Branch instructions, load store instructions, Software interrupt instructions, Program status register instructions, loading constants, Conditional execution, Introduction to Thumb instructions.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
1	Introduction to ARM processor	R1	BB
1	Fundamentals of ARM processor	R1	BB
1	Architecture of ARM processor	T1	BB
1	Register and CPSR,pipeline of ARM	T1	BB
1	Exceptions and interrupts interrupt vector table	T1	BB
2	ARM instruction set	T1	BB
1	ARM instruction set	T1	BB
2	Loading constansts,conditional execution	T1	BB
1	Introduction to thumb instructions	R1	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: :student will able design and implement programs on 8086 microprocessor.			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 11

Unit-V Syllabus

Advanced ARM Processors: Introduction to CORTEX Processor and its architecture, OMAP Processor and its Architecture.

No. of Sessions Planned	Topics	Reference	Teaching Method/ Aids
2	Introduction to CORTEX Processor	T2,R2	BB
1	Features of CORTEX Processor	T2,R2	BB
1	Architecture of CORTEX Processor	T2	BB
1	OMAP Introduction & features	T1, R 1	BB
2	Architecture of OMAP Processor	T1, R 1	BB
Gap beyond syllabus(if any):			
Gap within the syllabus(if any)			
Course Outcome 1: Design state model of a system and determine the transfer function for Linear Time Variant Systems			

*Session Duration: 50minutes

*Total Number of Hours/Unit: 7

TEXTBOOKS:

1. Advanced Microprocessors and Peripherals– .K.RayandK.M.Bhurchandani, MHE,2ndEdition 2006.

2. The 8052 microcontroller,Kenneth.J.Ayala , Cengaga Leaning, 3rd Ed.

3. ARM System Developer's guide, Andrew N SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier, 2012

REFERENCEBOOKS:

1.Microprocessor and interfacing, D.V.Hall,MGH,2nd Edition 2006.

2.Introduction to Embedded Systems, Shibu K.V,MHE,2009.

3. The8051Microcontrollers, ArchitectureandProgrammingandApplications-K.UmaRao,Andhe Pallavi,Pearsons,2009.

Lecture notes

Unit 1 link:

https://docs.google.com/presentation/d/1T8AmKFfZDkSn-fXu2Bt612bLOta4F72L/edit?usp=sharing&ouid=100385160781177538013&rtpof=true&sd=true

Unit 2 link:

https://docs.google.com/presentation/d/1xV4iMlD_UV1iyDk1PlwdXSvuS6mswfkQ/edit?usp=sharing&ouid=100385160781177538013&rtpof=true&sd=true

Unit 3 link:

https://docs.google.com/presentation/d/1iv8bmr-6mvv6wEhyjfp7b1R4W4_YZ-IM/edit?usp=sharing&ouid=100385160781177538013&rtpof=true&sd=true

Unit 4 link:

https://docs.google.com/presentation/d/17vcdzVH8rAczA9_c-TgerTFNn_BY-Nxh/edit?usp=sharing&ouid=100385160781177538013&rtpof=true&sd=true

Unit 5 link:

https://docs.google.com/presentation/d/1oNQ2onzkKrHaVDCTF7pxguAY_ZfHWCXr/edit?usp=sharing&ouid=100385160781177538013&rtpof=true&sd=true

Code No: 155CF **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, March - 2021
MICROPROCESSORS AND MICROCONTROLLERS
(Common to ECE, EIE)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

Discuss the following addressing modes with examples:
i) Direct ii) Register indirect iii) Base plus index iv) immediate v) Scaled indexed.
b) Write an ALP using 8086 instructions to count the numbers of zeros in a given 8-bit number. [8+7]

2.a) Explain structure of 8086 interrupt vector table with neat diagram.
b) Discuss the functions of segment registers of 8086 with examples. Give some advantages of memory segmentation. [7+8]

3.a) State various modes available for timers in 8051.
b) Explain how interrupts are prioritized? [8+7]

4.a) With example, explain the arithmetic and logic instruction of 8051 microcontroller.
b) Explain the different addressing modes of 8051. [7+8]

5.a) Draw and Explain interfacing of DAC with 8051. Write a program to generate square wave.
b) Explain bit addresses for RAM. [8+7]

6.a) Explain the bit addresses for I/O of 8051
b) Explain the baud rates of serial communication in 8051. [7+8]

7.a) Describe the pipeline operation of ARM.
b) Which are the different features of ARM instruction set that make it suitable for embedded applications. [7+8]

8.a) With a neat diagram, explain the different general purpose registers of ARM Processors.
b) Discuss about the OMAP processor in detail. [8+7]

---ooOoo---

Code No: 155CF **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, September - 2021
MICROPROCESSORS AND MICROCONTROLLERS
(Common to ECE, EIE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) Draw the Register organization of 8086 Microprocessor and explain the operation of each register.
b) Discuss about different instruction formats of 8086 with examples. [8+7]

2. With a neat diagram, explain the architecture of 8086 microprocessor. [15]

3.a) Explain the memory organization of 8051 microcontroller with neat diagram.
b) Write a program to transfer a byte from code memory address 1000H to internal RAM and external RAM address 10H and 1000H respectively. [9+6]

4. Explain the instruction set of 8051 microcontroller with suitable examples. [15]

5.a) Develop an assembly language program for key identification and key-code generation.
b) Explain the interfacing procedure of an 8-bit ADC. [7+8]

6.a) Discuss how wire-AND connection of all SDA and SCL lines help in bus arbitration.
b) How in and out data transaction takes place in USB? Give operational overview. [7+8]

7.a) What is Pipelining. Explain in detail schematically with respect to ARM processor.
b) Explain the ARM Single-Register and Multiple-Register load-store addressing modes with example. [8+7]

8. Explain the architecture of CORTEX processor with neat diagram. [15]

---ooOoo---

Code No: 126EM **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year II Semester Examinations, May - 2016
MICROPROCESSORS AND MICROCONTROLLERS
(Common to ECE, BME)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) List out different segmentations presented in 8086 Microprocessor. [2]
b) Draw the flag register of 8086 Microprocessor and explain function of each flag. [3]
c) Explain one byte and two byte instruction frame format. [2]
d) List the data transfer instruction set of 8086 microprocessor. [3]
e) Draw the BSR mode frame format. [2]
f) Explain the concept of interrupt service routine of 8086 microprocessor. [3]
g) Explain register set of 8051 Microcontroller. [2]
h) List out the difference between microprocessor and microcontroller. [3]
i) Draw the T0 and T1 registers of 8051 microcontroller. [2]
j) Explain the hard ware interrupts of 8051 microcontroller with examples. [3]

PART - B

(50 Marks)

2.a) Draw the register organization of 8086 Microprocessor and explain it.
b) Explain the minimum mode pins of 8086 Microprocessor in detail.
c) Explain the concept of physical address calculation of 8086 microprocessor. [3+3+4]

OR

3.a) Draw the internal architecture of 8086 microprocessor and explain its operation.
b) Draw the timing diagram of minimum mode write operation and explain it. [5+5]

4.a) Define addressing mode and explain different addressing modes used in 8086 Microprocessor with examples
b) List out different assembler directives used in 8086 microprocessor with examples. [5+5]

OR

5.a) Write an assembly language program to find the largest number in an array of 8-bit numbers.
b) List the string manipulation instruction set of 8086 microprocessor with examples. [5+5]

6.a) Draw the internal architecture of 8255 PPI and explain its operation.
b) Draw the interacting diagram of A/D convertor with 8086 microprocessor and explain its operation. [5+5]

OR

7.a) Explain the concept of keyboard and interfacing along with block diagram.
b) Explain the concept of methods of serial communication with examples. [5+5]

8.a) Draw the internal architecture of 8051 Microcontroller and explain its operation.
b) Draw the PSW and TCON registers of 8051 microcontroller. [5+5]

OR

9.a) Explain the different futures of 8051 microcontroller in detail.
b) Draw the pin diagram of 8051 microcontroller and explain the function of each pin in detail. [5+5]

10.a) Explain the different addressing modes used in 8051 microcontroller with examples.
b) Draw the SCON register frame format and explain it. [5+5]

OR

11.a) List out the different instruction set of 8051 microcontroller and explain with examples.
b) Write an assemble language program for LED blinking in 8051 microcontroller. [5+5]

---ooOoo---

Sri Indu Institute of Engineering & Technology

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Set – I

I - Mid Examinations, NOV-2022

Year &Branch: III-ECE (A,B,C) Date: 11/11/2022(FN)

Subject: MICROPROCESSOR AND MICRO CONTROLLERS Max. Marks: 10 Time: 60 mins

---

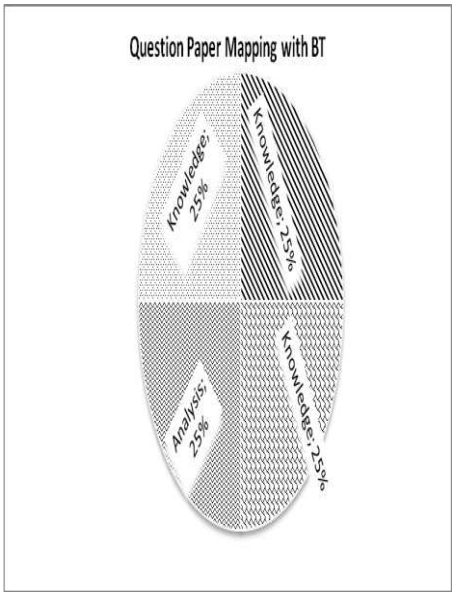
Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

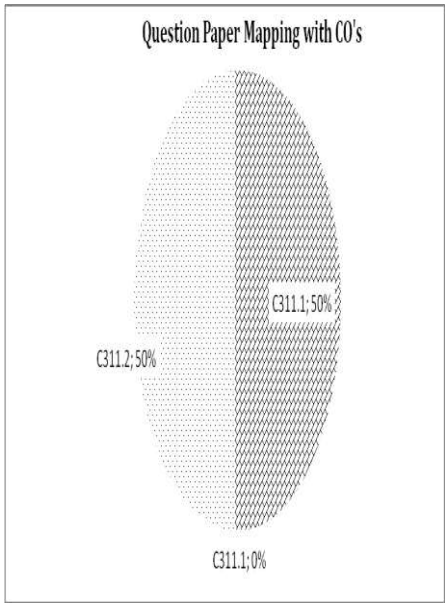
1.Draw the internal architecture of 8086 microprocessor and Explain its operation. (C311.1) (Knowledge)

2. Explain the various addressing modes of 8086 microprocessor? (C311.1) (Knowledge)

3.Explian the memory organization of 8051 micro controller. (C311.2) (Analysis)

4. Draw the pin configuration of 8051 micro controller and explain the operation. (C311.2) (Knowledge)





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II - Mid Examinations, JAN-2023

Set – I

Year &Branch: III-ECE (A,B,C) Date: 19/01/2023(FN)

Subject: MICROPROCESSOR AND MICRO CONTROLLERS Max. Marks: 10 Time: 60 mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

1. Draw and explain about OMAP(Open-Multimedia Application Platform) architecture.

(C311.5) (Comprehension)

2. Explain the interfacing of 8051 with external ROM and RAM?

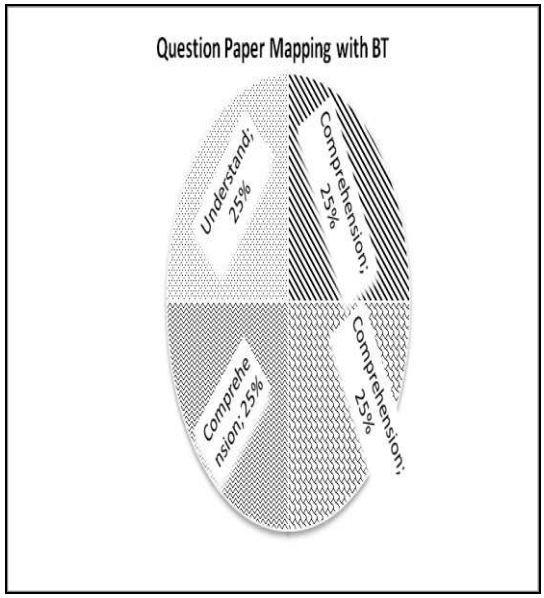
(C311.3) (Comprehension)

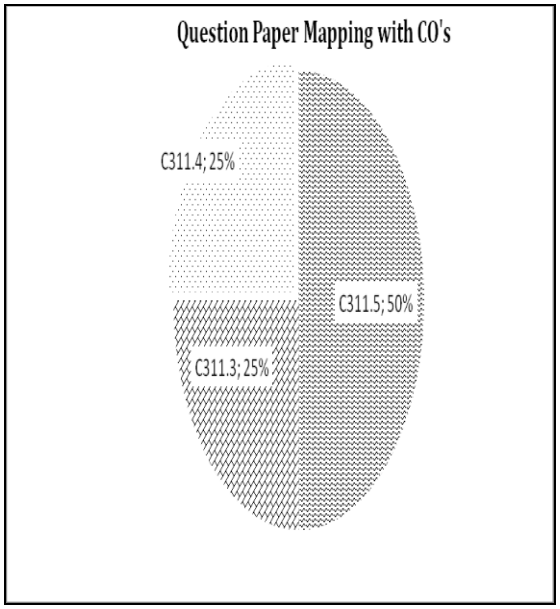
3. Explian about ARM Core architecture with the help of neat block diagram.

(C311.4) (Comprehension)

4. Write in detail about CORTEX-M architecture

(C311.5) (Understand)





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B-Tech I - Mid Examinations, NOV-2022

Objective Type Exam

Year &Branch: III –ECE-A **Date: 11-11-2022(FN)**

Subject: MPMC Max. Marks: 10 Time: 20 mins

Name: ……..Roll No……

Answer All the Questions. All Questions Carry Equal Marks.

I. Choose the Correct Answer:

1._____ is a positive edge triggered non maskable interrupt request [ ]

a) INTR b) RESET c) NMI d) NMINTR

2.8086 microprocessor memory size is _____[ ]

a)1 MB b) 128 Bytes c) 1 GB d) 1 TB

3. In _____ INT0 and INT1 are high. [ ]

a) level b) edge c) normal d)None of the above

4.Number of modes of operation of serial port are _____ [ ]

a) 1 b) 2 c)3 d)4

5. The general purpose registers are ……. [ ]

a) OF,FF,SF b) AX,BX,CX,DX c) CF,PF,AF d) None of the above

6.The 8086 allows only…….. active segments at a time [ ]

a) 10 b) 20 c) 4 d) 5

7. _____ is a volatile memory [ ]

a) RAM b)ROM c) EEROM d) PROM

8. The 8051 micro controller has how many I/O ports. [ ]

a)3 b) 1 c) 2 d)4

9. Which of these register of 8051 is of 16-bit [ ]

a) A b) PSW c) DPTR d)SP

10. The type of communication of serial port is _____ [ ]

a) Half Duplex b) Simplex c)Serial d) Full Duplex

II. Fill in the blanks:

11.The words used by assembly language to represent each instruction type is called _____.

12. _____ is a program used to join together several files into one large file.

13.1 Byte equal to _____bits.

14. IE stands for _____.

15. The minimum mode is used for small systems with a _____.

16. The 8086 has a _____ addresses and data bus_____.

17. Nibble equal to _____.

18. The size of the internal data RAM of 8051 is _____.

19. The creation or assertion of an interrupt using an instruction is called _____.

20. Number of general purpose registers in 8051 is _____

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

B-Tech I - Mid Examinations, JAN-2023

Objective Type Exam

Year &Branch: III –ECE-A **Date: 19-01-2023(FN)**

Subject: MPMC Max. Marks: 10 Time: 20 mins

Name: ……..Roll No……..

Answer All the Questions. All Questions Carry Equal Marks.

I. Choose the Correct Answer:

1 Address space of 8051 family is…….bytes [ ]

a) 64K b) 256 c) 128K d) 1024K

2 Resolution of a 12-bit ADC [ ]

a) 4096 b) 4095 c) 24 d) 23

3 USB stands for . [ ]

a) Universal serial Bus b) Universal Synchronous Bus

c) Universal Sequential Bus d) Universal Selection Bus

4. An ARM processor supports…….data type [ ]

a) 8-bit b) 16-bit c) 32-bit d) All the above

5. CPSR Stands for…… . [ ]

a) a)Control Programme Status Register b)Counter program status register

c) Current programme status register d)Current processor status register

6. ARM Thumb instruction supports…..data type [ ]

a) 8-bit b) 16-bit c) 32 –bit d)All the above

7. Memory of thumb instruction is [ ]

a) a) Half-word aligned b) Half-byte aligned c) Full-word aligned d)Full-byte aligned

8. Which of the following belongs to CORTEX microprocessors . [ ]

a) a) CORTEX-A b) CORTEX-M c)CORTEX-R

d)All the above

9. CISC stands for…….. [ ]

a) Conventional Instruction Set Computer b) Complex Instruction Set Computer

c) Computational Instruction Set Computer d) None Of the above

10.ARM CORTEX Series are _____ [ ]

a) 3 b) 2 c)1 d) None

II. Fill in the blanks:

11. In RS-232, RS stand for_____.

12. I2C is a_____two wire serial interface bus.

13. SPI stands for_____.

14. ARM stands for _____.

15. CPSR is a_____bit register

16. SPSR stand for_____.

17OMAP full form _____.

18. Thumb is _____bit instruction set.

19.NVIC stands for_____.

20.RISC stands for _____

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

B-Tech I - Mid Examinations, NOV-2022

Year &Branch: III –ECE-A **Date: 11-11-2022(FN)**

Subject: MPMC

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1TCLrmSpcO8DUEOqxx7RSjUayRAhTtIiS/view?usp=sharing

Objective Key Paper

I. Choose the correct alternative:

KEY:-

1.D	11.Assembly Language
2.A	12.Command
3.B	13.4 bits.
4.D	14. Interrupt Enable
5.B	15.Single processor.
6.C	16. 20 and 8
7.A	17.2 bytes or 16 bits
8.D	18.128
9.C	19.Interrupt
10.D	20.4

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

B-Tech I - Mid Examinations, NOV-2022

Year &Branch: III –ECE-A **Date: 19-01-2023(FN)**

Subject: MPMC

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1mJzn3wJh5cCkcQOFUe6ge_HZuLURJ1u7/view?usp=sharing

Objective Key Paper

KEY:-

1.C

2.A

3.A

4.C

5.C

6.B

7.A

8.D

9.B

10A

11.Recommended Standard

12.Serial Communication

13.Serial Peripheral Interface.

14. Advanced Risc Machine

15. Current Program Status Register.

16. Saved Program Status Register

17.Open Multimedia Application Platform

18.16

19.Nested Vested Interrupt Controller

20. Reduced Instruction Set Computer

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Website: https://siiet.ac.in/

ASSIGNMENT- 1

SUBJECT: MICROPROCESSORS AND MIRCORCONTROLLERS

1) Draw & explain the internal architecture of 8086 microprocessor?

(C311.1) (Knowledge)

2) Explain the addressing modes of 8086 (C311.1)(Knowledge)

3)Draw the pin configuration of 8051 micro controller& explain its operation

(C311.1)(Knowledge)

4)Explain the memory organization of 8051 micro controller

(C311.1) (Knowledge)

5) Draw the internal architecture of 8051 microcontroller and explain its operation?

(C311.1) (Knowledge)

6) Draw the structure of 8086 flag register and explain the bits? (C311.1)(Knowledge)

7) Explain about interrupt structure of 8086 microprocessor?

(C311.2) (Synthesis)

8)Explain the arithmetical and logical instructions of 8086 microprocessor

(C311.2) (Synthesis)

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ASSIGNMENT- 2

SUBJECT: MICROPROCESSOR & MICROCONTROLLERS

1. Explain the interfacing of 4x4 matrix keyboard with 8051
   (C311.4) (Evaluation)
2. Explain the interfacing of 8051 with external RAM & ROM (C311.2) (Synthesis)
3. Explain about ARM core architecture with the help of neat block diagram.
   (C311.4) (Evolution)
4. Explain thumb instruction set extensions of ARM Controllers? (C311.5) (Analysis)
5. Explain about open-multimedia application platform architecture.
   (C311.6) (Analysis)
6. Write in detail about CORTEX-M architecture?. (C311.6) (Analysis)
7. Explain interfacing of LCD to 8051 microcontroller? (C311.2) (Synthesis)
8. Explain software interrupt instruction and PSR instruction?
   (C311.6) (Analysis)

TUTORIAL TOPICS

SUBJECT: MICROPROCESSORS AND MICRO CONTROLLERS

S.NO	Unit	TOPIC	Number of Sessions Planned	Teaching method/Aids
1.	1	Register organization and flag register organization of 8086	1	BB
2		Assembler directives	1	BB
3		Addressing modes, instruction set 8086	1	BB
4	2	Pin diagram of 8051 microcontroller	1	BB
5		Architecture of 8051 microcontroller	1	BB
6		8051 timers and counters	1	BB
7	3	Interfacing of LCD to 8051	1	BB
8		ADC,DAC interface to 8051	1	BB
9		On board interfaces-12C Bus,SPI and UART	1	BB
10	4	Architecture of ARM processor	1	BB
11		ARM instruction set	1	BB
12	5	Architecture of CORTEX processor	1	BB
13		Architecture of OMAP processor	1	BB
14		Features of CORTEX processor	1	BB

TEXTBOOKS:

1.Advanced Microprocessors and Peripherals– .K.RayandK.M.Bhurchandani,MHE,2nd Edition 2006.

2. The 8052 microcontroller,Kenneth.J.Ayala , Cengaga Leaning, 3rd Ed.

3. ARM System Developer's guide, Andrew N SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier, 2012

REFERENCEBOOKS:

1.Microprocessor and interfacing, D.V.Hall,MGH,2nd Edition 2006.

2.Introduction to Embedded Systems,Shibu K.V,MHE,2009.

3.The8051Microcontrollers,ArchitectureandProgrammingandApplications-K.UmaRao,Andhe Pallavi,Pearsons,2009.

Course Title	MICROPROCESSORS AND MICROCONTROLLERS
Course Code	EC501PC
Programme	B.Tech
Year & Semester	III year I-semester, A sec
Regulation	R18
Course Faculty	VENU IPPALAPALLI, Assistant Professor, ECE

Slow learners:

S No	Roll no	No of backlogs	Internal-I Status	Internal-II Status
1	20X31A0401	4	19	21
2	20X31A0403	5	15	19
3	20X31A0406	4	18	21
4	20X31A0407	3	20	21
5	20X31A0408	3	14	21
6	20X31A0410	5	18	19
7	20X31A0411	4	20	21
8	20X31A0412	5	15	21
9	20X31A0413	4	19	21
10	20X31A0418	8	15	14
11	20X31A0419	4	22	19
12	20X31A0423	3	21	21
13	20X31A0427	3	17	21
14	20X31A0428	4	21	23
15	20X31A0430	4	23	19
16	20X31A0431	5	18	21
17	20X31A0433	3	16	22
18	20X31A0435	3	16	20
19	20X31A0436	5	17	21

20	20X31A0440	4	22	22
22	20X31A0445	4	21	21
23	20X31A0447	3	21	21
24	20X31A0450	4	21	21
25	20X31A0453	4	22	21
26	20X31A0454	5	15	21
27	20X31A0455	4	18	19
28	20X31A0456	5	15	21
30	20X31A0458	3	21	22
31	20X31A0462	3	23	20

Advanced learners

S.NO	ROLL.NO.	GATE MATERIAL
1	20X31A0404	Machine instructions and addressing modes, ALU, data-path, control unit, instruction pipelining
2	20X31A0409	
3	20X31A0415	
4	20X31A0416	
5	20X31A0420	
6	20X31A0421	
7	20X31A0422	
8	20X31A0425	
9	20X31A0432	
10	20X31A0434	
11	20X31A0437	
12	20X31A0438	
13	20X31A0439	
14	20X31A0442	
15	20X31A0444	
16	20X31A0449	
17	20X31A0452	
18	20X31A0459	

19	20X31A0460	

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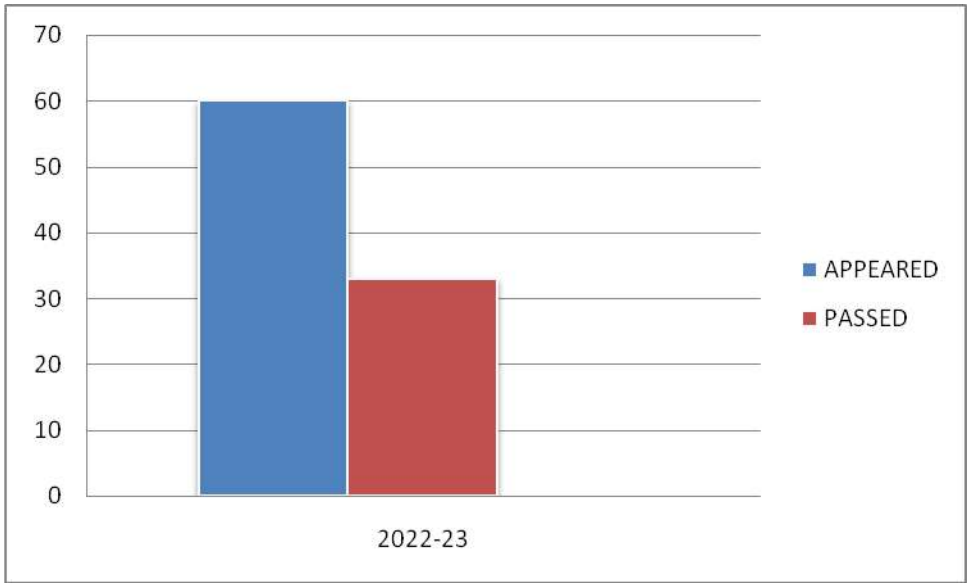
Website: https://siiet.ac.in/

BATCH ECE-III BTECH I SEM ECE-A RESULT ANALYSIS

ACADAMIC YEAR	COURSE NAME	NUMBER OF STUDENTS		QUESTION PAPER SETTING		PASS%
		APPEARED	PASSED	INTERNAL	EXTERNAL	
2022-23	MICROPROCESSORS AND MICROCONTROLLERS	60	33	COURSE FACULTY	JNTUH	55

MICROPROCESSORS AND MICROCONTROLLERS (C311) RESULT ANALYSIS



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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

REMEDIAL CLASSES TIME TABLE

A.Y 2022-23 **SEMESTER-I**

BRANCH/ SEC	MON 4.00 PM-5.00 PM	TUE 4.00 PM-5.00 PM	WED 4.00 PM-5.00 PM	THUR 4.00 PM-5.00 PM	FRI 4.00 PM-5.00 PM
II ECE-A	EDC	NATL	DSD	PTSP	SS
II ECE-B	NATL	DSD	PTSP	SS	EDC
III ECE-A	MPMC	DCCN	CS	BEFA	EMI
III ECE-B	DCCN	CS	BEFA	EMI	MPMC
III ECE-C	CS	BEFA	EMI	MPMC	DCCN
IV ECE-A	MW&OC	DIP	PPLE	NS&C	JAVA
IV ECE-B	DIP	PPLE	NS&C	JAVA	MW&OC
IV ECE-C	PPLE	NS&C	JAVA	MW&OC	DIP

Head of the Department
Electronics and Communication Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH,
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510.

PRINCIPAL
Sri Indu Institute of Engineering & Tech.
Sheriguda(Vill), Ibrahimpatnam,
R.R. Dist. Telangana -501 510.

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty : IPPALAPALLI VENU Academic Year: 2022-23

Branch & Section: ECE - A Examination: I Internal

Course Name: MICROPROCESSORS & MICROCONTROLLERS Year: III Semester: I

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj1	A1
Max. Marks ==>		5		5		5		5		10	5
1	20X31A0401	3						3		8	5
2	20X31A0402	5						4		9	5
3	20X31A0403	2						4		4	5
4	20X31A0404			4				4		9	5
5	20X31A0405	2						4		9	5
6	20X31A0406	2		2						9	5
7	20X31A0407			3		3				9	5
8	20X31A0408			1		2				6	5
9	20X31A0409	5		5						9	5
10	20X31A0410			2		2				9	5
11	20X31A0411	3		3						9	5
12	20X31A0412			1						9	5
13	20X31A0413	2		3						9	5
14	20X31A0414			4				4		9	5
15	20X31A0415	4						5		9	5
16	20X31A0416			2		2				7	5
17	20X31A0417			5		5				9	5
18	20X31A0418	1		2						7	5
19	20X31A0419	5		3						9	5
20	20X31A0420			3		4				5	5
21	20X31A0421			1				1		9	5
22	20X31A0422	3				5				9	5
23	20X31A0423			3		4				9	5
24	20X31A0424			3		2				9	5
25	20X31A0425	4				4				9	5
26	20X31A0426			2		3				9	5
27	20X31A0427			1				2		9	5
28	20X31A0428	3		4						9	5
29	20X31A0429	5				5				9	5
30	20X31A0430					4		5		9	5
31	20X31A0431			1		3				9	5
32	20X31A0432	5				5				9	5
33	20X31A0433			1		2				8	5
34	20X31A0434	4				5				9	5
35	20X31A0435			2				3		6	5
36	20X31A0436	3						3		6	5
37	20X31A0437	4		4						9	5
38	20X31A0438			4		4				10	5
39	20X31A0439			4				4		9	5

40	20X31A0440			4				4		9	5
41	20X31A0441	5						5		9	5
42	20X31A0442	5		5						9	5
43	20X31A0444			5		5				9	5
44	20X31A0445					4		5		7	5
45	20X31A0446			5		4				7	5
46	20X31A0447	3						4		9	5
47	20X31A0448			5		3				10	5
48	20X31A0449	5						5		10	5
49	20X31A0450			4		3				9	5
50	20X31A0451	4						4		9	5
51	20X31A0452					5		5		9	5
52	20X31A0453			5		4				8	5
53	20X31A0454	2				4				4	5
54	20X31A0455	3				1				9	5
55	20X31A0456	3				3				4	5
56	20X31A0458	3		4						9	5
57	20X31A0459			4		4				9	5
58	20X31A0460			4				5		9	5
59	20X31A0461	4				5				9	5
60	20X31A0462					4		5		9	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		23	0	25	0	25	0	20	0	56	60
Number of students attempted		29	0	37	0	31	0	22	0	60	60
Percentage of students scored more than target		79%		68%		81%		91%		93%	100%

CO Mapping with Exam Questions:

CO - 1	Y		Y				Y		Y	Y
CO - 2					Y				Y	Y
CO - 3									Y	Y
CO - 4										
CO - 5										
CO - 6										

% Students Scored >Target %	79%		68%		81%		91%		93%	100%

CO Attainment based on Exam Questions:

CO - 1	79%		68%				91%		93%	100%
CO - 2					81%				93%	100%
CO - 3									93%	100%
CO - 4										
CO - 5										

CO - 6										

CO	Subj	obj	Asgn	Overall	Level
CO-1	79%	93%	100%	91%	3.00
CO-2	81%	93%	100%	91%	3.00
CO-3		93%	100%	97%	3.00
CO-4					
CO-5					
CO-6					

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal 1 Examination) = **3.00**

Faculty Signature

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (Internal Examination-2)

Name of the faculty : IPPALAPALLI VENU Academic Year: 2022-23

Branch & Section: ECE - A Examination: II Internal

Course Name: MICROPROCESSORS & MICROCONTROLLERS Year: III Semester: I

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj2	A2
Max. Marks ==>		5		5		5		5		10	5
1	20X31A0401					4		4		8	5
2	20X31A0402					3		5		9	5
3	20X31A0403	3				4				7	5
4	20X31A0404	4				4				8	5
5	20X31A0405	5		4						7	5
6	20X31A0406			4		4				8	5
7	20X31A0407	4		3						9	5
8	20X31A0408			3		5				8	5
9	20X31A0409	5				2				8	5
10	20X31A0410	4				3				7	5
11	20X31A0411	4		4						8	5
12	20X31A0412			5		4				7	5
13	20X31A0413	3		5						8	5
14	20X31A0414	2		5						8	5
15	20X31A0415	3		5						7	5
16	20X31A0416			4		4				8	5
17	20X31A0417			4				5		9	5
18	20X31A0418					2		3		4	5
19	20X31A0419	3						4		7	5
20	20X31A0420			5				3		8	5
21	20X31A0421			4				4		7	5
22	20X31A0422	4						5		8	5
23	20X31A0423	3				5				8	5
24	20X31A0424	3		4						7	5
25	20X31A0425			3				5		8	5
26	20X31A0426	5				2				7	5
27	20X31A0427	3				5				8	5
28	20X31A0428			5				4		9	5
29	20X31A0429	3				5				8	5
30	20X31A0430			3		4				7	5
31	20X31A0431	3				5				8	5
32	20X31A0432			5				4		7	5
33	20X31A0433	4				4				9	5
34	20X31A0434			3				4		8	5
35	20X31A0435	5		3						7	5
36	20X31A0436			4				4		8	5
37	20X31A0437	4				3				7	5
38	20X31A0438			3				5		8	5
39	20X31A0439	3				4				9	5
40	20X31A0440			4				4		9	5
41	20X31A0441	4				5				8	5
42	20X31A0442			4				4		7	5
43	20X31A0444			4				3		7	5

44	20X31A0445	4				4				8	5
45	20X31A0446	4		3						7	5
46	20X31A0447			4				4		8	5
47	20X31A0448					4		4		8	5
48	20X31A0449			4		3				7	5
49	20X31A0450	5				3				8	5
50	20X31A0451			4				5		7	5
51	20X31A0452					4		4		8	5
52	20X31A0453	4		3						9	5
53	20X31A0454	4				4				8	5
54	20X31A0455			4		3				7	5
55	20X31A0456			4				4		8	5
56	20X31A0458			5				4		8	5
57	20X31A0459	4				4				9	5
58	20X31A0460	4						3		8	5
59	20X31A0461			4		4				7	5
60	20X31A0462	4				3				8	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		30	0	34	0	28	0	24	0	59	60
Number of students attempted		31	0	34	0	31	0	24	0	60	60
Percentage of students scored more than target		97%		100%		90%		100%		98%	100%

CO Mapping with Exam Questions:

CO - 1										
CO - 2										
CO - 3		Y							Y	Y
CO - 4	Y								Y	Y
CO - 5			Y						Y	Y
CO - 6					Y		Y		Y	Y

CO Attainment based on Exam Questions:

CO - 1										
CO - 2										
CO - 3									98%	100%
CO - 4	97%								98%	100%
CO - 5			100%						98%	100%
CO - 6					90%		100%		98%	100%

CO	**Subj**	obj	Asgn	Overall	Level
CO-1					
CO-2					
CO-3		98%	100%	99%	3.00
CO-4	97%	98%	100%	98%	3.00
CO-5	100%	98%	100%	99%	3.00

Attainment Level	
1	40%
2	50%
3	60%

CO-6	95%	98%	100%	98%	3.00

Attainment (Internal Examination-2) = **3.00**

Faculty Signature

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty : IPPALAPALLI VENU Academic Year: 2022-23

Branch & Section: ECE - A Year / Semester: III / I

Course Name: MICROPROCESSORS & MICROCONTROLLERS

S.No	Roll Number	Marks Secured
1	20X31A0401	16
2	20X31A0402	6
3	20X31A0403	-1
4	20X31A0404	38
5	20X31A0405	28
6	20X31A0406	18
7	20X31A0407	33
8	20X31A0408	12
9	20X31A0409	45
10	20X31A0410	14
11	20X31A0411	14
12	20X31A0412	4
13	20X31A0413	28
14	20X31A0414	35
15	20X31A0415	39
16	20X31A0416	16
17	20X31A0417	35
18	20X31A0418	-1
19	20X31A0419	14
20	20X31A0420	16
21	20X31A0421	32
22	20X31A0422	36
23	20X31A0423	18
24	20X31A0424	15
25	20X31A0425	26
26	20X31A0426	19
27	20X31A0427	17
28	20X31A0428	26
29	20X31A0429	26
30	20X31A0430	30
31	20X31A0431	14
32	20X31A0432	29
33	20X31A0433	16
34	20X31A0434	34
35	20X31A0435	17
Max Marks		75

S.No	Roll Number	Marks Secured
36	20X31A0436	11
37	20X31A0437	30
38	20X31A0438	44
39	20X31A0439	37
40	20X31A0440	7
41	20X31A0441	33
42	20X31A0442	43
43	20X31A0444	34
44	20X31A0445	4
45	20X31A0446	35
46	20X31A0447	26
47	20X31A0448	7
48	20X31A0449	57
49	20X31A0450	8
50	20X31A0451	39
51	20X31A0452	34
52	20X31A0453	34
53	20X31A0454	1
54	20X31A0455	17
55	20X31A0456	5
56	20X31A0458	14
57	20X31A0459	41
58	20X31A0460	30
59	20X31A0461	31
60	20X31A0462	13

Class Average mark	23
Number of students performed above the target	31
Number of successful students	60

Attainment Level	% students
1	40%
2	50%

Percentage of students scored more than target	52%
Attainment level	**2**

3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Outcome Attainment

Name of the faculty IPPALAPALLI VENU
Branch & Section: ECE - A
Course Name: MICROCONTROLLERS

Academic Year: 2022-23
Examination: I Internal
Year: III
Semester: I

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00		3.00	2.00	2.25
CO2	3.00		3.00	2.00	2.25
CO3	3.00	3.00	3.00	2.00	2.25
CO4		3.00	3.00	2.00	2.25
CO5		3.00	3.00	2.00	2.25
CO6		3.00	3.00	2.00	2.25
Internal & University Attainment:			3.00	2.00	
Weightage			25%	75%	
O Attainment for the course (Internal, Universi			0.75	1.50	
CO Attainment for the course (Direct Method)			2.25		

Overall course attainment level **2.25**

Faculty Signature

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Program Outcome Attainment (from Course)

Name of Faculty: IPPALAPALLI VENU Academic Year: 2022-23
Branch & Section: ECE - A Year: III
Course Name: MICROPROCESSORS & MICROCONTI Semester: I

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	1	-	-	-	-	-	-	-	3	2	1
CO2	3	2	3	3	-	-	-	-	-	-	-	2	2	1
CO3	3	3	2	3	-	-	-	-	-	-	2	2	3	3
CO4	3	3	2	3	-	-	-	-	-	-	-	3	3	3
CO5	3	3	3	2	-	-	-	-	-	-	3	3	3	3
CO6	2	2	1	3	-	-	-	-	-	-	-	2	3	3
Course	**2.83**	**2.5**	**2.17**	**2.5**							**2.5**	**2.5**	**2.67**	**2.33**

CO	**Course Outcome Attainment**
CO1	2.25
CO2	2.25
CO3	2.25
CO4	2.25
CO5	2.25
CO6	2.25
Overall course attainment level	**2.25**

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainment	**2.12**	**1.88**	**1.63**	**1.88**							**1.88**	**1.88**	**2.00**	**1.75**

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)

Faculty Signature

ASSIGNMENTS AND REGISTERS

Assignment 1 script link:

https://drive.google.com/file/d/1zO5VlOZY1knNNnPjIwO2WLjkU6eA1d8R/view?usp=sharing

Assignment 2 script link:

https://drive.google.com/file/d/1g9t_cJC9jChw8LOXnvOlkjgkjQZVqs4I/view?usp=sharing

Attendance register link:

https://drive.google.com/file/d/16TAXsQ4BddJaJA_4b1AQEInZ7kdvcDV8/view?usp=sharing