COURSE FILE

ON

COMPILER DESIGN

Course Code – CS601PC

III B.Tech II-SEMESTER
A.Y.: 2022-2023

Prepared by

Dr. SasiKumar D
Associate Professor

Sri Indu Institute of Engineering & Technology

Recognized Under 2(f) of UGC Act 1956
Approved by AICTE, New Delhi
Affiliated to JNTUH, Hyderabad.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Academic Year	2022-2023
Course Title	COMPILER DESIGN
Course Code	**CS601PC**
Programme	B.Tech
Year & Semester	III year II-semester
Branch & Section	CSE-A
Regulation	R18
Course Faculty	Dr.Sasikumar D, AssociateProfessor

Index of Course File

S. No.	Name of the content
1	Institute vision and mission
2	Department vision and mission /PEO
3	POs /PSOs
4	Course Syllabus with Structure
5	Course Outcomes (CO)
6	Mapping CO with PO/PSO; Course with PO/PSO with Justification
7	Academic Calendar
8	Time table - highlighting your course periods including tutorial
9	Lesson plan with number of hours/periods, TA/TM, Text/Reference book
10	Web references
11	Lecture notes
12	List of Power point presentations / Videos
13	University Question papers
14	Internal Question papers, Key with CO and BT
15	Assignment Question papers mapped with CO and BT
16	Result Analysis to identify weak and advanced learners - 3 times in a semester
17	Result Analysis at the end of the course
18	Remedial class for weak students - schedule and evidences
19	Advance Learners- Engagement documentation
20	CO, PO/PSO attainment sheets
21	Attendance register (Theory/Tutorial/Remedial) - Teacher/Course delivery record; Continuous evaluation
22	Course file (Digital form)

Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510.
Campus Ph:9640590999, 9347187999, 8096951507.

https://siiet.ac.in

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To continuous assess of teaching-learning process through institute-industry

   collaboration..

IM3: To be a centre of excellence for innovative and emerging fields in technology

   development with state-of-art facilities to faculty and students fraternity.

IM4: To create an enterprising environment to ensure culture, ethics and social responsibility

   among the stakeholders

Sri Indu Institute of
Engineering & Technology

Recognized Under 2(f) of UGC Act 1956
Approved by AICTE, New Delhi
Affiliated to JNTUH, Hyderabad.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a prominent knowledge hub for learners, strive for educational excellence with innovative and industrial techniques so as to meet the global needs.

Mission:

DM1 : To provide ambience that enhances innovations, problem solving skills, leadership qualities, decision making, team-spirit and ethical responsibilities.

DM2 : To impart quality education with professional and personal ethics, so as to meet the challenging technological needs of the industry and society.

DM3 : To provide academic infrastructure and develop linkage with the world class organizations to strengthen industry-academia relationships for learners.

DM4 : To provide and strengthen new concepts of research in the thrust area of Computer Science and Engineering to reach the needs of Government and Society.

B. Ratna Kaul
Computer Science & Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH.
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 1C.

PRINCIPAL
Sri Indu Institute of Engineering & Tech.
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

https://siiet.ac.in

Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510.
Campus Ph:9640590999, 9347187999, 8096951507.

Sri Indu Institute of
Engineering & Technology

Recognized Under 2(f) of UGC Act 1956
Approved by AICTE, New Delhi
Affiliated to JNTUH, Hyderabad.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

PROGRAM EDUCATIONAL OBJECTIVES

PEO1: To develop trained graduates with strong academic and technical skills of modern computer science and engineering.

PEO2: To promote trained graduates with leadership qualities and the ability to solve real time problems using current techniques and tools in interdisciplinary environment.

PEO3: To motivate the graduates towards lifelong learning through continuing education and professional development.

PROGRAM SPECIFIC OUTCOMES

PSO1 : **Professional Skills:** To implement computer programs of varying complexity in the areas related to Web Design, Cloud Computing, Network Security and Artificial Intelligence.

PSO2: **Problem-Solving Skills**: To develop quality products using open ended programming environment.

Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510.
Campus Ph:9640590999, 9347187999, 8096951507.

https://siiet.ac.in

Sri Indu Institute of Engineering & Technology

Recognized Under 2(f) of UGC Act 1956
Approved by AICTE, New Delhi
Affiliated to JNTUH, Hyderabad.

PROGRAMME OUTCOMES (POs)

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO6: **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Main Road, Sheriguda, Ibrahimpatnam, R.R. Dist. 501 510.
Campus Ph: 9640590999, 9347187999, 8096951507.

https://siiet.ac.in

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITYHYDERABAD
B.Tech. in COMPUTER SCIENCE AND ENGINEERING
III YEAR COURSE STRUCTURE AND SYLLABUS(R18)
Applicable From 2018-19 Admitted Batch

III YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	CS501PC	Formal Languages & Automata Theory	3	0	0	3
2	CS502PC	Software Engineering	3	0	0	3
3	CS503PC	Computer Networks	3	0	0	3
4	CS504PC	Web Technologies	3	0	0	3
5	CS515PE	Professional Elective -I	3	0	0	3
6		Professional Elective -II	3	0	0	3
7	CS505PC	Software Engineering Lab	0	0	3	1.5
8	CS506PC	Computer Networks & Web Technologies Lab	0	0	3	1.5
9	EN508HS	Advanced Communication Skills Lab	0	0	2	1
10	*MC510	Intellectual Property Rights	3	0	0	0
		Total Credits	21	0	8	22

III YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	CS601PC	Machine Learning	3	1	0	4
2	CS602PC	Compiler Design	3	1	0	4
3	CS603PC	Design and Analysis of Algorithms	3	1	0	4
4		Professional Elective – III	3	0	0	3
5		Open Elective-I	3	0	0	3
6	CS604PC	Machine Learning Lab	0	0	3	1.5
7	CS605PC	Compiler Design Lab	0	0	3	1.5
8		Professional Elective-III Lab	0	0	2	1
9	*MC609	Environmental Science	3	0	0	0
		Total Credits	18	3	8	22

CS602PC: COMPILER DESIGN

III Year B.Tech. CSE II-Sem

L T P C
3 1 0 4

Prerequisites

1. A course on "Formal Languages and Automata Theory
2. A course on "Computer Organization and architecture"
3. A course on" Computer Programming and Data Structures"

Course Objectives:

Introduce the major concepts of language translation and compiler design and impart the knowledge of practical skills necessary for constructing a compiler.

Topics include phases of compiler, parsing, syntax directd translation, type checking use of symbol tables, code optimization techniques, intermediate code generation, code generation and data flow analysis.

Course Outcomes:

- Demonstratetheabilitytodesignacompilergivenasetoflanguagefeatures.
- Demonstratethetheknowledgeofpatterns,tokens&regularexpressionsforlexical analysis.
- Acquireskillsinusinglextool&yacctoolfordevleopingascannerandparser.
- Design and implement LL and LR parsers
- Designalgorithmstodocodeoptimizationinordertoimprovetheperformanceof aprogramin terms of space and time complexity.
- Design algorithms to generate machine code.

UNIT-I

Introduction: The structure of a compiler, the science of building a compiler, programming language basics

Lexical Analysis: The Role of the Lexical Analyzer, Input Buffering, Recognition of Tokens, The Lexical AnalyzerGeneratorLex,FiniteAutomata,FromRegularExpressionstoAutomata,Designofa Lexical-Analyzer Generator, Optimization of DFA-Based Pattern Matchers**.**

UNIT-II

Syntax Analysis: Introduction, Context-Free Grammars, Writing a Grammar, Top-Down Parsing, Bottom-Up Parsing, Introduction to LR Parsing: Simple LR, More Powerful LR Parsers, Using Ambiguous Grammars and Parser Generators.

UNIT-III

Syntax-DirectedTranslation: Syntax-Directed Definitions, EvaluationOrdersforSDD's, Applications of Syntax-Directed Translation, Syntax-Directed Translation Schemes, Implementing L-Attributed SDD's.

Intermediate-Code Generation: Variants of Syntax Trees, Three-Address Code, Types and Declarations, Type Checking, Control Flow, Switch-Statements, Intermediate Code for Procedures.

UNIT-IV

Run-Time Environments: Stack Allocation of Space, Access to Nonlocal Data on the Stack, Heap Management, Introduction to Garbage Collection, Introduction to Trace-Based Collection.

Code Generation: Issues in the Design of a Code Generator ,The Target Language**,** Addresses int he Target Code, BasicBlocksandFlowGraphs, Optimizationof BasicBlocks, ASimpleCodeGenerator, PeepholeOptimization,RegisterAllocationandAssignment,DynamicProgrammingCode-Generation.

UNIT-V

Machine-Independent Optimization: The Principal Sources of Optimization ,IntroductiontoData-Flow Analysis, Foundations of Data-Flow Analysis, Constant Propagation, Partial-Redundancy Elimination, Loops in Flow Graphs.

TEXTBOOK:

1. Compilers: Principles, Techniques and Tools, Second Edition, Alfred V. Aho, Monica S. Lam, Ravi Sethi, Jeffry D. Ullman**.**

REFERENCEBOOKS:

1. Lex&Yacc–JohnR.Levine,TonyMason,DougBrown,O'reilly
2. CompilerConstruction,Louden,Thomson.

Department of Computer Science and Engineering

Course Outcomes

Course: COMPILER DESIGN (C322))   **Class: III – II SEM – A - Section**

After completing this course the student will be able to:

C322.1   Describe structure of a compiler and basics of programming languages (Knowledge)

C322.2   Design Lexical analyzer generator by using regular expressions and finite automata.(Synthesis)

C322.3   Design and implement LL and LR parsers and use YACC Tool for developing a parser.(Synthesis)

C322.4   Explain the applications of SDT and different types of intermediate-code generation (Comprehension)

C322.5   Identify the storage organization used to support the run-time environment ofa program and effectively generate machine codes(Knowledge).

C322.6   Apply the several algorithms for collecting and optimizing the information using data flow analysis(Application).

Mapping of course outcomes with program outcomes:

High -3   Medium -2   Low-1

PO/PSO/CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C322.1	3	-	-	-	-	-	-	-	-	-	3	-	3	1
C322.2	2	2	-	2	3	-	-	-	-	-	3	-	2	3
C322.3	2	2	-	2	3	-	-	-	-	-	2	-	2	2
C322.4	2	-	-	2	3	-	-	-	-	-	1	-	1	2
C322.5	-	3	-	1	2	-	-	-	-	-	-	-	2	3
C322.6	-	3	-	-	-	-	-	-	1	-	-	-	-	1
C322	2.25	2.5	-	1.7	2.75	-	-	-	1	-	2.25	-	2	2

Department of Computer Science and Engineering
CO – PO / PSO Mapping Justification

Course: COMPILER DESIGN **(C322)**   **Class: III – II SEM CSE-A Section**

PROGRAMME OUTCOMES (POs):

PO1 **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 **Problem analysis:** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO4 **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO9 **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO11 **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PROGRAM SPECIFIC OUTCOMES (PSOs):

PSO1 **Professional Skills:** The ability to implement computer programs of varying complexity in the areas related to web design, cloud computing and networking.

PSO2 **Problem-Solving Skills:** The ability to develop quality products using open ended programming environment.

C322.1   Describe structure of a compiler and basics of programming languages (Knowledge)

	Justification
PO1	Gain knowledge on Phases of a compiler.(level 3)
PO11	Gain knowledge on programming language basics for project management.(level 3)
PSO1	Gain knowledge on design of compiler.(level 3)
PSO2	Recognise the concepts to develop products(level 1)

C322.2   Design Lexical analyzer generator by using regular expressions and finite automata.(Synthesis)

	Justification
PO1	Gain knowledge ondevelopment of lexical analyzer phase of compiler.(level 3)
PO2	Designingof lexical analyzer should know the basics of finite automata.(level 2)
PO4	Recognizing the knowledge of constructing finite automata from regular expression. (level 2)
PO5	Select LEX tool to design a lexical analyzer phase of a compiler(level 3)
PO11	Demonstrate knowledge on LEX tool.(level 3)
PSO1	Ability to implement computer programs for Lexical Analyzer phase of compiler.(level 2)
PSO2	Ability to develop compiler product.(level 3)

C322.3   Design and implement LL and LR parsers and use YACC Tool for developing a parser.(Synthesis)

	Justification
PO1	Gain knowledge ontop down and bottom up parsing.(level 2)
PO2	Designing of syntax analysis should know the basics of context free grammar.(level 2)
PO4	Recognizing the knowledge of LL(1) grammars and LR grammars(level 2)
PO5	Select YACC tool to design LALR bottom up parser.(level 3)
PO11	Demonstrate knowledge on YACC tool.(level 2)
PSO1	Ability to implement computer programs for Syntax analysis phase of a compiler. (level 2)
PSO2	Ability to develop compiler product.(level 2)

C322.4 **Explain the applications of SDT and different types of intermediate-code generation (Comprehension)**

	Justification
PO1	Gain knowledge about SDT and intermediate code generation.(level 2)
PO4	Express problem analysis using SDT and intermediate code generation.(level 2)
PO5	Design semantic analysis phase of a compiler(level 3)
PO11	Explain the applications of SDT(level 1)
PSO1	Ability to implement computer programs for Semantic analysis phase of a compiler. (level 1)
PSO2	Ability to develop compiler product.(level 2)

C322.5 **Identify the storage organization used to support the run-time environment of a program and effectively generate machine codes (Knowledge).**

	Justification
PO2	Analyze the storage organization.(level 3)
PO4	Analyze machine code generation efficiently .(level 1)
PO5	Gain knowledge on Heap Management and Dynamic Programming Code-Generation. (level 2)
PSO1	Ability to optimize storage organization and effectively generate machine codes.(level 2)
PSO2	Ability to develop compiler product.(level 3)

C322.6 **Apply the several algorithms for collecting and optimizing the information using data flow analysis (Application).**

	Justification
PO2	Apply the several algorithms for data-flow analysis.(level 3)
PO9	Implement several algorithms for data flow analysis as a team.(level 1)
PSO2	Ability to develop compiler product.(level 1)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
ACADEMIC CALENDAR 2022-23
B. Tech./B. Pharm. III YEAR I & II SEMESTERS

I SEM

S. No	Description	Duration	
		From	To
1	Commencement of I Semester classwork	09.09.2022	
2	1st Spell of Instructions (including Dussehra Recess)	09.09.2022	10.11.2022 (9 Weeks)
3	Dussehra Recess	03.10.2022	08.10.2022 (1 Week)
4	First Mid Term Examinations	11.11.2022	17.11.2022 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	24.11.2022	
6	2nd Spell of Instructions	18.11.2022	12.01.2023 (8 Weeks)
7	Second Mid Term Examinations	16.01.2023	21.01.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	23.01.2023	28.01.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	30.01.2023	
10	End Semester Examinations	30.01.2023	11.02.2023 (2 Weeks)

Note: No. of Working/ instructional days: 92

II SEM

S. No	Description	Duration	
		From	To
1	Commencement of II Semester classwork	13.02.2023	
2	1st Spell of Instructions	13.02.2023	08.04.2023 (8 Weeks)
3	First Mid Term Examinations	10.04.2023	15.04.2023 (1 Week)
4	Submission of First Mid Term Exam Marks to the University on or before	22.04.2023	
5	2nd Spell of Instructions (including Summer Vacation)	17.04.2023	24.06.2023 (10 Weeks)
6	**Summer Vacation**	15.05.2023	27.05.2023 (2 Weeks)
7	Second Mid Term Examinations	26.06.2023	01.07.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	03.07.2023	08.07.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	08.07.2023	
10	End Semester Examinations	10.07.2023	22.07.2023 (2 Weeks)

Note: No. of Working/ instructional days: 90

REGISTRAR

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC)
Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956
(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

TIME TABLE FOR A.Y 2022-23

Class: III-B. Tech CSE -A   Semester: II   LH. NO: A-201   W.E.F:13-02-2023

Period/ Day	1 9:40-10:30	2 10:30-11:20	3 11:20-12:10	4 12:10-1:00	1:00-1:30	5 1:30-2:20	6 2:20-3:10	7 3:10-4:00
Monday	DAA	CD	LIB	STM	L U N C H	STM LAB(BATCH-I)/CD LAB(BATCH-II)		
Tuesday	STM	DAA	DAA/ML(T)	ML		FIOT	STM	SPORTS
Wednesday	FIOT	CD	INT	STM		ML/CD(T)	CO-C/SS/DAA	
Thursday	FIOT	ML LAB(BATCH-I)/STM LAB(BATCH-II)				DAA	CD	STM
Friday	CD	COUN	ML	FIOT		ML LAB(BATCH-II)/CD LAB(BATCH-I)		
Saturday	CD	FIOT	CD/DAA(T)	DAA		ML		DAA

(T) – Tutorial (concern faculty)

Subject Code	Subject Name	Name of the Faculty	Subject Code	Subject Name	Name of the Faculty
CS601PC	Machine Learning	Mrs N Shilpa		Fundamentals of Internet of Things	Mrs. M.Sruthi
CS602PC	Compiler Design	Dr. Sasikumar D	CS604PC	Machine Learning Lab	Mrs N Shilpa/ K.Manmadha / V. Divya
CS603PC	Design and Analysis of Algorithms	Mr A Vijay Kumar	CS605PC	Compiler Design Lab	Dr. Sasikumar D / Ms K Mounika/ P.Swathi
CS615PE	Software Testing Methodologies	Mrs E Rupa	CS625PE	Software Testing Methodologies Lab	Mrs E Rupa/ Mrs S Akhila / Mrs. M.Sruthi
	CO-C/SS/DAA/ Cyber Security	Mrs. M.Sruthi	LIB	Library	Mrs K.Manmadha
Sports	Sports	Mr A Vijay Kumar	COUN	Counselling	Mrs.A.Sudha
Internet	Internet	Mrs.A.Sudha	CS601PC	Machine Learning	Mr M Dattatreya Goud (Adjunct)
			MC609	Environmental Science(LE)	Mr D Nagaraju

Class In-Charge : Mrs N Shilpa   Mentor 1 : Mrs N Shilpa   Mentor 2: Mrs E Rupa

Class In-Charge

Computer Science & Engg. Dept.
HOD
SRI INDU INSTITUTE OF ENGG & TECH.
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 1C

PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(V), Ibrahimpatnam
R.R. Dist. Telangana
PRINCIPAL

LESSON PLAN

Course Title	COMPILER DESIGN
Course Code	CS601PC
Programme	B.Tech
Year & Semester	III-year II-semester
Regulation	R18
Course Faculty	MrDr.Sasikumar D, AssociateProfessor , CSE

S.NO	Unit	Topic	Number of Sessions Planned	Teaching Method/Aids	Reference
1.		Language Processors	1	Black Board	T1
2.		The Structure of a Compiler	2	Black Board	T1
3.		The Science of Building a Compiler	1	Black Board	T1
4.		Programming Language Basics.	1	Black Board	T1
5.		**Tutorial1**(Language Processors, The Structure of a Compiler)	1	Black Board	T1
6.	1	The Role of the Lexical Analyzer	2	Black Board	T1
7.		Input Buffering	1	Black Board	T1
8.		Recognition ofTokens	2	Black Board	T1
9.		**Tutorial2**(The Role of the Lexical Analyzer ,Input Buffering)	1	Black Board	T1
10		The Lexical-Analyzer Generator Lex	1	Black Board	T1
11		Finite Automata	1	Black Board	T1
12		Regular Expressions toAutomata	2	Black Board	T1
13		Design of a Lexical-Analyzer Generator	1	Black Board	T1
14		**Tutorial3**(The Lexical-Analyzer Generator Lex, Regular Expressions toAutomata, Design of a Lexical-Analyzer Generator)	1	Black Board	T1
15		Optimization of DFA-Based PatternMatchers	2	Black Board	T1
16		Introduction, Context-Free Grammars	1	Black Board	T1
17		Writing a Grammar	2	Black Board	T1
18	2	**Tutorial4**(Optimization of DFA-Based PatternMatchers ,Context-Free Grammars)	1	Black Board	T1
19		Top-Down Parsing	5	Black Board	VR1
20		**Tutorial5**(Design of a Lexical-Analyzer Generator, Context-Free Grammars, Top-DownParsing)	1	Black Board	T1
21		Bottom-Up Parsing, Introduction to LR Parsing	2	Black Board	T1
22		Simple LR	1	Black Board	T1
23		**Tutorial6**(SLR)	1	Black Board	T1
24		More Powerful LRParsers	2	Black Board	T1

25		Using Ambiguous Grammars	1	Black Board	T1
26		Parser Generators.	2	Black Board	T1
27		**Tutorial7**(More Powerful LRParsers, Parser Generators)	1	Black Board	T1
28		Syntax-Directed Definitions	1	Black Board	T1
29		Evaluation Orders for SDD's	2	Black Board	T1
30		Applications of Syntax-Directed Translation	2	Black Board	T1
31		**Tutorial8**(Syntax-Directed Definitions)	1	Black Board	T1
32		Syntax-Directed Translation Schemes	3	Black Board	T1
33		Implementing L-Attributed SDD's.	1	Black Board	T1
34		Variants of Syntax Trees	1	Black Board	T1
35	3	**Tutorial9**(Variants of syntax tree)	1	Black Board	T1
36		Three-Address Code	2	Black Board	T1
37		Types andDeclarations	1	Black Board	T1
38		Type Checking	2	Black Board	T1
39		**Tutorial10**(Three Address Code)	1	Black Board	T1
40		Control Flow	1	Black Board	T1
41		Back patching	1	Black Board	T1
42		Switch-Statements	1	Black Board	T1
43		Intermediate Code for Procedures	2	Black Board	T1
44		**Tutorial11**(Back patching, IntermediateCode for Procedures)	1	Black Board	T1
45		Storage organization	1	Black Board	T1
46		Stack Allocation of Space	1	Black Board	T1
47		Access to Nonlocal Data on the Stack,	1	Black Board	T1
48	4	Heap Management	1	Black Board	T1
49		Introduction to Garbage Collection	1	Black Board	T1
50		**Tutorial12**(Stack Allocation of Space, Heap Management)			
51		Introduction to Trace-Based Collection.	1	Black Board	T1
52		Issues in the Design of a Code Generator	1	Black Board	T1
53		The Target Language	1	Black Board	T1
54		Addresses in the Target Code, Basic Blocks and Flow Graphs	1	Black Board	T1
55		Optimization of Basic Blocks	1	Black Board	T1
56		**Tutorial13**(Basic Blocks and Flow Graphs, Optimization of Basic Blocks)	1	Black Board	T1
57		A Simple Code Generator, Peephole Optimization	1	Black Board	T1
58		Register Allocation and Assignment	1	Black Board	T1
59		Dynamic Programming Code-Generation.	1	Black Board	T1
60		The Principal Sources of Optimization	1	Black Board	T1
61		Introduction to Data-Flow Analysis	1	Black Board	T1
62		**Tutorial14**(Peephole Optimization, The Principal Sources of Optimization)	1		
63		Foundations of Data-Flow Analysis,	1	Black Board	T1

	5	Constant Propagation			
64		Partial-Redundancy Elimination	1	Black Board	T1
65		Loops in Flow Graphs	1	Black Board	T1
66		**Tutorial5**(Constant Propagation, Loops in Flow Graphs)	1	Black Board	T1

TEXT BOOKS

1. Compilers: Principles, Techniques and Tools, Second Edition, Alfred V. Aho, Monica S. Lam, Ravi Sethi, Jeffry D. Ullman, Pearson.

REFERENCE BOOKS

1. Compiler Construction-Principles and Practice, Kenneth C Louden, Cengage Learning.
2. Modern compiler implementation in C, Andrew W Appel, Revised edition, Cambridge University Press.
3. The Theory and Practice of Compiler writing, J. P. Tremblay and P. G. Sorenson, TMH
4. Writing compilers and interpreters, R. Mak, 3rd edition, Wiley student edition.
5. lex & yacc – John R. Levine, Tony Mason, Doug Brown, O'reilly

WEB REFERENCES

S.No	Web Link
WR1:	**https://www.geeksforgeeks.org/compiler-design-tutorials/**
WR2:	**https://www.tutorialspoint.com/compiler_design/**
WR3:	**https://www.youtube.com/watch?v=_ck1Lnm28hQ&t=7s**
WR4:	**http://ecomputernotes.com/compiler-design**

LECTURE NOTES

UNIT-I

https://drive.google.com/file/d/1cu6GhBONlGcX4yyFc9o1ZeLfixzU4c7I/view?usp=sharing

UNIT-II

https://drive.google.com/file/d/1zLUxbIrqW2ffBDXhHbbNrJ6hzrlAY5OK/view?usp=sharing

UNIT-III

https://drive.google.com/file/d/19x8iWjCH2lplUnENgy5JX3HR5UB75ggv/view?usp=sharing

UNIT-IV

https://drive.google.com/file/d/1os2vFlfM3WkwT_bxATZuTGtJzUfQJ6tn/view?usp=sharing

UNIT-V

https://drive.google.com/file/d/13zvqvzrFnBlWtlv5UCcGyapHw5pCHTBn/view?usp=sharing

List of video REFERENCES

VR1: https://www.youtube.com/watch?v=Qkwj65l_96I&list=PLEbnTDJUr_IcPtUXFy2b1sGRPsLFMghhS&index=1

VR2: https://www.youtube.com/watch?v=e73sb5pyriQ

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year II Semester Examinations, August - 2022COMPILER DESIGN
(Computer Science and Engineering)

Time: 3 Hours   Max.Marks:75

Answer any five questions All questions carry equal marks

- - -

1.a) What are the advantages of a compiler over an interpreter?
  b) Draw the structure of a compiler and describe various phases in the compilation processmention the output of the following statement: $id_1=id_2+id_3*50$ at each phase.   [5+10]

2.a) Design the LEX program that recognizes the tokens of a C language and returns thetoken found.
  b) Give the DFA and NFA to accept the strings containing a, b such that the stringcontains even number of a's and odd number of b's.   [7+8]

3.a) Remove the left recursion for the following grammar and also find FIRSTS andFOLLOWs.
     $E \rightarrow E + T \mid T$
     $T \rightarrow T * F \mid F F \rightarrow (E)/id$
  b) Write the steps/algorithm to construct the predictive parser table and explain with anexample.   [7+8]

4.a) Construct the Recursive Descent Parser with backtracking for the following grammar:
     $S \rightarrow aSbS \mid bSaS \mid \mathcal{E}$
  b) Compute LR(0) items for the following grammar and construct SLR parser table: [7+8]$S \rightarrow L=R \mid R$
     $L \rightarrow *R \mid idR \rightarrow L$

5.a) Construct the syntax directed definition to convert infix notation into postfix notation.
  b) Describe different ways of implementing intermediate code generation of a three-address statement.   [8+7]

6.a) Explain how an L-attributed grammar is converted into a translation scheme.
  b) Compare and contrast S-Attributed definitions with L-Attributed definitions.   [8+7]

7. How is stack storage allocation strategy different from heap allocation strategy?Describe them mentioning their merits and demerits.   [15]

8. Explain the foundations and basic notations used in data-flow analysis for optimizationswith examples. [15]

---oo0oo---

CodeNo:156AH

R18

JAWAHARLALNEHRUTECHNOLOGICALUNIVERSITY HYDERABAD
B.Tech IIIYear II SemesterExaminations,August/September-2021 COMPILER DESIGN
(ComputerScienceandEngineering)

Time:3Hours   **Max.Marks: 75**

Answer any five questions
Allquestionscarryequalmarks

1.a)   StatethereasonsforseparatingLexicalanalysisandSyntax analysis.
  b)   Discuss how Finite Automata is used to recognize tokens and perform lexical analysis with example.   [7+8]

2.a)   HowtospecifytheTokens?DifferentiateToken,LexemeandPatternwithsuitable examples.
  b)   ExplainvariousErrorRecoverystrategies inLexicalanalysis.   [7+8]

3.a)   What do you mean byAmbiguous Grammar? Check whether the following grammar is Ambiguous or not
       S→aAB,
       A→bC/cd,
       C→cd,
       B→c/d
  b)   Writeanote onYacc.   [8+7]

4.   ConstructCLRparsingtableforthefollowingGrammar S
         →L=R
       S→R
       L→*R
       L→id
        R→L(Writeallnecessaryprocedures).   [15]

5.a)   GiveSyntax Directed TranslationschemeforSimpleDeskCirculator.
  b)   Convert the following arithmetic expression into Syntax Tree and Three Address Code b*3(a+b).   [7+8]

6.a)   DifferentiateSynthesizedand InheritedAttributeswithexample.
  b)   GenerateIntermediatecodeforthefollowingcodesegmentalongwiththeSyntax Directed Translation Scheme.
       if (a > b)
       x=a+b;
       else
       x=a-b;
       Where'a'and'x'areofrealand'b'ofinttypedata.   [7+8]

7. a) What is Flow-Graph? Explain how the given program can be converted into Flow- Graph?
   b) Construct DAG for the following basic block:

   d:= b+c
   e:=a+b
   b:=b*c
   a:=e-d   [8+7]

8. a) "*Copypropagation Leads to Dead code*" -Justify the statement.
   b) Explain Global Data Flow analysis with necessary equations.   [7+8]

---ooOoo---

CodeNo:156AH

R18

JAWAHARLALNEHRUTECHNOLOGICALUNIVERSITY HYDERABAD
B.TechIIIYearIISemesterExaminations,February/March-2022
COMPILERDESIGN
(ComputerScienceandEngineering)

Time:3Hours   **Max.Marks: 75**

Answer any five questions
Allquestionscarryequalmarks

1.a)   Writedownthestepsin constructingDFA fortheregularexpression (a/b)*aab(a/b)*.
 b)   Explain with an example how lex program perform lexical analysis for the
      arithmeticoperatorsandidentifiersinC?   [7+8]

2.a)   Givethe basic structureofacompiler and explainvarious components in brief.
 b)   Describetheanalysis-synthesis modelof a compiler.   [7+8]

  Whatisleft-factoring?Writethealgorithmtoeliminateleft-factoringfromagrammar. Explain
     the same with an example.
 b)   Consider the following grammar.
      bexpr→ bexpr **or** bterm | bterm
      bterm→bterm**and**bfactor|bfactor
      bfactor→**not**bfactor|(bexpr)|**true**|**false**
      i) Constructaparsetreeforthesentence**not(true orfalse)**
       ii)   Isthis
         grammarambiguous? Why?   [7+8]

4.   Show that the following grammar is LALR(1)   [15]
           S→Aa | bAc | dc | bda
           A→d

5. a)   Whatarethethreeformsofintermediatecoderepresentations?Explain them.
  b)   Givethesyntax-directeddefinitionofasimpledeskcalculatorandconstructan annotated
       parse tree for the input expression (4*7+1)*2.   [7+8]

6.   ExplainaboutsyntaxdirectedtranslationofBooleanexpressionswithandwithout back
       patching.   [15]

7. a)   Whatisanactivationrecord?Describevariouscomponentsinanactivationrecord considering
       a sample c program.
  b)   Writedownthecode generationalgorithmandexplain briefly.   [8+7]

8. How to construct the basic block and compute DAG for the code fragment? Explain with the following code fragment. [15]

```
procedurefun(x,y,z) begin
        y=z+1; z=z+x;
end fun beginmain()
        a=2; b=3;
        fun(A+B,A,B);
        print(A); endmain
```

---ooOoo---

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

I- Mid Examinations, MAY-2023

Year &Branch: III-CSE(A,B,C)   Date: 10/05/2023 (FN)

Subject:COMPILER DESIGN   Marks: 10   Time: 60 min

Answer any **TWO** Questions. All Question Carry Equal Marks   2*5=10

marks(This question paper is prepared with Course Outcome and BT's mapping)

1. Explain about phases of compiler. (C322.1)(Comprehension)   (5M)
2. Explain LEX tool in detail.   (C322.2)(Comprehension)   (5M)
3. Explain the steps to compute FIRST and FOLLOW with Grammar

   E->TE'

   E'->+TE' | €

   T->FT'

   T'->*FT' | €

   F->(E) | id   (C322.3)   (Comprehension)   (5M)

4. (a) Define Synthesized Attributes , Inherited Attributes .(C322.4)((Knowledge)

   (b)Write short notes on error recovery strategies in parsing.(C322.3) (Knowledge)

QUESTION PAPER MAPPING WITH CO'S

C321.4 25%
C321.6 40%
C321.5 35%

QUESTION PAPER MAPPING WITH BT'S

SYNTHESIS
COMPREHENSION....
KNOWLEDGE

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

I- Mid Examinations, MAY-2023

Year &Branch: III-CSE(A,B,C)　　　　　　　　　　Date: 10/05/2023 (FN)

Subject:COMPILER DESIGN　　　　Marks: 10　　　　Time: 60 min

Answer any **TWO** Questions. All Question Carry Equal Marks　　2*5=10 marks

Discriptive ANSWER KEY

https://docs.google.com/document/d/1sTLz4NM4GnAiiZsG8DvjSp6Jb63auNXE/edit?usp=sharing&ouid=114024940021959755534&rtpof=true&sd=true

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

I - Mid Examinations, MAY -2023

Year & Branch: III-CSE(A,B,C)   Date: 10/05/2023(FN)

Subject: COMPILER DESIGN   Marks: 10   Time: 60 min

Answer any **TWO** Questions. All Question Carry Equal Marks   2*5=10

marks(This question paper is prepared with Course Outcome and BT's mapping)

1 .a) Differentiate between compiler and interpreter.   (2)   (C322.1)   (Analysis)
b) Explain about input buffering   (3)   (C322.1)(Comprehension)

2. Construct DFA for (a|b)*abb by using direct method   (5)   (C322.2)   (Synthesis)

3.a) Explain about backtracking with an example.   (2)   (C322.3)(Comprehension)
b) Consider the CFG: (3)   (C322.3) (Evaluation)
S→SS+|SS*|a   and the string aa+a*
Give a leftmost derivation ,rightmost derivation and parse tree for the given input.

4.a) Explain about SDD.   (3)   (C322.4)(Comprehension)
b) List the FIRST and FOLLOW Rules   (2)   (C322.3) (Analysis)

QUESTION PAPER MAPPING WITH CO'S
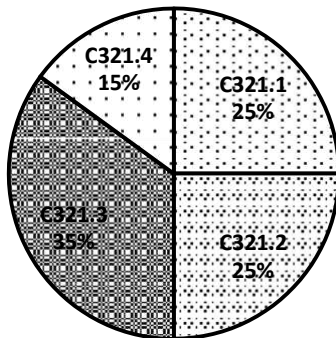
C321.4 15%
C321.1 25%
C321.3 35%
C321.2 25%

QUESTION PAPER MAPPING WITH BT'S

EVALUATION 15%
ANALYSIS 20%
SYNTHESIS 25%
COMPREHENSION 40%

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

I - Mid Examinations, MAY -2023

Year & Branch: III-CSE(A,B,C)   Date: 10/05/2023(FN)
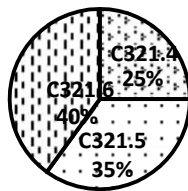
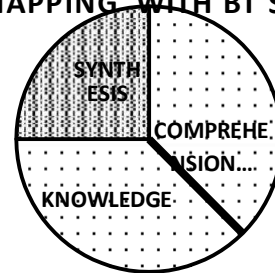Subject: COMPILER DESIGN   Marks: 10   Time: 60 min

Answer any TWO **Questions. All Question Carry Equal Marks   2*5=10**

Discriptive ANSWER KEY

https://docs.google.com/document/d/1_ibpuhs5i_DuCxOfQs4iie8PE509ZaNc/edit?usp=sharing&ouid=114024940021959755534&rtpof=true&sd=true

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

B.TECH. IIIYEAR II SEM., I Mid Term Examinations, MAY – 2023

COMPILER DESIGN

Objective Exam

Nam :_____   Hall Ticket No.

Answer All Questions. All Questions Carry Equal Marks.Time: 20   Min. Marks: 10.

   I. Choose the correct alternative:

1. What is a compiler? [ ]
a) system program that converts instructions to machine language
b) system program that converts machine language to high-level language
c) system program that writes instructions to perform
d) None of the mentioned

2. Which of the following is a stage of compiler design? [ ]
a) Semantic analysis
b) Intermediate code generator
c) Code generator
d) All of the mentioned

3. What is the use of a symbol table in compiler design? [ ]
a) Finding name's scope
b) Type checking
c) Keeping all of the names of all entities in one place
d) All of the mentioned

4. Which of the following error can a compiler check? [ ]
a) Syntax Error
b) Logical Error
c) Both Logical and Syntax Error
d) Compiler cannot check errors

5. A programmer, writes a program to multiply two numbers instead of dividing them by mistake, how can this error be detected? [ ]
a) Compiler or interpreter
b) Compiler only
c) Interpreter only
d) None of the mentioned

6. Who is responsible for the creation of the symbol table? [ ]
a) Assembler
b) Compiler
c) Interpreter
d) All of the mentioned

7. Which of the following is known as a compiler for a high-level language that runs on one machine and produces code for a different machine? [ ]
a) Cross compiler
b) Multipass compiler
c) Optimizing compiler
d) One pass compiler

8. Which of the following is a system program that integrates a program's individually compiled modules into a form that can be executed? [　]
a) Interpreter
b) Assembler
c) Compiler
d) Linking Loader

9. Which of the following is a definition of compiler? [　]
a) Acceptance of a program written in a high-level language and produces an object program
b) Program is put into memory and executes it
c) Translation of assembly language into machine language
d) None of the mentioned

10. Which of the following phase of the compiler is Syntax Analysis? [　]
a) Second
b) Third
c) First
d) All of the mentioned

II Fill in the Blanks

11. Which of the following concept of FSA is used in the compiler＿＿＿＿＿＿＿＿.
12. What is CFG＿＿＿＿＿＿＿＿＿＿＿.
13. ＿＿＿＿＿＿＿＿＿＿the following error can Compiler diagnose
14. In which of the＿＿＿＿＿＿＿＿＿＿phase of the compiler is Lexical Analyser.
15. Which of＿＿＿＿＿＿＿＿＿does an address code involve.
16. Characters are grouped into tokens in which of the＿＿＿＿＿phase of the compiler design.
17. Why System program such as compiler are designed＿＿＿＿＿＿＿.
18. Which of the technique＿＿＿＿＿＿＿＿is used for building cross compilers for other machines.
19. Which of the can detect an error if a programmer by mistake writes multiplication instead of division＿＿＿＿＿＿＿.
20. What is the first phase of compiler＿＿＿＿＿＿＿.

COMPILER DESIGN OBJECTIVE MID I KEY:

https://docs.google.com/document/d/1Enbh5j5LysgsVaGr2-SWc9uXXvxTMLrF/edit?usp=sharing&ouid=114024940021959755534&rtpof=true&sd=true

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510
II- Mid Examinations, JUNE-2023

Year & Branch: III-CSE-A, B,C   Date: 26/07/2023(FN)

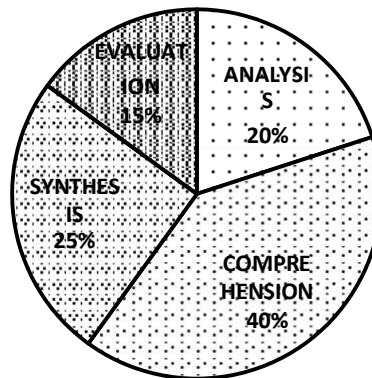Subject: COMPILER DESIGN   Marks: 10   Time: 60 min

Answer any **TWO** Questions. All Question Carry Equal Marks   2*5=10 marks
(This question paper is prepared with Course Outcome and BT's mapping)

1. Explain Quadruples, triples, indirect triples with the statement a = b * -c + b * -c (5M)
   (C322.4) (Comprehension)
2. Explain in detail about storage organization (5M). (C322.5)(Comprehension)
3. Explain different principle sources of optimization technique with suitable examples(5M)
   (C322.6)(Comprehension)
4. a) What are the forms of target program?(2M) (C322.5)   (Synthesis)

   b) What is machine independent code optimization? (3M) (C322.6)   (Synthesis)

QUESTION PAPER MAPPING WITH CO'S — C321.4 25%, C321.6 40%, C321.5 35%

QUESTION PAPER MAPPING WITH BT'S — SYNTHESIS 25%, COMPREHENSION 75%

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

II- Mid Examinations, JUNE-2023

Year & Branch: III-CSE-A, B, C   Date: 26/07/2023(FN)

Subject: COMPILER DESIGN   Marks: 10   Time: 60 min

Answer any **TWO** Questions. All Question Carry Equal Marks   2*5=10 marks

ANSWER KEY

https://docs.google.com/document/d/1xt4e1PQ8c6Ulr8QIgmjFoePaRNGTgVzT/edit?usp=sharing&ouid=114024940021959755534&rtpof=true&sd=true

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510
II- Mid Examinations, JUNE-2023

Year & Branch: III-CSE-A, B,C   Date: 26/07/2023(FN)

Subject: COMPILER DESIGN   Marks: 10   Time: 60min

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

1. Define following terms Type system, Type expression, Type equivalence, three address code, DAG.

    (C322.4)(Knowledge) (5M)

2. Explain in detail about Mark-and-sweep garbage collector algorithm.(C322.5)(Comprehension) (5M)

3. Explain peephole optimization.   (C322.5)(Comprehension) (5M)

4. Explain different principal sources of code optimization.   (C322.6)(Comprehension) (5M)
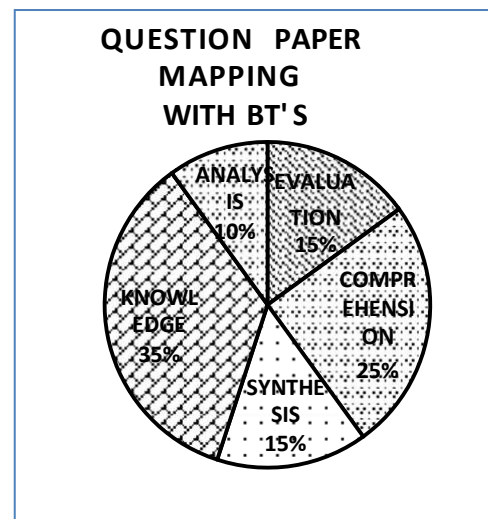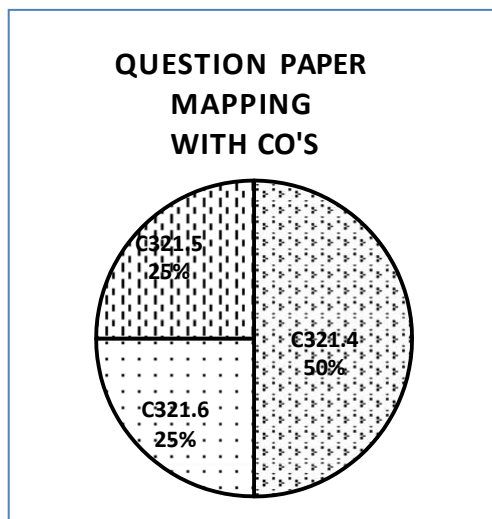
QUESTION PAPER MAPPING WITH CO'S

- C321.5 25%
- C321.4 50%
- C321.6 25%

QUESTION PAPER MAPPING WITH BT'S

- ANALYSIS 10%
- EVALUATION 15%
- COMPREHENSION 25%
- KNOWLEDGE 35%
- SYNTHESIS 15%

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510

II- Mid Examinations, JUNE-2023

Year & Branch: III-CSE-A, B,C   Date:

Subject: COMPILER DESIGN   Marks: 10   Time:

60min

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks
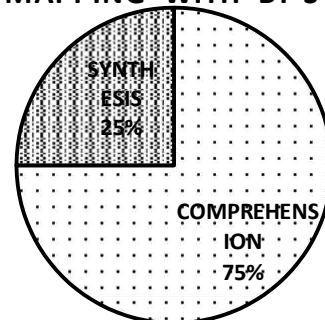
ANSWER KEY:

https://docs.google.com/document/d/1YU58_iC-7r_VZinjRI8F5nOppqtK6qBf/edit?usp=sharing&ouid=114024940021959755534&rtpof=true&sd=true

Sri Indu Institute of Engineering & Technology

Sheriguda (V), Ibrahimpatnam (M), R.R.Dist-501 510
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
B.TECH. III YEAR II SEM., II Mid Term Examinations, JUNE – 2023
COMPILER DESIGN
Objective Exam

Name_____**Hall Ticket No**.

Answer All Questions. All Questions Carry Equal Marks.   Time: 20 Min. Marks: 10.

1. *Determining common sub expression can be done using_____[   ]*
A)Compiler B)Interpreter C)DAG D)Parse tree

2. Control stack in run time environment is used to manage_____   [   ]
A) Data object B) Active procedures C) Target code D) None of the above

3. Recursive procedures are not supported by_____   [ ]
A) Stack allocation B) Heap allocation C) Static allocation D) Code area

4. Following is a form of an object code_____   [   ]
A) Three address code B) Polish notation C) Relocatable code D) None of the above

5. Code generation take_____as input   [ ]
A) Source code B) Assembly language code C) Intermediate code D) None of the above

6. The statement of the form a:=b is called a_____Statement.   [   ]
A)Common B)Copy C) Induction Variable D) Decode

7. The storage strategy in which activation record is maintained even after the execution of a procedure is completed.   [   ]
A)Stack allocation B) Heap allocation C) Static allocation D)Dynamic allocation

8. Reduction in strength means_____   [   ]
A) Removing loop invariant computations
B) Replacing runtime computations by compile time computations
C)Removing common sub-expression elimination
D)Replacing costly operation by cheaper one

9. The graph that shows basic block and their successor relationships is called_____[   ]
A) Flow graph B) Control graph C) Hamilton graph D) DAG

10. Data flow equations can be computed using_____   [   ]
A) Available expression   B) Reaching definitions C) Live variable analysis D) All of the above

Fill in the blanks

11. General Form of a three-address statement is _____

12. At a point in a program if the value of the variable can be used subsequently, then that variable is _____Variable.

13. Any statement that immediately follows a goto or conditional goto statement in a sequence of three address statements is a _____

14. List out optimization of basic blocks methods_____

15.DAG stands for_____

16.Register allocation is an important issue in_____phase.

17._____is a sequence of consecutive statements in which flow of control enters at the beginning and the end without halt .

18.The process of moving the statement from one part of the program to another is called_____

19.Data flow analysis is done during_____phase.

20.In_____method the number of jumps and tests can be reduced by writing the code two times.

COMPILER DESIGN OBJECTIVE MID II KEY:

https://docs.google.com/document/d/1zKUhgpuELdpZa0BD9Gawi-VtFDYapj5b/edit?usp=sharing&ouid=114024940021959755534&rtpof=true&sd=true

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510 Website: https://siiet.ac.in/

Assignment Questions-I

(Assignment Questions are mapped with CO's, BT)

ASSIGNMENT -I

1. Explain about following: (C322.1)   (Comprehension)
a) Static scope and block structure   b) Environments and States
c) Parameter passing mechanism   d) Role of a Lexical Analyzer.

2. Construct DFA for by using – ((a+b)* + (ac)*) by direct method.   (C322.2) (Synthesis)

3. a) State FIRST and FOLLOW Rules and construct SLR parsing table for the grammar:
E→E+T/T, T→T*F/F, F→ (E)/id   (C322.3)   (Knowledge)
b) Write a short note on YACC   (C322.3)   (Knowledge)

4. a) Construct CLR Parsing table for the grammar: (C322.3)   (Synthesis)
S → Aa/bAc/dc/bda
A→d   and also parse the input bdc
b) Compare and contrast LR parsing techniques.   (C322.3)   (Evaluation)

5. a) Write short on dependency graph   (C322.4)   (Knowledge)
   b) Define syntax tree. What is S-attributed definition? Explain construction of syntax tree for the expression a-4+c using SDD.   (C322.4)   (Knowledge)

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956 (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510 Website: https://siiet.ac.in/

Assignment Questions-II

(Assignment Questions are mapped with CO's, BT)

1. a) Define Type Equivalence?(C322.4) (Knowledge)
b) Explain intermediate code for procedures.(C322.4) (Comprehension)

2. a) Define Basic Block. List the terminologies used in basic block.(C322.5)(Knowledge)
b) What is DAG? Mention its applications?(C322.5)(Synthesis)
c) Construct DAG for the following basic blocks:(C322.5) (Synthesis)
i) a := b*c   ii) d := b   iii) e := d * c   iv) b := e   v) f := b + c   vi) g := f + d

3. a) Write short notes on Peephole optimization.(C322.5)(Knowledge)
b) Define Activation Record? Explain in brief about the fields in activation record. (C322.5)(Knowledge)

4. Write about data flow analysis?(C322.6)(Knowledge)

5. What is flow graph? Explain in detail about loops in flow graph.(C322.6)(Synthesis)

Result Analysis:

Course Title	COMPILER DESIGN
Course Code	CS601PC
Programme	B.Tech
Year & Semester	IIIyear II-semester, A sec
Regulation	R18
Course Faculty	Mr.Dr.Sasikumar D , Assistant Professor , CSE

Weak Students:

S No	Roll no	No of backlogs	Internal-I Status	Internal-II Status
1	20X31A0503	6	17	18
2	20X31A0506	4	20	19
3	20X31A0507	6	17	19
4	20X31A0508	3	23	21
5	20X31A0511	5	18	16
6	20X31A0520	4	21	19
7	20X31A0526	5	23	21
8	20X31A0527	3	23	17
9	20X31A0530	3	22	22
10	20X31A0531	5	24	23
11	20X31A0533	5	22	18
12	20X31A0540	3	21	17
13	20X31A0541	3	23	21
14	20X31A0546	3	21	21
15	20X31A0554	3	21	19
16	20X31A0556	5	17	5
17	20X31A0557	3	21	21
18	20X31A0558	6	5	20
19	20X31A0559	5	21	22

Advanced learners

S No	Roll No	Gate Material
1	20X31A0501	
2	20X31A0502	
3	20X31A0504	
4	20X31A0510	
5	20X31A0512	Lexical Analysis / Parsing/ Syntax-directed Translation/ Intermediate Code Generation/ Runtime Environment/ Matching
6	20X31A0513	
7	20X31A0514	
8	20X31A0515	
9	20X31A0516	
10	20X31A0518	
11	20X31A0519	
12	20X31A0522	
13	20X31A0523	
14	20X31A0529	
15	20X31A0534	
16	20X31A0535	
17	20X31A0537	
18	20X31A0538	

19	20X31A0539	
20	20X31A0542	
21	20X31A0544	
22	20X31A0545	
23	20X31A0549	
24	20X31A0550	
25	20X31A0551	. Lexical Analysis / Parsing/ Syntax-directed Translation/ Intermediate Code Generation/ Runtime Environment/ Matching
26	20X31A0553	
27	20X31A0556	
28	20X31A0560	
29	21X35A0501	
30	21X35A0502	

BATCH CSE-III BTECH II- SEM CSE - A RESULT ANALYSIS

ACADAMIC YEAR	COURSE NAME	NUMBER OF STUDENTS		QUESTION PAPER SETTING		PASS%
		APPEARED	PASSED	INTERNAL	EXTERNAL	
2022-23	COMPILER DESIGN	63	52	COURSE FACULTY	EXTERNAL	82.53 %

COMPILER DESIGN (C324) Result Analysis
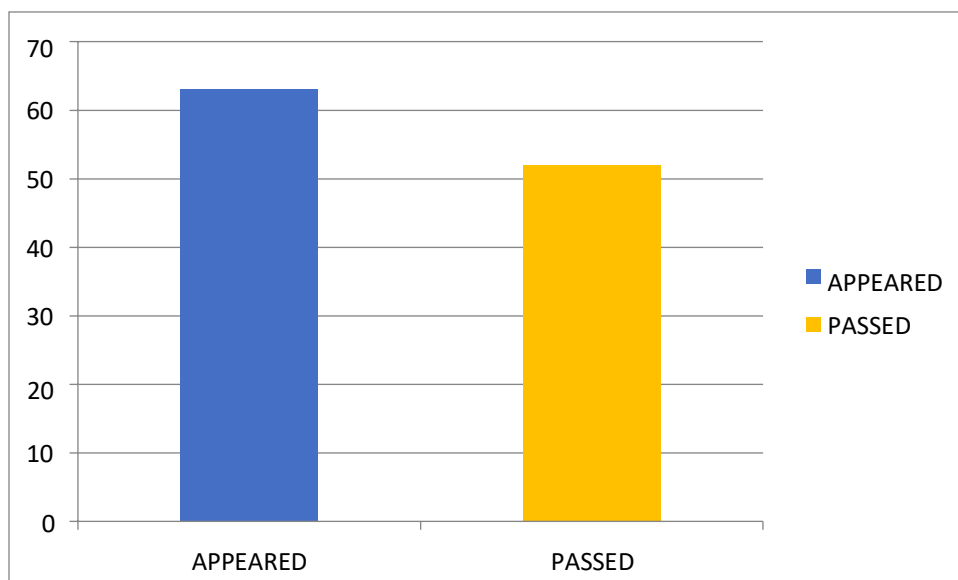
SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC)
Accredited by NAAC with A+ Grade, Recognized under 2(f) of UGC Act 1956
(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)
Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510
Website: https://siiet.ac.in/

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

REMEDIAL CLASSES TIME TABLE

A.Y 2022-23   SEMESTER-II

BRANCH/ SEC	MON 4.00 PM- 5.00 PM	TUE 4.00 PM-5.00 PM	WED 4.00 PM- 5.00 PM	THUR 4.00 PM- 5.00 PM	FRI 4.00 PM- 5.00 PM
II CSE-A	DM	JAVA	DBMS	BEFA	OS
II CSE-B	BEFA	DBMS	DM	OS	JAVA
II CSE-C	DBMS	OS	BEFA	JAVA	DM
III CSE-A	CD	ML	DAA	STM	FIOT
III CSE-B	DAA	FIOT	CD	ML	STM
III CSE-C	ML	STM	FIOT	CD	DAA
IVCSE-A	OB	TQM	DS	.	-
IV CSE-B	DS	OB	TQM	.	-
IV CSE-C	TQM	DS	OB	.	-

HOD
Computer Science & Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH.
Shenguda(V), Ibrahimpatnam(M), R.R.Dist-501 1C

PRINCIPAL
Sri Indu Institute of Engineering & Tech
Shenguda(Vill) Ibrahimpatnam,
R.R. Dist Telangana -501 510

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Computer Science and Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty: **Dr.Sasikumar D**   Academic Year: **2022-23**

Branch & Section: **CSE- A**   Examination: **I Internal**

Course Name: COMPILER DESIGN   Year: **III**   Semester: **II**

S.No	HT No.	Q1a	Q1b	Q1c	Q2a	Q2b	Q2C	Q3A	Q3b	Q3c	Q4a	Q4b	Q4c	Obj1	A1
Max. Marks ==>		5			5			5			1	1	3	10	5
1	20X31A0501	4						5						9	5
2	20X31A0502	5			5									9	5
3	20X31A0503	5												7	5
4	20X31A0504	5			4									9	5
5	20X31A0506	5			2									8	5
6	20X31A0507	5												7	5
7	20X31A0508	5			5									8	5
8	20X31A0509	5			4									9	5
9	20X31A0510	4			4									9	5
10	20X31A0511	5												8	5
11	20X31A0512	5			4									9	5
12	20X31A0513	4			4									8	5
13	20X31A0514	5			4									9	5
14	20X31A0515	5			5									9	5
15	20X31A0516	5			4									9	5
16	20X31A0517	5			4									9	5
17	20X31A0518	5			4									9	5
18	20X31A0519	5			4									9	5
19	20X31A0520	4			4									8	5
20	20X31A0521	4			4									8	5
21	20X31A0522	5			4									9	5
22	20X31A0523	5			4									9	5
23	20X31A0524	5			4									8	5
24	20X31A0525	4			5									9	5
25	20X31A0526	5			4									9	5
26	20X31A0527	5			4									9	5
27	20X31A0528	5			3									9	5
28	20X31A0529	5			5									9	5
29	20X31A0530	5			4									8	5
30	20X31A0531	5			5									9	5
31	20X31A0532	3			4									9	5
32	20X31A0533	4			4									9	5
33	20X31A0534	4			5									9	5
34	20X31A0535	5			5									9	5
35	20X31A0536	5			4									8	5
36	20X31A0537	5			4									8	5
37	20X31A0538	5			5									9	5
38	20X31A0539	4			4									9	5
39	20X31A0540	4			4									8	5

#	Roll No														
40	20X31A0541	5			4									9	**5**
41	20X31A0542	4			4									9	**5**
42	20X31A0543	5			5									9	**5**
43	20X31A0544	5			5									9	**5**
44	20X31A0545	5			5									9	**5**
45	20X31A0546	4			4									8	**5**
46	20X31A0547	4			4									9	**5**
47	20X31A0548	4			4									9	**5**
48	20X31A0549	5			5									9	**5**
49	20X31A0550	5			4									8	**5**
50	20X31A0551	5			5									8	**5**
51	20X31A0552	4			4									9	**5**
52	20X31A0553	5			4									8	**5**
53	20X31A0554	4			4									8	**5**
54	20X31A0555	5			4									9	**5**
55	20X31A0556	4												8	**5**
56	20X31A0557	4			4									8	**5**
57	20X31A0558		A											AB	**5**
58	20X31A0559	5			2									9	**5**
59	20X31A0560	5			5									9	**5**
60	21X35A0501	5			5									7	**5**
61	21X35A0502	5			5									8	**5**
62	21X35A0503	5			5									9	**5**
63	21X35A0504	3			2									9	**5**
64															

Target set by the faculty / HoD	3.00	0.00	0.00	3.00	0.00	0.00	3.00	0.00	0.00	0.60	0.60	1.80	6.00	3.00
Number of students performed above	62	0	0	54	0	0	1	0	0	0	0	0	62	63
Number of students attempted	62	1	0	57	0	0	1	0	0	0	0	0	63	63
Percentage of students scored more than target	100%	0%		95%			100%						98%	100%

CO Mapping with Exam Questions:

CO - 1	Y			Y										Y	Y
CO - 2							Y	Y						Y	Y
CO - 3										Y				Y	Y
CO - 4															
CO - 5															
CO - 6															

CO Attainment based on Exam Questions:

CO - 1	100%			95%										98%	100%
CO - 2														98%	100%
CO - 3														98%	100%
CO - 4															
CO - 5															
CO - 6															

CO	Subj	obj		Asgn	Overall	Level
CO-1	97%	98%		100%	99%	
CO-2		98%		100%	99%	
CO-3		98%		100%	99%	
CO-4						
CO-5						
CO-6						

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal 1 Examination) = **3.00**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Computer Science and Engineering
Course Outcome Attainment (Internal Examination-2)

Name of the faculty**Dr.Sasikumar D**   Academic Year: **2022-23**
Branch & Section: CSE- A   Examination: II Internal
Course Name: **COMPILERDESIGN**   Year: III   Semester: II

S.N	HT No.	Q1a	Q1b	Q1c	Q2a	Q2b	Q2c	Q3a	Q3b	Q3c	Q4a	Q4b	Q4c	Obj4	A4
Max. Marks ==>		**2**	**3**		**2**	**3**		**5**			**5**			**10**	**5**
1	20X31A0501				2	3		3						8	**5**
2	20X31A0502				2	3		5						8	**5**
3	20X31A0503										5			8	**5**
4	20X31A0504	2	3								5			7	**5**
5	20X31A0506	2			2	3								7	**5**
6	20X31A0507					3					4			7	**5**
7	20X31A0508					3					5			8	**5**
8	20X31A0509				2	3								8	**5**
9	20X31A0510				2	3					4			7	**5**
10	20X31A0511				2	2								7	**5**
11	20X31A0512					3					4			7	**5**
12	20X31A0513				2	3					3			8	**5**
13	20X31A0514					3		3						8	**5**
14	20X31A0515				2	3		5						7	**5**
15	20X31A0516				2	3					5			8	**5**
16	20X31A0517				2	2					5			8	**5**
17	20X31A0518				2	3					3			8	**5**
18	20X31A0519				2	2					3			7	**5**
19	20X31A0520				2	3					2			7	**5**
20	20X31A0521					3					4			7	**5**
21	20X31A0522				2	2		4						7	**5**
22	20X31A0523				2	3		5						7	**5**
23	20X31A0524				2	3					2			8	**5**
24	20X31A0525				2	3					4			8	**5**
25	20X31A0526	2	2								4			8	**5**
26	20X31A0527					2					3			7	**5**
27	20X31A0528				2	3					3			7	**5**
28	20X31A0529							4			5			7	**5**
29	20X31A0530				2	3					4			8	**5**
30	20X31A0531				2	3					5			8	**5**
31	20X31A0532					2					2			7	**5**
32	20X31A0533					3		3						7	**5**
33	20X31A0534				2	3					4			8	**5**
34	20X31A0535				2	3					4			9	**5**
35	20X31A0536							4			4			7	**5**
36	20X31A0537				2	3		4						7	**5**
37	20X31A0538				2	3					4			7	**5**
38	20X31A0539	2	2								5			7	**5**

S.No	Roll No															
39	20X31A0540					2					3			7	**5**
40	20X31A0541	2	3								4			7	**5**
41	20X31A0542					3					4			7	**5**
42	20X31A0543				2	2	4							8	**5**
43	20X31A0544				2	3	5							7	**5**
44	20X31A0545														**5**
45	20X31A0546														**5**
46	20X31A0547														**5**
47	20X31A0548														**5**
48	20X31A0549														**5**
49	20X31A0550														**5**
50	20X31A0551														**5**
51	20X31A0552														**5**
52	20X31A0553														**5**
53	20X31A0554														**5**
54	20X31A0555														**5**
55	20X31A0556														**5**
56	20X31A0557														**5**
57	20X31A0558														**5**
58	20X31A0559														**5**
59	20X31A0560														**5**
60	21X35A0501														**5**
61	21X35A0502														**5**
62	21X35A0503														**5**
63	21X35A0504														**5**

Target set by the faculty / HoD	1.20	1.80	0.00	1.20	1.80	0.00	3.00	0.00	0.00	3.00	0.00	0.00	6.00	3.00
Number of students performed above the target	6	5	0	37	50	0	18	0	0	39	0	0	61	63
Number of students attempted	6	5	0	37	50	0	18	0	0	44	0	0	63	63
Percentage of students scored more than target	100%	100%		100%	###		100%			89%			97%	100%

CO Mapping with Exam Questions:

CO - 1														
CO - 2														
CO - 3														
CO - 4	Y												Y	Y
CO - 5				Y		Y							Y	Y
CO - 6										Y			Y	Y

% Students Scored >Target %	100%			100%			100%			100%			100%	100%

CO Attainment based on Exam Questions:

CO - 1														
CO - 2														
CO - 3														
CO - 4	100%												97%	100%
CO - 5				100%			100%						97%	100%
CO - 6										89%			97%	100%

CO	Subj	obj		Asgn	Overall	Level
CO-1						
CO-2						
CO-3						
CO-4	100%	97%		100%	99%	3.00
CO-5	100%	97%		100%	99%	3.00
CO-6	89%	97%		100%	95%	3.00

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal Examination-2) =   **3.00**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Computer Science and Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty : Dr.SasiKumar D Academic Year: **2022-23**
Branch & Section: CSE- A Year / Semester: III/II
Course Name: **COMPILER DESIGN**

S.No	Roll Number	Marks Secured	S.No	Roll Number	Marks Secured
1	20X31A0501	10	36	20X31A0537	32
2	20X31A0502	32	37	20X31A0538	26
3	20X31A0503	13	38	20X31A0539	43
4	20X31A0504	40	39	20X31A0540	19
5	20X31A0506	5	40	20X31A0541	26
6	20X31A0507	1	41	20X31A0542	43
7	20X31A0508	13	42	20X31A0543	41
8	20X31A0509	27	43	20X31A0544	37
9	20X31A0510	27	44	20X31A0545	48
10	20X31A0511	4	45	20X31A0546	13
11	20X31A0512	26	46	20X31A0547	26
12	20X31A0513	26	47	20X31A0548	12
13	20X31A0514	30	48	20X31A0549	41
14	20X31A0515	26	49	20X31A0550	43
15	20X31A0516	26	50	20X31A0551	43
16	20X31A0517	17	51	20X31A0552	10
17	20X31A0518	45	52	20X31A0553	32
18	20X31A0519	28	53	20X31A0554	26
19	20X31A0520	8	54	20X31A0555	48
20	20X31A0521	13	55	20X31A0556	7
21	20X31A0522	46	56	20X31A0557	13
22	20X31A0523	34	57	20X31A0558	1
23	20X31A0524	7	58	20X31A0559	1
24	20X31A0525	15	59	20X31A0560	42
25	20X31A0526	2	60	21X35A0501	44
26	20X31A0527	9	61	21X35A0502	28
27	20X31A0528	17	62	21X35A0503	49
28	20X31A0529	37	63	21X35A0504	27
29	20X31A0530	4			
30	20X31A0531	4			
31	20X31A0532	26			
32	20X31A0533	9			
33	20X31A0534	16			
34	20X31A0535	38			
35	20X31A0536	13			

Max Marks	75

Class Average mark	#DIV/0!
Number of students performed above the target	0
Number of successful students	63

Attainment Level	% students
1	40%
2	50%

Percentage of students scored more than target	0%		3	60%
Attainment level	**1**			

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Computer Science and Engineering

Course Outcome Attainment

Name of the faculty Dr.SasiKumar D

Branch & Section: CSE-A

Course Name:COMPILER DESIGN

Academic Year 2022-23

Examination: I Internal

Year: III

Semester: II

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00		3.00	1.00	1.50
CO2	3.00		3.00	1.00	1.50
CO3	3.00		3.00	1.00	1.50
CO4		3.00	3.00	1.00	1.50
CO5		3.00	3.00	1.00	1.50
CO6		3.00	3.00	1.00	1.50
Internal & University Attainment:			3.00	1.00	
Weightage			25%	75%	
CO Attainment for the course (Internal, University)			0.75	0.75	
CO Attainment for the course (Direct Method)			1.50		

Overall course attainment level **1.50**

Name of Faculty: Dr.SasiKumar D
Academic Year: 2022-23
Branch & Section: CSE- A   Year: III

Course Name: COMPILER DESIGN   Semester: II

CO-PO mapping

PO/PSO/CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C322.1	3	-	-	-	-	-	-	-	-	-	3	-	3	1
C322.2	2	2	-	2	3	-	-	-	-	-	3	-	2	3
C322.3	2	2	-	2	3	-	-	-	-	-	2	-	2	2
C322.4	2	-	-	2	3	-	-	-	-	-	1	-	1	2
C322.5	-	3	-	1	2	-	-	-	-	-	-	-	2	3
C322.6	-	3	-	-	-	-	-	-	1	-	-	-	-	1
C322	2.25	2.5	-	1.7	2.75	-	-	-	1	-	2.25	-	2	2

CO	Course Outcome Attainment
CO1	1.50
CO2	1.50
CO3	1.50
CO4	1.50
CO5	1.50
CO6	1.50
Overall course attainment level	1.50

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO Attainment	1.38	0.00	1.13	0.00	0.50	0.00	0.00	1.00	0.00	0.00	1.50	0.00

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)

ASSIGNMENTS AND REGISTER

Assignment-1 Script Link:

https://drive.google.com/file/d/1C1rC5dflM0Qrsx67Pxrmi-AtpHex00Rh/view?usp=sharing

Assignment-2 Script Link:

https://drive.google.com/file/d/1D9PQ6ABDcit1lzjBTW73QXpRX8Ra9EOa/view?usp=sharing

Attendance Register Link:

https://drive.google.com/file/d/1lC-v_SiV6tPsy1foCxZOOyQH6u_slFS5/view?usp=sharing