Sri Indu Institute of Engineering & Technology

Recognized Under 2(f) of UGC Act 1956
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Affiliated to JNTUH, Hyderabad.

COURSE FILE

ON

Computer Organization and Architecture

Course Code - CS304PC

II B.Tech I-SEMESTER

A.Y.: 2022-2023

Prepared by

Dr.D.Sasikumar
Associate Professor

B. Rahul Kanth
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PRINCIPAL
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Academic Year	2022-2023
Course Title	Computer Organization and Architecture
Course Code	CS304PC
Programme	B.Tech
Year & Semester	II year I-semester
Branch & Section	CSE-A
Regulation	R18
Course Faculty	Dr. D. Sasikumar, Associate Professor

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To continuous assess of teaching-learning process through institute-industry collaboration..

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students fraternity.

IM4: To create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a prominent knowledge hub for learners, strive for educational excellence with innovative and industrial techniques so as to meet the global needs.

Mission:

DM1 : To provide ambience that enhances innovations, problem solving skills, leadership qualities, decision making, team-spirit and ethical responsibilities.

DM2 : To impart quality education with professional and personal ethics, so as to meet the challenging technological needs of the industry and society.

DM3 : To provide academic infrastructure and develop linkage with the world class organizations to strengthen industry-academia relationships for learners.

DM4 : To provide and strengthen new concepts of research in the thrust area of Computer Science and Engineering to reach the needs of Government and Society.

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

PROGRAM EDUCATIONAL OBJECTIVES

PEO1: To develop trained graduates with strong academic and technical skills of modern computer science and engineering.

PEO2: To promote trained graduates with leadership qualities and the ability to solve real time problems using current techniques and tools in interdisciplinary environment.

PEO3: To motivate the graduates towards lifelong learning through continuing education and professional development.

PROGRAM SPECIFIC OUTCOMES

PSO1 : **Professional Skills:** To implement computer programs of varying complexity in the areas related to Web Design, Cloud Computing, Network Security and Artificial Intelligence.

PSO2: **Problem-Solving Skills**: To develop quality products using open ended programming environment.

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PROGRAMME OUTCOMES (POs)

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design/development of solutions:**Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO6: **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. tech. in COMPUTER SCIENCE AND ENGINEERING

II YEAR COURSE STRUCTURE AND SYLLABUS (R18)

Applicable From 2018-19Admitted Batch

II YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	CS301ES	Analog and Digital Electronics	3	0	0	3
2	CS302PC	Data Structures	3	1	0	4
3	MA303BS	Computer Oriented Statistical Methods	3	1	0	4
4	CS304PC	Computer Organization and Architecture	3	0	0	3
5	CS305PC	Object Oriented Programming using C++	2	0	0	2
6	CS306ES	Analog and Digital Electronics Lab	0	0	2	1
7	CS307PC	Data Structures Lab	0	0	3	1.5
8	CS308PC	IT Workshop Lab	0	0	3	1.5
9	CS309PC	C++ Programming Lab	0	0	2	1
10	*MC309	Gender Sensitization Lab	0	0	2	0
		Total Credits	**14**	**2**	**12**	**21**

II YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	CS401PC	Discrete Mathematics	3	0	0	3
2	SM402MS	Business Economics & Financial Analysis	3	0	0	3
3	CS403PC	Operating Systems	3	0	0	3
4	CS404PC	Database Management Systems	3	1	0	4
5	CS405PC	Java Programming	3	1	0	4
6	CS406PC	Operating Systems Lab	0	0	3	1.5
7	CS407PC	Database Management Systems Lab	0	0	3	1.5
8	CS408PC	Java Programming Lab	0	0	2	1
9	*MC409	Constitution of India	3	0	0	0
		Total Credits	**18**	**2**	**8**	**21**

***MC-Satisfactory/Unsatisfactory**

CS304PC: COMPUTER ORGANIZATION AND ARCHITECTURE

B.TECH II Year I Sem. **L T P C**

3 0 0 3

Co-requisite: A Course on "Digital Logic Design and Microprocessors".

Course Objectives:

- The purpose of the course is to introduce principles of computer organization and the basic architectural concepts.
- It begins with basic organization, design, and programming of a simple digital computer and introduces simple register transfer language to specify various computer operations.
- Topics include computer arithmetic, instruction set design, microprogrammed control unit, pipelining and vector processing, memory organization and I/O systems, and multiprocessors

Course Outcomes:

- Understand the basics of instructions sets and their impact on processor design.
- Demonstrate an understanding of the design of the functional units of a digital computer system.
- Evaluate cost performance and design trade-offs in designing and constructing a computer processor including memory.
- Design a pipeline for consistent execution of instructions with minimum hazards.
- Recognize and manipulate representations of numbers stored in digital computers

UNIT - I

Digital Computers: Introduction, Block diagram of Digital Computer, Definition of Computer Organization, Computer Design and Computer Architecture.

Register Transfer Language and Micro operations: Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit.

Basic Computer Organization and Design: Instruction codes, Computer Registers Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

UNIT - II

Microprogrammed Control: Control memory, Address sequencing, micro program example, design of control unit.

Central Processing Unit: General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control

.

UNIT - III

Data Representation: Data types, Complements, Fixed Point Representation, Floating Point Representation.

Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

UNIT - IV

Input-Output Organization: Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt Direct memory Access.

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.

UNIT - V

Reduced Instruction Set Computer: CISC Characteristics, RISC Characteristics.

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor.

Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Inter processor arbitration, Inter processor communication and synchronization, Cache Coherence.

TEXT BOOK:

1. Computer System Architecture – M. Moris Mano, Third Edition, Pearson/PHI.

REFERENCE BOOKS:

1. Computer Organization – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGrawHill.
2. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI.
3. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.

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Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510

Website: https://siiet.ac.in/

Department of Computer Science and Engineering

Course Outcomes

Course: Computer Organization and Architecture **Class: II-I SEM CSE -A-Section**

After completing this course the student will be able to:

C214.1	To understand the basic components and design of CPU,ALU and Control Unit (Comprehension)
C214.2	To Design and implement micro programmed control units, instruction formats and addressing modes. (Synthesis)
C214.3	To understand how to perform computer arithmetic operations . (Comprehension)
C214.4	To understand memory hierarchy and input output organization. (Comprehension)
C214.5	To understand the pipeline and vector processing and multiprocessors. (Comprehension)
C214.6	To understand the background of internal communication of computer. (Comprehension)

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO/PSO/ CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C214.1	3	-	-	-	-	-	1	-	-	-	-	2	1	2
C214.2	3	-	-	-		-	-	-	1	-	-	1	2	1
C214.3	2	-	-	-	3	-	-	-	-	-	-	-	1	2
C214.4	3	-	-	-	-	-	-	1	-	-	-	-	2	1
C214.5	3	2	1	-	-	-	-	-	-	-	-	-	1	1
C214.6	3	3	-	-	2	1	-	-	-	2	-	-	1	2
Course	**2.9**	**2.5**	**1**	**-**	**2.5**	**1**	**1**	**1**	**1**	**2**	**-**	**1.5**	**1.3**	**1.5**

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CO – PO / PSO Mapping Justification

Course: Computer Organization and Architecture (C214) **Class: II-I SEM-CSE- A**

PO1: Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design / Development of Solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO5: Modern Tool Usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The Engineer & Society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment & Sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual & Team Work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

PO12: Life Long Learning: Recognize the need for, and have the preparation and ability to engage in independent and life long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1	**Professional Skills:** Ability to implement computer programs of varying complexity in the areas related to web design, cloud computing and networking.
PSO2	**Problem Solving Skills:** The ability to develop quality products using open ended programming environment

C214.1 To understand the basic components and design of CPU,ALU and Control Unit (Comprehension)

	Justification
PO1	Understanding the intricate components and design of a CPU, ALU, and Control Unit requires a synthesis of mathematical, scientific, and engineering knowledge.
PO7	Efficient CPUs and control units drive technological advancements that positively impact society.
PO12	Understanding the basic components and design of CPUs, ALUs, and Control Units serves as a foundational step in an engineer's lifelong learning journey.
PSO1	Understanding of CPU, ALU, and Control Unit design is not only foundational but also highly applicable in implementing computer programs across web design, cloud computing, and networking domains.
PSO2	Understanding the basic components and design of a CPU, ALU, and Control Unit significantly enhances problem-solving skills in open-ended programming environments.

C214.2 To Design and implement micro programmed control units, instruction formats and addressing modes. (Synthesis)

	Justification
PO1	By applying mathematics, science, engineering fundamentals, and specialized knowledge in computer engineering, professionals can solve complex engineering problems related to micro programmed control units, instruction formats, and addressing modes.
PO9	The ability to adapt to evolving project needs, be open to feedback, and iterate designs based on collaborative input is essential in a team environment.
PO12	The design and implementation of micro programmed control units, instruction formats, and addressing modes necessitate a commitment to lifelong learning.
PSO1	The knowledge and skills required for designing and implementing micro programmed control units, instruction formats, and addressing modes are directly

	applicable in programming for web design, cloud computing, and networking.
PSO2	Proficiency in micro programming and control unit design aids in debugging and troubleshooting complex issues.

C214.3 To understand how to perform computer arithmetic operations . (Comprehension)

	Justification
PO1	Understanding computer arithmetic operations involves applying mathematical concepts, scientific knowledge of electronics, foundational engineering principles, and specialized expertise in computer engineering.
PO5	Understanding computer arithmetic involves employing numerical analysis techniques.
PSO1	Knowledge of arithmetic operations is essential in developing networking protocols.
PSO2	Comprehensive knowledge of arithmetic operations facilitates debugging and troubleshooting complex issues.

C214.4 To understand memory hierarchy and input output organization. (Comprehension)

	Justification
PO1	By applying mathematics, science, engineering fundamentals, and specialization, engineers can address complex engineering problems related to memory hierarchy and I/O organization.
PO8	Ethical engineering practice involves compliance with industry standards and regulations.
PSO1	Understanding memory hierarchy and I/O organization allows developers to create responsive and efficient web applications that handle data transfer and user interactions effectively.
PSO2	Proficiency in memory hierarchy and I/O organization fosters effective debugging and optimization.

C214.5 To understand the pipeline and vector processing and multiprocessors. (Comprehension)

	Justification
PO1	Pipeline and vector processing involve mathematical concepts like parallelism, vector operations, and matrix manipulations.
PO2	Utilizing first principles and research, engineers can optimize computational performance.
PO3	Engineers proficient in these techniques design solutions that meet specified computational needs.
PSO1	Understanding these processing methods aids in optimizing network protocols.
PSO2	Understanding pipeline processing, vector processing, and multiprocessors enhances problem-solving skills in an open-ended programming environment.

C214.6 To understand the background of internal communication of computer. (Comprehension)

	Justification
PO1	Engineers use mathematical models and algorithms to optimize data transfer protocols, ensuring efficient communication between various components within the system.
PO2	Understanding the background of internal communication within computer systems empowers engineers to identify, research, analyze, and propose solutions for complex engineering problems.
PO5	The knowledge of internal communication within computer systems enables engineers to effectively employ modern engineering and IT tools, including prediction, modeling, and analysis tools.
PO6	Engineers assess how internal communication systems impact society.
PO10	Engineers can create clear and concise design documentation related to communication architectures and protocols.
PSO1	Programs developed with a strong understanding of internal communication can adapt to diverse computing environments.
PSO2	Understanding the background of internal communication within computers empowers engineers to develop high-quality products within open-ended programming environments.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

ACADEMIC CALENDAR 2022-23

B. Tech./B.Pharm. II YEAR I & II SEMESTERS

I SEM

S. No	Description	Duration	
		From	To
1	Commencement of I Semester classwork	**28.11.2022**	
2	1st Spell of Instructions	28.11.2022	21.01.2023 (8 Weeks)
3	First Mid Term Examinations	23.01.2023	30.01.2023 (1 Week)
4	Submission of First Mid Term Exam Marks to the University on or before	04.02.2023	
5	2nd Spell of Instructions	31.01.2023	29.03.2023 (8 Weeks)
6	Second Mid Term Examinations	31.03.2023	08.04.2023 (1 Week)
7	Preparation Holidays and Practical Examinations	10.04.2023	15.04.2023 (1 Week)
8	Submission of Second Mid Term Exam Marks to the University on or before	15.04.2023	
9	End Semester Examinations	17.04.2023	29.04.2023 (2 Weeks)

Note: No. of Working / Instructional Days: 93

II SEM

S. No	Description	Duration	
		From	To
1	Commencement of II Semester classwork	**01.05.2023**	
2	1st Spell of Instructions (including Summer Vacation)	01.05.2023	08.07.2023 (10 Weeks)
3	**Summer Vacation**	15.05.2023	27.05.2023 (2 Weeks)
4	First Mid Term Examinations	10.07.2023	15.07.2023 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	22.07.2023	
6	2nd Spell of Instructions	18.07.2023	11.09.2023 (8 Weeks)
7	Second Mid Term Examinations	12.09.2023	16.09.2023 (1 Week)
8	Preparation Holidays and Practical Examinations	19.09.2023	23.09.2023 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	23.09.2023	
10	End Semester Examinations	25.09.2023	07.10.2023 (2 Weeks)

Note: No. of Working / Instructional Days: 92

24/11/22

REGISTRAR

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

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TIME TABLE FOR A.Y 2022-23

Class: II-B. Tech CSE -A **Semester: I** **LH. NO: A-301** **W.E.F:28-11-2022**

Period/ Day	1	2	3	4	1:00-1:30	5	6	7
	9:40-10:30	10:30-11:20	11:20-12:10	12:10-1:00		1:30-2:20	2:20-3:10	3:10-4:00
Monday	COSM	ITWS LAB(BATCH-I)/ A&DE LAB(BATCH-II)			L U N C H	A&DE	DS	C++
Tuesday	COSM	C++	COA	DS		A&DE	CO-C/SS/DAA	
Wednesday	C++	COSM	INT	COA		DS LAB(BATCH-I)/ C++ LAB(BATCH-II)		
Thursday	DS	GS LAB		COSM/DS(T)		C++	A&DE	SPORTS
Friday	COA	DS LAB(BATCH-II)/ C++ LAB(BATCH-I)				A&DE	LIB	DS/COSM(T)
Saturday	C++	DS	COUN	COA		ITWS LAB(BATCH-II)/ A&DE LAB(BATCH-I)		

(T) – Tutorial (concern faculty)

Subject Code	Subject Name	Name of the Faculty	Subject Code	Subject Name	Name of the Faculty
CS301ES	Analog and Digital Electronics	Mrs. S.Alekhya	CS309PC	C++ Programming Lab	Mrs P H Swarna Rekha/ Mrs.P.Souwjanya/ Mrs.G.Swapna
CS302PC	Data Structures	Mrs. D.Rajeshwari	MC309	Gender Sensitization Lab	Mrs S Swapna
MA303BS	Computer Oriented Statistical Methods	Mrs. B.Ramadevi		CO-C/SS/DAA	Mrs. D.Rajeshwari
CS304PC	Computer Organization and Architecture	Dr. Sasikumar D	Sports	Sports	Mr K Veera Kishore
CS305PC	Object Oriented Programming Using C++	Mrs P H Swarna Rekha	Internet	Internet	Mrs. Ch Sai Vijaya
CS306ES	Analog and Digital Electronics Lab	Mrs. S.Alekhya	LIB	Library	Mrs P H Swarna Rekha
CS307PC	Data Structures Lab	Mrs. D.Rajeshwari/ Mrs D.Uma/ Mrs.A.Sudha	COUN	Counselling	Mrs.R.Sravanthi
CS308PC	IT Workshop Lab	Mrs T Ramya Priya/ Mrs.Ch.Sai Vijaya/ Mrs. Jakkala Priyanka			
Class In-Charge : Mrs. D.Rajeshwari		Mentor 1 : Mrs. D.Rajeshwari		Mentor 2: Mrs P H Swarna Rekha	

Class In-Charge HOD PRINCIPAL

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LESSON PLAN

Course Title	Computer Organization and Architecture
Course Code	CS304PC
Programme	B.Tech
Year & Semester	II-year I-semester
Regulation	R18
Course Faculty	Dr.D.Sasikumar, Associate Professor , CSE

S. NO	Unit	TOPIC	Number of Sessions Planned	Teaching method/Aids	REFERENCE
1	I	Introduction to Digital Computers	1	Black Board	T1
2		Block diagram of Digital Computer	1	Black Board	T1
3		Definition of Computer Organization	1	Black Board	T1
4		Computer Design and Computer Architecture	2	Black Board	T1
5		Instruction codes	1	Black Board	T1
6		Computer Registers	1	Black Board	T1
7		Computer instructions	1	Black Board	T1
8		Timing and Control	2	Black Board	T1
9		Instruction cycle	1	Black Board	T1
10		Memory Reference Instructions	2	Black Board	T1
11		Input – Output and Interrupt	1	Black Board	T1
12		Complete Computer Description	2	Black Board	T1
13		Control memory	1	Black Board	T1
14		Address sequencing	1	Black Board	T1
15		micro programexample	2	Black Board	T1
16		design of control unit	2	Black Board	T1
17	II	Control memory	1	Black Board	T1
18		Address sequencing	2	Black Board	T1
19		micro program example	2	Black Board	T1
20		design of control unit	1	Black Board	T1
21		General Register Organization	2	Black Board	T1
22		Instruction Formats	1	Black Board	T1

23		Addressing modes	2	Black Board	T1
		Data Transfer and Manipulation	2	Black Board	T1
24		Program Control	1	Black Board	T1
	III	Data types	2	Black Board	T1
25		Complements	1	Black Board	T1
		Fixed Point Representation	2	Black Board	T1
26		Floating Point Representation.	2	Black Board	T1
27		Addition and subtraction	1	Black Board	T1
28		multiplication Algorithms	2	Black Board	T1
29		Division Algorithms	1	Black Board	T1
30		Floating – point Arithmetic operations	2	Black Board	T1
		Decimal Arithmetic unit	2	Black Board	T1
31		Decimal Arithmetic operations.	1	Black Board	T1
32	IV	Input-Output Interface	2	Black Board	T1
33		Asynchronous data transfer	2	Black Board	T1
34		Modes of Transfer	2	Black Board	T1
35		Priority Interrupt	1	Black Board	T1
36		Direct memory Access	2	Black Board	T1
37		Memory Hierarchy	1	Black Board	T1
38		Main Memory	2	Black Board	T1
39		Auxiliary memory	2	Black Board	T1
40		Associate Memory	1	Black Board	T1
41		Cache Memory	2	Black Board	T1
42	V	CISC Characteristics	1	Black Board	T1
43		RISC Characteristics	1	Black Board	T1
44		Parallel Processing	1	Black Board	T1
45		Pipelining	1	Black Board	T1
46		Arithmetic Pipeline	1	Black Board	T1
47		Parallel Processing	1	Black Board	T1
48		Pipelining	1	Black Board	T1
49		Arithmetic Pipeline	1	Black Board	T1
50		Instruction Pipeline	1	Black Board	T1
		RISC Pipeline	1	Black Board	T1
51		Vector Processing	1	Black Board	T1
52		Array Processors	1	Black Board	T1
53		Characteristics of Multiprocessors	1	Black Board	T1
		Interconnection Structures	1	Black Board	T1
54		Inter processor arbitration	1	Black Board	T1
55		Inter processor communication and synchronization	1	Black Board	T1
56		Cache Coherence.	1	Black Board	T1

TEXT BOOKS:

1. Computer System Architecture, M. Moris Mano, Third Edition, Pearson.

REFERENCE:

1. Computer Organization – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGrawHill.
2. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI.
3. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.

WEB REFERENCES:

WR1: https://www.tutorialspoint.com/computer_organization/index.asp

WR2: https://www.studytonight.com/computer-architecture/vector-and-superscalar

WR3: https://www.tutorialspoint.com/what-are-instruction-codes-and-operands-in-computer-architecture

Unit1 link:

https://drive.google.com/file/d/1DFMfaBn3ZgO5WI7Vg_eFChTGm25EkX9J/view?usp=sharing

Unit 2 link:

https://drive.google.com/file/d/1Buqw9xAnQl8MhvC88aIeWZb1TmnCtbyI/view?usp=sharing

Unit 3 link:

https://drive.google.com/file/d/1zDOF6w42LRiuZO302bh-BQSuy9Q-XA4e/view?usp=sharing

Unit 4 link:

https://drive.google.com/file/d/1PYNB48NbgynYG8_4p26HLLx_jC9VBOCC/view?usp=sharing

Unit 5 link:

https://drive.google.com/file/d/1NjjoF_0OcilF2aqUiESmv8Ui0tr_PX6c/view?usp=sharing

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

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(Approved by AICTE,NewDelhi and Affiliated toJNTUH, Hyderabad)

KhalsaIbrahimpatnam, Sheriguda (V),Ibrahimpatnam(M),RangaReddy Dist.,Telangana–501510

Website: https://siiet.ac.in/

Power point presentation

PPT link:

https://docs.google.com/presentation/d/1wiFSZlu7_4UGcsH0voB-jWW8ujCENWiv/edit?usp=sharing&ouid=107122273852189527807&rtpof=true&sd=true

Code No: 153AG **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, March – 2021

COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science and Engineering)

Time: 3 hours **Max. Marks:75**

Answer any five questions
All questions carry equal marks

1.a) Discuss the functional units of a digital computer.
b) Demonstrate construction of a common bus system with multiplexers. [7+8]

2.a) Design a 4-bit combinational circuit decrementer using four full-adder circuits.
b) What is the difference between a direct and an indirect address instruction? How many references tomemory are needed for each type of instruction to bring an operand into a processor register? [7+8]

3.a) Discuss the need of memory stack and stack limits.
b) Explain the general register organization of the processor. [7+8]

4. Explain addition and subtraction of floating point numbers with an example and necessary flowchart. [15]

5.a) A two way set associative cache has lines of 16 bytes and a total size of 8 K bytes. The 64 Mbytesmain memory is byte addressable. Show the format of main memory address.
b) How does SDRAM differ from ordinary DRAM? [8+7]

6.a) Explain the major differences between the central computer and peripheral. How to resolve thesedifferences?
b) Discuss the Strobe control method of Asynchronous data transfer. [8+7]

7.a) What is parallel processing? Explain Flynn's classification of computer.
b) Illustrate vector operations and vector processing. [8+7]

8.a) Discuss about RISC Pipeline.
b) What is cache coherence problem? Discuss solutions for it. [7+8]

---ooOoo---

CodeNo:153AG **R18**

JAWAHARLALNEHRUTECHNOLOGICALUNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, March - 2022
COMPUTERORGANIZATIONANDARCHITECTURE

(Common to CSE,CSBS,CSIT,CSE(SE),CSE(CS),CSE(AIML),CSE(DS),CSE(N))

Time:3Hours **Max.Marks: 75**

Answer any five questions

All questions carry equal marks

---

1. a)	Explain in detail computer design and computer architecture.	
b)	Explain in detail life cycle of instruction.	[9+6]
2.	Explain the following. a) Register transfer. b) Input-Output and interrupt.	[7+8]
3.	Explain in detail various types of addressing modes with examples.	[15]
4.a)	Explain in detail about data transfer instructions.	
b)	Discuss the various types of instruction formats.	[7+8]
5.a)	Explain floating point representation of decimal numbers.	
b)	Explain the decimal addition operation with a neat diagram.	[7+8]
6.a)	Explain the subtraction operation with signed 2'scomplement data.	
b)	Explain in brief fixed point data representation.	[6+9]
7.a)	Explain the working process of DMA.	
b)	Compare cache and main memory.	[9+6]
8.a)	Explain in brief inter-processor communication.	
b)	Discuss the characteristics of multi-processors.	[8+7]

---ooOoo---

Code No: 153AG **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, August/September – 2022

COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to CSE, CSBS, CSIT, CSE(SE), CSE(CS), CSE(AIML), CSE(DS), CSE(N))

Time: 3 Hours **Max.Marks:75**

Answer any five questions

All questions carry equal marks

1.a)	What is the difference between Computer Organization and Computer Architecture?	
b)	Write a short note on instruction code format.	[8+7]
2.a)	Explain the format of Register reference instructions and their functionalities.	
b)	Draw and explain the flowchart for interrupt cycle.	[8+7]
	Define the following terms: i) Control memory ii) Address sequencing	
b)	Explain about the microinstruction format with neat sketch.	[8+7]
4.a)	Explain about various addressing modes.	
b)	Briefly explain about General purpose registers and Flag registers.	[7+8]
5.a)	Explain the flow chart for addition operation with sign-magnitude data.	[8+7]
b)	Perform (-25) + (-10) in binary with negative numbers in 2's complement.	
6.a)	Explain the Booth's algorithm for signed multiplication.	
b)	Draw the flowchart for floating point division.	[8+7]
7.a)	Explain the block diagram of I/O interface.	
b)	Write a short note on Cache memory.	[8+7]
8.a)	Explain about instruction pipelining with an example.	
b)	Discuss about the serial arbitration technique.	[8+7]

---oo0oo---

CodeNo:153AG **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations,September-2021

COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science and Engineering)

Time:3hours **Max.Marks:75**

Answer any five questions

All questions carry equal marks

---

1. a) Draw the block diagram of a digital computer and explain the purpose of each part.
   b) Design a 4-bit combinational circuit decrementer using four full-adder circuits. [6+9]

2. What are the common fields found in instruction format? Explain various instruction formats based on types of CPU Organization? [15]

3. Perform the arithmetic operation (+41)+(-13) and (-41)-(-13) in binary using signed 2's complement representation for negative numbers. [15]

4. a) Draw the block diagram of a typical DMA controller and explain.
   b) Explain Daisy-Chain priority interrupt in detail. [8+7]

5. a) Construct a diagram for a 4×4 omega Switching network. Show the switch setting required to connect input 3 to output 1.
   b) Give a brief note on mutual exclusion with a semaphore. [9+6]

6. a) Differentiate between computer organization and computer architecture.
   b) Explain the Stored Program organization in detail. [7+8]

7. Explain the micro program sequencer for a control memory with a neat diagram. [15]

8. Derive an algorithm in flowchart form for adding and subtracting two fixed point binary numbers when negative numbers are in the signed-2's complement representation. [15]

---ooOoo---

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Shereguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 **Set – I**

I - Mid Examinations, JAN -2023

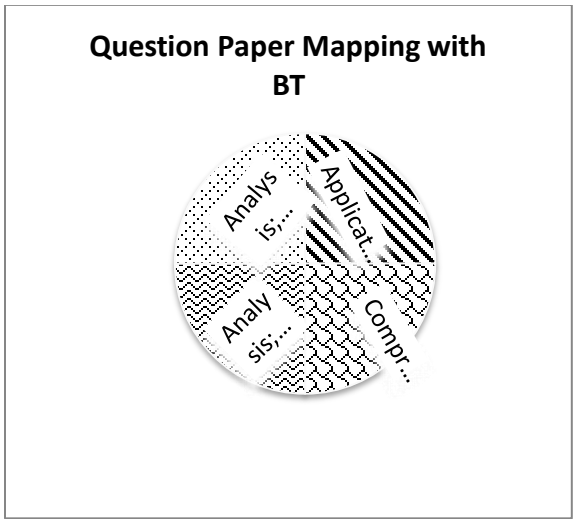
Year &Branch: II CSE-A Date:23-01-2023(FN)

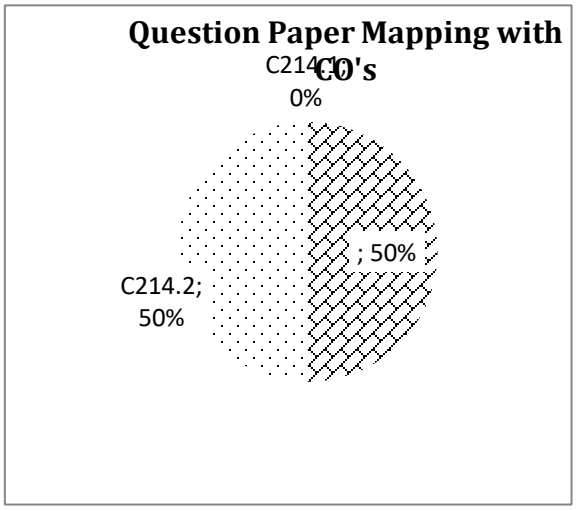
Subject: COA Max. Marks: 10 Time: 60mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

(This question paper is prepared with Course Outcome and BT's mapping)

1	Briefly explain Arithmetic logic shift unit.	(5)	C214.1	(Comprehension)
2.	Draw the Bus system for four registers & Explain.	(5)	C214.1	(Application)
3	Explain about the micro program example.	(5)	C214.2	(Analysis)
4	Draw block diagram of control memory & the associated hardware needed for selecting the next microinstruction address.	(5)	C214.2	(Analysis)





SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Shereguda (V), Ibrahimpatnam (M), R.R.Dist-501 510 **Set – I**

II - Mid Examinations, MAR -2023

Year &Branch: II CSE-A Date:05-03-2023(FN)

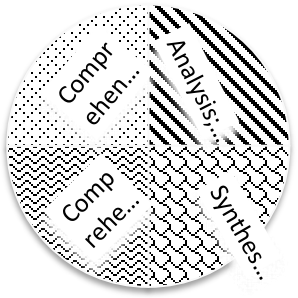
Subject: COA Max. Marks: 10 Time: 60mins

Answer any **TWO** Questions. All Question Carry Equal Marks 2*5=10 marks

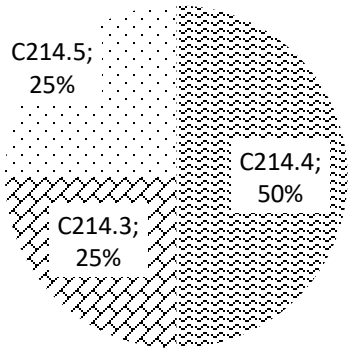
(This question paper is prepared with Course Outcome and BT's mapping)

1	**a)** Differentiate between Isolated I/O and Memory mapped I/O?	(2.5)	C214.4	(Analysis)
	b) Explain Programmed I/O in detail?	(2.5)	C214.4	(Comprehension)
2	What are the various forms available for establishing an interconnection network in a multiprocessor system?	(5)	C214.5	(Synthesis)
3	With an example, explain Booth Multiplication Algorithm?	(5)	C214.3	(Comprehension)
4	Give a neat sketch that illustrates the components in a typical memory hierarchy.	(5)	C214.4	(Comprehension)

Question Paper Mapping with BT



Question Paper Mapping with CO's



Sri Indu Institute of Engineering & Technology

Sheriguda (Vill), Ibrahimpatnam (Mdl), R.R.Dist-501 510

Computer Organization & Architecture (Objective Exam)

B.TECH II YEAR, I SEM, I MID-TERM EXAMS, JAN-2023.

ROLL NO:_____ NAME:_____ MARKS:

Date: 23 .01.2023(FN) **Time: 20 Min.** **Max Marks:10**

Answer All the Questions. All Questions Carry Equal Marks.

I. Choose the correct alternative:

1. The 2's complement of a binary no. is obtained by adding_____to its 1's complement. [ ]
   a)12 b)8 c)2 d)1

2.A register capable of shifting its binary information either to the right or the left is called a [ ]
   a)Parallel register b)Serial register c)Shift register d)Storage register

3. Program counter contents indicate: [ ]
   a)The time elapsed since execution begins
   b) the count of programs being executed after switching the power ON
   c) The address where next instruction is stored
   d) The time needed to execute a program

4. Which part of the computer is used for calculating and comparing? [ ]
   a) Disk unit b) Control unit c) ALU d) Modem

5. Micro Operation is shown as: [ ]
   a) R1→R2 b) R1←R2 c) both d) none

6. Which of the following is a type of architecture used in the computers nowadays? [ ]
   a) Micro architecture b) Harvard architecture
   c) Von Neumann architecture d) System design

7. ____are the different types of generating control signals [ ]
   a) Hardwired b) Microinstruction c) Micro programmed d) both micro programmed and Hardwired

8. Which of the following is the full form of CISC [ ]

a) Complex instruction sequential compilation

b) Complete instruction sequential compilation

c) Complex Integrated sequential Compiler

d) Complex instruction set Computer

9. Which of the following is considered to be the brain of a computer system [ ]
a) Pascal b) Control unit c) CPU d) Memory

10. The length of the one byte instruction is [ ]
a) 2 bytes b) 1 byte c) 3 bytes d) 4 bytes

II. Fill in the blanks:

1. ALU Performs_____operations.
2. The two operations of a stack are the_____and_____.
3. An 8×1 multiplexer contains_____selection lines.
4. An 8-bit register contains the data 11001001.What is the value after circular left shift operation_____.
5. Flip flop stores_____bits of data.
6. The size of the memory in basic computer is_____.
7. The operations executed on data stored in registers are called_____.
8. Abbreviation of SBR_____.
9. In microprogram_____Address bits are using in instruction format.
10. Write the micro operation for symbol INCPC_____.

Sri Indu Institute of Engineering & Technology

Sheriguda (Vill), Ibrahimpatnam (Mdl), R.R.Dist-501 510

Computer Organization & Architecture (Objective Exam)

B.TECH II YEAR, I SEM, II MID-TERM EXAMS, March-2023.

ROLL NO:_____ NAME:_____ MARKS:

Date: 05 .03.2023(FN) **Time: 20 Min.** **Max Marks:10**

Answer All the Questions. All Questions Carry Equal Marks.

I. Choose the correct alternative:

1. How many types of modes of I/O Data Transfer. ( )

a. 2 b. 3 c. 4 d. 5

2. The registers of the controller are_____ ( )

a. 16 bit b. 32 bit c.64 bit d.128 bit

3. The method which offers higher speeds of I/O transfers is_____ ( )

a. Interrupts b. Memory mapping c. Program-controlled I/O d. DMA

4. Depending on mechanism of timing data, data transfer can be ( )

a. synchronous b. asynchronous c. both a &b d. none of the above

5. The DMA controller has_____registers. ( )

a. 4 b.3 c.2 d.5

6. When power is switched off which memory loses its data? ( )

a. Non-Volatile Memory b. Volatile Memory c. Both a and b d. None of the above

7. What is the formula for Hit Ratio? ( )

a. Hit/(Hit + Miss) b. Miss/(Hit + Miss) c. (Hit + Miss)/Miss d. (Hit + Miss)/Hit

8. Which of the following is correct example for Auxiliary Memory? ( )

a. Magnetic disks b. Tapes c. Flash memory d. Both a and b

9. What is the Basic difference between vector and array processors? ( )

a. Register b. Pipelining c. Both a & b d. None of these

10. Which one of the following is true? ( )

a. A+C=0 b. C=A+B c. B=3C d. (B-C)>0

II. Fill in the blanks:

1. is an implementation technique whereby multiple instructions are overlapped during an execution.
2. Array processor is represented in_____
3. Giga bytes are equal to _____
4. A floating point number is said to be normalized, if the most significant bit of the mantissa is _____
5. What is the 2's complement of $(1100)_2$ _____
6. Keyboard and Mouse Comes under? _____
7. The fastest data access is provided using _____
8. How many types of multiprocessors?_____
9. Status bit is also called_____
10. Characteristic of RISC (Reduced Instruction Set Computer) instruction set is _____

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Sheriguda(V),Ibrahimpatnam(M),R.R.Dist-501510

B-Tech I-Mid Examinations,JAN-2023

Year & Branch: II–CSE-A **Date:23-01-2023(FN)**

Subject: COA

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1gnM5VZNl-T5lMw9iHRSL8dYes0uGAYMc/view?usp=sharing

Objective Key Paper

Fill in the blanks:

1. Arithmetic and Logic shift unit
2. Push down, pop up
3. 3
4. 10010011
5. 1
6. 4096×16 bits
7. Micro operation
8. Subroutine register
9. 12
10. Pc←Pc+1

Multiple choice questions:

1 .d	6. C
2. c	7. d
3. c	8.d
4. c	9.c
5. b	10.b

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Sheriguda(V),Ibrahimpatnam(M),R.R.Dist-501510

B-Tech II-Mid Examinations,March-2023

Year & Branch: II–CSE-A **Date:05-03-2023(FN)**

Subject:COA

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/1o09gP9Qz0tANgSIIpzww1Y3Colw3J663/view?usp=sharing

Objective Key Paper

Fill in the blanks:

1. Pipelining
2. SIMD
3. 1024 MB
4. 1
5. $(0100)_2$
6. Input peripherals
7. Registers
8. 2
9. Flag bit
10. One instruction per cycle

Multiple choice questions:

1 .b	9.b
2. b	10.b
3. d	
4. c	
5. b	
6. b	
7. a	
8. d	

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Website: https://siiet.ac.in/

ASSIGNMENT QUESTIONS

ASSIGNMENT-1

(Assignment Questions are mapped with Co's BT)

1. Draw the bus system for 4 registers and explain. (Knowledge) (C214.1)
2. 8-bit register contains the binary value 10011100. What register value after an arithematic shift right & left.(knowledge) (C214.3)
3. Draw the block diagram of control memory and associated hardware needed for selection of next micro instruction address. (knowledge) (C214.2)
4. Draw a flow chart for program interrupt.(Knowledge) (C214.1)
5. List registers for basic computer and give their function in program execution. (Knowledge) (C214.1)
6. Describe the micro programmed control organization and compare its advantages over hardwired control. (Knowledge) (C214.2)
7. Explain the Addressing modes. (Knowledge) (C211.3)

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ASSIGNMENT-2

(Assignment Questions are mapped with Co's BT)

1. Convert the following decimal number to binary
   a)1231 b) 673 c) 1998 (Application)(C214.3)
2. Perform the arithmetic operation (+42) +(-13) and (-42)-(-13) in binary using signed 2's complement representation for negative numbers. (Application)(C214.3)
3. Differentiate between memory mapped I/O and Interrupt I/O. (Knowledge) (C214.4)
4. Explain programmed I/O in detail. (Knowledge) (C214.4)
5. Write the example explain booth multiplication. (Knowledge) (C214.3)
6. Illustrate vector operations and vector processing. (Knowledge) (C214.5)
7. Discuss about pipelining and RISC pipeline. (Knowledge) (C214.5)
8. Explain associated memory hardware organisation in detail. (Knowledge) (C214.4)
9. What is floating point representation explain with example. (Knowledge) (C214.3)

Result Analysis:

Course Title	Computer Organization and Architecture
Course Code	CS304PC
Programme	B.Tech
Year & Semester	II year I-semester, A sec
Regulation	R18
Course Faculty	Dr.D.Sasikumar, Associate Professor , CSE

SLOW LEARNERS STUDENTS

S. No	Roll No	No of backlogs	Internal-I Status	Internal-II Status
1	21X31A0512	5	14-P	17-P
2	21X31A0519	1	22-P	21-P
3	21X31A0539	5	18-P	17-P
4	21X31A0549	3	19-P	17-P
5	21X31A0559	3	22-P	23-P
6	21X31A0565	4	21-P	22-P

ADVANCED LEARNER STUDENTS

S .No	Roll No	(SGPA)	Gate Material
1	21X31A0504	8.1	DMA, Digital computer , Floating point representation, Arthimetic logic shift unit ,Micro programmed sequencer, Common bus system
2	21X31A0506	7.85	
3	21X31A0523	7.75	
4	21X31A0533	7.54	
5	21X31A0540	7.95	
6	21X31A0560	7.71	

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Khalsa Ibrahimpatnam, Sheriguda (V), Ibrahimpatnam (M), Ranga Reddy Dist., Telangana – 501 510

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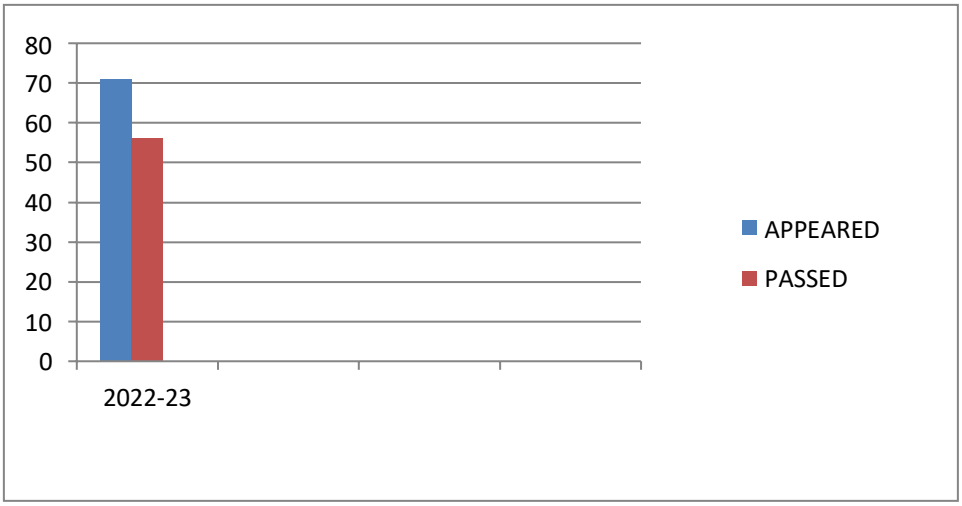
BATCH CSE-II BTECH I SEM CSE-A RESULT ANALYSIS

ACADAMIC YEAR	COURSE NAME	NUMBER OF STUDENTS		QUESTION PAPER SETTING		PASS%
		APPEARED	PASSED	INTERNAL	EXTERNAL	
2022-23	Computer organization and architecture	71	56	COURSE FACULTY	JNTUH	78.87%

COMPUTER ORGANIZATION AND ARCHITECTURE (C214) RESULT ANALYSIS



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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

REMEDIAL CLASSES TIME TABLE

A.Y 2023-24 **SEMESTER-I**

BRANCH/ SEC	MON 4.00 PM-5.00 PM	TUE 4.00 PM-5.00 PM	WED 4.00 PM-5.00 PM	THUR 4.00 PM-5.00 PM	FRI 4.00 PM-5.00 PM
II CSE-A	DE	DS	JAVA	COA	COSM
II CSE-B	DS	DE	COSM	JAVA	COA
II CSE-C	COSM	COA	DE	DS	JAVA
III CSE-A	SE	FLAT	CN	WT	PPL
III CSE-B	WT	CN	SE	PPL	FLAT
III CSE-C	FLAT	WT	PPL	CN	SE
IVCSE-A	C&NS	DM	CC	POE	RTS
IV CSE-B	CC	RTS	C&NS	DM	POE
IV CSE-C	RTS	CC	POE	C&NS	DM

HOD
Computer Science & Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH.
Sheriguda(V), Ibrahimpatnam(M), R.R.Dist-501 510

PRINCIPAL
Principal
Sri Indu Institute of Engineering & Tech
Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana -501 510

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of **Computer Science and Engineering**

Course Outcome Attainment (Internal Examination-1)

Name of the faculty : Dr.D.Sasikumar Academic Year: 2022-23

Examination:

Branch & Section: CSE-A I Internal

Course Name: COA Year: II Semester: I

S.No	HT No.	Q1a	Q1 b	Q2a	Q2 b	Q3a	Q3b	Q4a	Q4 b	Obj1	A1
Max. Marks ==>		**5**		**5**		**5**		**5**		**10**	**5**
1	21X31A0501	5				2				9	5
2	21X31A0502	5				4				9	5
3	21X31A0503	5				4				10	5
4	21X31A0504	5				5				10	5
5	21X31A0505	5				4				9	5
6	21X31A0506	5				5				10	5
7	21X31A0507	4								9	5
8	21X31A0508			5		4				9	5
9	21X31A0509	5		3						6	5
10	21X31A0510	5								5	5
11	21X31A0511	5				4				8	5
12	21X31A0512	5								6	5
13	21X31A0513	4		5						8	5
14	21X31A0514	5				5				6	5
15	21X31A0515	5				4				10	5
16	21X31A0516	5				4				9	5
17	21X31A0517			4		5				9	5
18	21X31A0518	5				3				8	5
19	21X31A0519	4		4						9	5
20	21X31A0520	4		5						8	5
21	21X31A0521	4		4						9	5
22	21X31A0522			5		4				9	5
23	21X31A0523	5				5				9	5
24	21X31A0524	5				4				8	5
25	21X31A0525	5				5				9	5
26	21X31A0526	3				5				10	5
27	21X31A0527	5				4				8	5
28	21X31A0528	4				3				7	5
29	21X31A0529	5		4						8	5
30	21X31A0530	5		3						6	5
31	21X31A0531	3		2						7	5
32	21X31A0532	5		4						8	5
33	21X31A0533	5		5						10	5

34	21X31A0534	5				5				9	5
35	21X31A0535	5								6	5
36	21X31A0536	4		3						8	5
37	21X31A0537	5				3				9	5
38	21X31A0538	5		5						9	5
39	21X31A0539	1				3				9	5
40	21X31A0540	5		5						10	5
41	21X31A0541	4		4						9	5
42	21X31A0542	4		4						9	5
43	21X31A0543			4		4				10	5
44	21X31A0544	5								10	5
45	21X31A0545	4		5						9	5
46	21X31A0546	4								10	5
47	21X31A0547	5								4	5
48	21X31A0548	5		4						9	5
49	21X31A0549					5				9	5
50	21X31A0550	3				5				9	5
51	21X31A0552	4		4						10	5
52	21X31A0554	5				5				7	5
53	21X31A0555	4		3						9	5
54	21X31A0556	5		4						9	5
55	21X31A0557	5		4						10	5
56	21X31A0559	4				4				9	5
57	21X31A0560	5				5				9	5
58	21X31A0561	4				5				9	5
59	21X31A0562	4		5						8	5
60	21X31A0563	5				3				9	5
61	21X31A0564	4		5						9	5
62	21X31A0565	5		3						8	5
63	22X35A0501	4				4				9	5
64	22X35A0502	2		5						9	5
65	22X35A0503	4		3						10	5
66	22X35A0504	4				3				10	5
67	22X35A0505	5				4				9	5
68	22X35A0506			4		4				10	5
69	22X35A0507	5		3						10	5
70	22X35A0508	4				4				10	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	
Number of students performed above the target		47	0	24	0	26	0	0	0	52	0
Number of students attempted		48	0	25	0	27	0	0	0	53	55
Percentage of students scored more than target		98%		96%		96 %				98%	0%

CO Mapping with Exam Questions:

CO - 1	Y		Y				Y		Y	Y
CO - 2					Y				Y	Y
CO - 3									Y	Y
CO - 4										
CO - 5										
CO - 6										
% Students Scored >Target %	98%		96%		96 %				98%	0%

CO Attainment based on Exam Questions:

CO - 1	98%		96%						98%	0%
CO - 2					96 %				98%	0%
CO - 3									98%	0%
CO - 4										
CO - 5										
CO - 6										

CO	Subj	obj	Asgn	Overall	Level
CO-1	97%	98 %	0%	65%	3.00
CO-2	96%	98 %	0%	65%	3.00
CO-3		98 %	0%	49%	1.00
CO-4					
CO-5					
CO-6					

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal 1 Examination) = **2.33**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of **Computer Science and Engineering**

Course Outcome Attainment (Internal Examination-2)

Name of the faculty :	Dr.D.Sasikumar	Academic Year:	2022-23
Branch & Section:	CSE-A	Examination:	II Internal
		Year:	II
Course Name:	COA	Semester:	I

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Obj 2	A2
Max. Marks ==>		5		5		5		5		10	5
1	21X31A0501	0		0						9	5
2	21X31A0502	4		0		4				10	5
3	21X31A0503	4		4						10	5
4	21X31A0504	5				5				10	5
5	21X31A0505			3		4				8	5
6	21X31A0506	5		5						10	5
7	21X31A0507	4				3				9	5
8	21X31A0508	5								4	5
9	21X31A0509	3		3						5	5
10	21X31A0510					5				4	5
11	21X31A0511	5				3				8	5
12	21X31A0512			1		1				5	5
13	21X31A0513	5		5						7	5
14	21X31A0514	4				5				8	5
15	21X31A0515			4		4				8	5
16	21X31A0516	5								4	5
17	21X31A0517	3		4						7	5
18	21X31A0518			3		4				9	5
19	21X31A0519	4				5				7	5
20	21X31A0520	5				4				9	5
21	21X31A0521			5						4	5
22	21X31A0522	4		4						9	5
23	21X31A0523	5				4				10	5
24	21X31A0524			5		5				7	5
25	21X31A0525	5		5						8	5
26	21X31A0526	5				4				9	5
27	21X31A0527			3		4				10	5
28	21X31A0528			5						4	5
29	21X31A0529	5		5						10	5
30	21X31A0530	5		4						10	5

31	21X31A0531	5								7	5

32	21X31A0532			3		2				9	5
33	21X31A0533	5				4				9	5
34	21X31A0534	5		5						9	5
35	21X31A0535			5						6	5
36	21X31A0536	3		4						6	5
37	21X31A0537					4				6	5
38	21X31A0538	5				4				8	5
39	21X31A0539	2		2						8	5
40	21X31A0540	5		5						9	5
41	21X31A0541	2		3						10	5
42	21X31A0542	4				5				10	5
43	21X31A0543			3		4				8	5
44	21X31A0544	5								6	5
45	21X31A0545	5		5						8	5
46	21X31A0546	1				1				10	5
47	21X31A0547			4						5	5
48	21X31A0548			3		4				7	5
49	21X31A0549	3		3						6	5
50	21X31A0550	3				3				6	5
51	21X31A0552			3		4				6	5
52	21X31A0554	5		5						9	5
53	21X31A0555	3		3						8	5
54	21X31A0556			4		4				9	5
55	21X31A0557			4		5				8	5
56	21X31A0559	4		5						9	5
57	21X31A0560	5				5				10	5
58	21X31A0561			4		5				9	5
59	21X31A0562	5		5						9	5
60	21X31A0563	4				3				7	5
61	21X31A0564			5		5				9	5
62	21X31A0565	4		5						8	5
63	22X35A0501	5		4						10	5
64	22X35A0502			5		5				9	5
65	22X35A0503	3				4				9	5
66	22X35A0504	4		3						9	5
67	22X35A0505			5		4				10	5
68	22X35A0506	3				4				7	5
69	22X35A0507	4		3						7	5
70	22X35A0508	4		5						8	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		40	0	39	0	31	0	0	0	58	70

Number of students attempted	44	0	43	0	34	0	0	0	60	70
Percentage of students scored more than target	91%		91%		91 %				97%	100 %

CO Mapping with Exam Questions:

CO - 1										
CO - 2										
CO - 3		Y							Y	Y
CO - 4	Y								Y	Y
CO - 5			Y						Y	Y
CO - 6					Y		Y		Y	Y

CO Attainment based on Exam Questions:

CO - 1										
CO - 2										
CO - 3									97%	100 %
CO - 4	91%								97%	100 %
CO - 5			91%						97%	100 %
CO - 6					91 %				97%	100 %

CO	**Subj**	obj	Asgn	Overall	Level
CO-1					
CO-2					
CO-3		97 %	100 %	98%	3.00
CO-4	91%	97 %	100 %	96%	3.00
CO-5	91%	97 %	100 %	96%	3.00
CO-6	91%	97 %	100 %	96%	3.00

Attainment (Internal Examination-2) = **3.00**

Attainment Level	
1	40%
2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of **Computer Science and Engineering**

Course Outcome Attainment (University Examinations)

Name of the faculty: Dr.D.Sasikumar
Academic Year: 2022-23
Branch & Section: CSE-A
Year / Semester: II / I
Course Name: COA

S.No	Roll Number	Marks Secured
1	21X31A0501	26
2	21X31A0502	27
3	21X31A0503	28
4	21X31A0504	36
5	21X31A0505	27
6	21X31A0506	32
7	21X31A0507	15
8	21X31A0508	26
9	21X31A0509	28
10	21X31A0510	10
11	21X31A0511	29
12	21X31A0512	2
13	21X31A0513	47
14	21X31A0514	31
15	21X31A0515	27
16	21X31A0517	37
17	21X31A0518	26
18	21X31A0519	38
19	21X31A0520	40
20	21X31A0521	26
21	21X31A0522	28
22	21X31A0523	36
23	21X31A0524	28
24	21X31A0525	60
25	21X31A0526	38
26	21X31A0527	13
27	21X31A0528	2
28	21X31A0529	11
29	21X31A0530	26
30	21X31A0531	26
31	21X31A0532	31
32	21X31A0533	41
33	21X31A0534	36

S.No	Roll Number	Marks Secured
35	21X31A0536	10
36	21X31A0537	46
37	21X31A0538	26
38	21X31A0539	9
39	21X31A0540	43
40	21X31A0541	26
41	21X31A0542	34
42	21X31A0543	26
43	21X31A0544	26
44	21X31A0545	38
45	21X31A0546	30
46	21X31A0547	29
47	21X31A0548	36
48	21X31A0549	8
49	21X31A0550	26
50	21X31A0552	12
51	21X31A0554	48
52	21X31A0555	28
53	21X31A0556	15
54	21X31A0557	26
55	21X31A0558	8
56	21X31A059	8
57	21X31A0560	8
58	21X31A0561	8
59	21X31A0562	8
60	21X31A0563	8
61	21X31A0564	8
62	21X31A0565	56
63	22X35A0501	48
64	22X35A0502	15
65	22X35A0503	61
66	22X35A0504	35
67	22X35A0505	15

34	21X31A0535	42		68	22X35A0506	14
				69	22X35A0507	50
				70	22X35A0508	45
Max Marks 75						

Class Average mark	25
Number of students performed above the target	48
Number of successful students	69
Percentage of students scored more than target	70%
Attainment level	**3**

Attainment Level	**% students**
1	40%
2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of **Computer Science and Engineering**

Course Outcome Attainment

Name of the faculty :	Dr.D.Sasikumar	Academic Year:	2022-23
Branch & Section:	CSE-A	Examination:	I Internal
Course Name:	COA	Year:	II
		Semester:	I

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00		3.00	3.00	3.00
CO2	3.00		3.00	3.00	3.00
CO3	1.00	3.00	2.00	3.00	2.75
CO4		3.00	3.00	3.00	3.00
CO5		3.00	3.00	3.00	3.00
CO6		3.00	3.00	3.00	3.00
Internal & University Attainment:			2.83	3.00	
Weightage			25%	75%	
CO Attainment for the course (Internal, University)			0.71	2.25	
CO Attainment for the course (Direct Method)			2.96		

Overall course attainment level **2.96**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of **Computer Science and Engineering**

Program Outcome Attainment (from Course)

Name of Faculty:	Dr.D.Sasikumar	Academic Year:	2022-23
Branch & Section:	CSE-A	Year:	II
Course Name:	COA	Semester:	I

CO-PO mapping

PO/PSO/ CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C214.1	3	-	-	-	-	-	1	-	-	-	-	2	1	2
C214.2	3	-	-	-		-	-	-	1	-	-	1	2	1
C214.3	2	-	-	-	3	-	-	-	-	-	-	-	1	2
C214.4	3	-	-	-	-	-	-	1	-	-	-	-	2	1
C214.5	3	2	1	-	-	-	-	-	-	-	-	-	1	1
C214.6	3	3	-	-	2	1	-	-	-	2	-	-	1	2
Course	**2.9**	**2.5**	**1**	**-**	**2.5**	**1**	**1**	**1**	**1**	**2**	**-**	**1.5**	**1.3**	**1.5**

CO	Course Outcome Attainment
CO1	3.00
CO2	3.00
CO3	2.75
CO4	3.00
CO5	3.00
CO6	3.00
Overall course attainment level	**2.96**

PO-ATTAINMENT

	PO1	PO2	PO3	PO 4	PO 5	PO 6	PO7	PO8	PO9	PO10	PO11	PO12
CO Attainment	**2.56**	**2.56**	**2.17**	**2.37**	**2.07**	-	-	-	-	-	-	**2.47**

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

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(Approved by AICTE,NewDelhi and Affiliated to JNTUH, Hyderabad)

Khalsa Ibrahimpatnam, Sheriguda (V),Ibrahimpatnam(M),RangaReddy Dist.,Telangana–501510
Website: https://siiet.ac.in/

ASSIGNMENTS AND REGISTERS

Assignment 1 scrift link:

https://drive.google.com/file/d/1b8awES9UZMQISDfRdHmS8EJ1zz9w4s0a/view?usp=sharing

Assignment 2 scrift link:

https://drive.google.com/file/d/1DUdU2HJeM-52LQOVDZjTVhIjkIpudhtf/view?usp=sharing

Attendance register link:

https://drive.google.com/file/d/1FSZ2UTdgDXahiueBVu0xiROx-bmz7RcA/view?usp=sharing