



ESTD : 2007



Sri Indu Institute of Engineering and Technology (Autonomous)

(Formerly RVR Institute of Engineering & Technology)

An Autonomous Institution Under UGC

NAAC Accredited. Recognized Under 2(f) of UGC Act 1956

Approved by AICTE, New Delhi, & Affiliated to JNTUH, Hyderabad.

JNTUH CODE: X3

EAMCET CODE: INDI

COURSE FILE

ON

ELECTRONIC DEVICES & CIRCUITS

Course Code – EC201ES

I-B. Tech Semester-II

A.Y. 2022-2023

Prepared by

Mrs.D.ARUNA KUMARI

Asst. Professor

Head of the Department
Department of H&S
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(VIII) Ibrahimpatnam (M) R.R. Dist-501 510

PRINCIPAL
Sri Indu Institute of Engineering & Techn.
Sheriguda(VIII), Ibrahimpatnam
R.R. Dist. Telangana-501 510.



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INSTITUTE VISION & MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

- **IM1:** To offer outcome-based education and enhancement of technical and practical skills.
- **IM2:** To Continuous assess of teaching-learning process through institute-industry collaboration.
- **IM3:** To be a center of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.
- **IM4:** To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

Head of the Department
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PROGRAM OUTCOMES

PO1: ENGINEERING KNOWLEDGE: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: PROBLEM ANALYSIS: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: DESIGN/DEVELOPMENT OF SOLUTIONS: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: MODERN TOOL USAGE: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO6: THE ENGINEER AND SOCIETY: Apply reasoning informed by the contextual knowledge to associate, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: ENVIRONMENT AND SUSTAINABILITY: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: ETHICS: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: INDIVIDUAL AND TEAM WORK: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: COMMUNICATION: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

PO11: PROJECT MANAGEMENT AND FINANCE: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: LIFE-LONG LEARNING: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change


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SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
B.Tech. in COMPUTER SCIENCE AND ENGINEERING (AI & ML)
COURSE STRUCTURE, I YEAR SYLLABUS (BR22 Regulations)

Applicable from Academic Year: 2022-23 Batch

I Year I Semester

I Year I Semester

S. No.	Course Code	Course Title	L	T	P	Credits
1.	MA101BS	Matrices and Calculus	3	1	0	4
2.	AP102BS	Applied Physics	3	1	0	4
3.	CS103ES	Programming for problem solving	3	0	0	3
4.	ME102ES	Engineering Workshop	0	1	3	2.5
5.	EN104HS	English for Skill Enhancement	2	0	0	2
6.	CS106ES	Elements of Computer Science & Engineering	0	0	2	1
7.	AP105BS	Applied Physics Laboratory	0	0	3	1.5
8.	CS107ES	Programming for problem solving Laboratory	0	0	2	1
9.	EN107HS	English Language and Communication Skills Laboratory	0	0	2	1
10.	*MC101ES	Environmental Science	3	0	0	0
11.		Induction Programme				
		Total	14	3	12	20

I Year II Semester

S. No.	Course Code	Course Title	L	T	P	Credits
1.	MA201BS	Ordinary Differential Equations and Vector Calculus	3	1	0	4
2.	CH203BS	Engineering Chemistry	3	1	0	4
3.	ME201ES	Computer Aided Engineering Graphics	1	0	4	3
4.	EE201ES	Basic Electrical Engineering	2	0	0	2
5.	EC201ES	Electronic Devices and Circuits	2	0	0	2
6.	CH206BS	Engineering Chemistry Laboratory	0	0	2	1
7.	EE202ES	Basic Electrical Engineering Laboratory	0	0	2	1
8.	CS201ES	Python Programming Laboratory	0	1	2	2
9.	CS203ES	IT Workshop	0	0	2	1
		Total	11	3	12	20

Course Objectives:

1. To introduce components such as diodes, BJTs and FETs.
2. To know the applications of devices.
3. To know the switching characteristics of devices.

Course Outcomes: Upon completion of the Course, the students will be able to:

1. Acquire the knowledge of various electronic devices and their use on real life.
2. Know the applications of various devices.
3. Acquire the knowledge about the role of special purpose devices and their applications.

UNIT - I

Diodes: Diode - Static and Dynamic resistances, Equivalent circuit, Diffusion and Transition Capacitances, V-I Characteristics, Diode as a switch- switching times.

UNIT - II

Diode Applications: Rectifier - Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Rectifiers with Capacitive and Inductive Filters, Clippers-Clipping at two independent levels, Clamper-Clamping Circuit Theorem, Clamping Operation, Types of Clampers.

UNIT - III

Bipolar Junction Transistor (BJT): Principle of Operation, Common Emitter, Common Base and Common Collector Configurations, Transistor as a switch, switching times,

UNIT - IV

Junction Field Effect Transistor (FET): Construction, Principle of Operation, Pinch-Off Voltage, Volt-Ampere Characteristic, Comparison of BJT and FET, FET as Voltage Variable Resistor, MOSFET, MOSTET as a capacitor.

UNIT – V

Special Purpose Devices: Zener Diode - Characteristics, Zener diode as Voltage Regulator, Principle of Operation - SCR, Tunnel diode, UJT, Varactor Diode, Photo diode, Solar cell, LED, Schottky diode.

TEXT BOOKS:

1. Jacob Millman - Electronic Devices and Circuits, McGraw Hill Education
2. Robert L. Boylestead, Louis Nashelsky- Electronic Devices and Circuits theory, 11th Edition, 2009, Pearson.

REFERENCE BOOKS:

1. Horowitz -Electronic Devices and Circuits, David A. Bell – 5th Edition, Oxford.
2. Chinmoy Saha, Arindam Halder, Debaati Ganguly - Basic Electronics-Principles and Applications, Cambridge, 2018.



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**Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist.,
Telangana – 501510**

Course: Electronic Devices and Circuits

Class: I- B TECH- CSE(AI&ML)

Course Outcomes

After completing this course the student will be able to:

C125.1: Acquire the knowledge of diode with the help of V-I characteristics. (Understand)

C125.2: Analyze the applications of diode. (Analyze)

C125.3: Understand the principle of operation of BJT. (Understand)

C125.4: Know the characteristics of BJT under various biasing conditions. (Applying)

C125.5: Interpret the construction, operation and characteristics of FET. (Understand)

C125.6: Analyze the performance of special purpose devices and their applications. (Analyze)

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO / CO	PO 1	PO2	PO3	PO4	PO5	P O 6	PO 7	PO 8	PO 9	PO 10	PO1 1	PO12	PSO1	PSO2
C125.1	3	2	-	-	3	-	-	-	-	-	2	3	3	3
C125.2	-	1	3	-	-	-	1	-	-	-	2	2	3	3
C125.3	1	3	-	-	2	1	-	-	-	-	2	-	3	3
C125.4	2	-	2	2	-	-	-	-	-	-	2	3	3	3
C125.5	2	3	3	-	3	-	-	1	-	-	2	2	3	3
C125.6	3	3	-	-	3	-	-	-	1	1	2	3	3	3
C125	2.20	2.40	2.67	2.00	2.75	1	1	1	1	1	2.00	2.60	3.00	3.00



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CO-PO mapping Justification

C125.1: Acquire the knowledge of diode with the help of V-I characteristics. (Understand)

	Justification
PO1	Applying basic knowledge on Electronic Devices And Circuits students can solve basic circuit problems.
PO2	Engineering problems often involve the proper utilization of diodes in electronic circuits. Identifying issues related to diode behavior is crucial for effective problem-solving.
PO5	Acquiring knowledge of diode V-I characteristics through the use of modern simulation tools aligns with PO Modern Tool Usage. The integration of simulation software enables engineers to create, select, and apply appropriate techniques for predicting and modeling diode behavior.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Students can continuously learning to explore more knowledge in semiconductor devices.
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

C125.2: Analyze the applications of diode. (Analyze)

	Justification
PO2	Students can analyze the rectifier, clippers, clamper Circuits using loop equations.
PO3	Students can design the different transistor configuration circuits.
PO7	Engineers focusing on sustainable development can leverage diodes and their applications to design energy-efficient systems, develop renewable energy technologies, and create environmentally friendly products.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Students can continuously learning to explore more knowledge in semiconductor devices.

PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

C125.3: Understand the principle of operation of BJT. (Understand)

	Justification
PO1	Understanding the principle of operation of a BJT involves the application of mathematics, science, engineering fundamentals, and specialization in electronics.
PO2	Understanding the principle of operation of a BJT is crucial for problem analysis in electronic engineering. By identifying, formulating, and analyzing complex engineering problems related to BJT behavior, engineers can reach substantiated conclusions.
PO5	Applying simulation tools to visualize and analyze BJT characteristics, including V-I curves.
PO6	Engineers applying BJTs or any technology must assess the broader societal, health, safety, legal, and cultural impacts of their work.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

C125.4: Know the characteristics of BJT under various biasing conditions. (Applying)

	Justification
PO1	Engineers must apply mathematical models, semiconductor physics, and circuit theory to solve complex engineering problems related to BJT biasing and amplifier design.
PO3	The characteristics of BJTs under various biasing conditions play a crucial role in the design and development of engineering solutions. Engineers need to consider these characteristics to design system components or processes that meet specified needs, taking into account public health and safety, as well as cultural, societal, and environmental considerations.
PO4	Engineers, through research-based knowledge, can conduct experiments, analyze data, and synthesize information to draw valid conclusions about BJT behavior.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Students can continuously learning to explore more knowledge in semiconductor devices.

PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

C125.5: Interpret the construction, operation and characteristics of FET. (Understand)

	Justification
PO1	The knowledge of FET principles serves as a foundation for solving complex engineering problems related to electronic circuits and systems.
PO2	Recognizing challenges in electronic circuit design and signal processing that involve FET behavior.
PO3	Students, equipped with this knowledge, can design solutions for complex engineering problems, create system components using FETs, and consider health, safety, environmental, cultural, and societal factors in their designs.
PO5	Students can apply small signal model techniques in the design of FET amplifiers.
PO8	By understanding the construction, operation, and characteristics of FETs, engineers can responsibly and ethically apply this technology.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Students can continuously learning to explore more knowledge in semiconductor devices.
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

C125.6: Analyze the performance of special purpose devices and their applications. (Analyze)

	Justification
PO1	Students get the knowledge on special purpose devices like Zener, Tunnel, varactor diode, UJT, SCR to simplify the complex circuits for analysis.
PO2	Stude Students can design the special purpose devices like Zener, Tunnel, varactor diode, UJT, SCR .
PO5	Students can apply transistor hybrid model techniques in the design of BJT amplifiers.
PO9	Individuals equipped with expertise in the performance of these devices can effectively tackle complex problems or challenges that require the utilization of such technology. They can provide innovative solutions by leveraging their understanding of device capabilities.

PO10	Understanding device performance allows engineers to provide clear and precise instructions for integrating these devices into larger systems or for their specific applications.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Understanding the performance of special purpose devices places learning within the broader context of technological change.
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.



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Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist, Telangana - 501 510

<https://siiet.ac.in/>

Lr. No. SIET/BR22/Academic Calendar/2022/02

Date: 15.12.2022

REVISED ACADEMIC CALENDAR I B.TECH FOR THE ACADEMIC YEAR 2022-23 (BR22-REGULATIONS)

Dr. I. Satyanarayana,
Principal.

X3

To,
All the HOD's
Sir,

Sub: SIET (Autonomous)-Academic & Evaluation-Revised Academic Calendar for I B.Tech - I & II Semesters for the academic year 2022-2023-Reg.

The approved Academic Calendar for I B.Tech - I & II Semesters for the academic year 2022-23 is given below.

I-SEMESTER

S. NO	Description	Period		Duration
		From	To	
1.	Commencement of I Semester class work (including Induction programme)	03.11.2022		
2.	1 st Spell of Instructions	03.11.2022	28.12.2022	8 Weeks
3.	I Mid Examinations	29.12.2022	04.01.2023	1 Week
4.	Submission of First Mid Term Exam Marks to the Autonomous Section on or before	10.01.2023		
5.	2 nd Spell of Instructions	05.01.2023	02.03.2023	8 Weeks
6.	Second Mid Term Examinations	03.03.2023	09.03.2023	1 Week
7.	Preparation & Practical Examinations	10.03.2023	16.03.2023	1 Week
8.	Submission of Second Mid Term Exam Marks to the Autonomous Section on or before	16.03.2023		
9.	I Semester End Examinations	17.03.2023	01.04.2023	2 Weeks

II-SEMESTER

S. NO	Description	Period		Duration
		From	To	
1.	Commencement of II Semester class work	03.04.2023		
2.	1 st Spell of Instructions (including Summer Vacation)	03.04.2023	10.06.2023	10 Weeks
	Summer Vacation	15.05.2023	27.05.2023	2 Weeks
3.	I Mid Examinations	12.06.2023	17.06.2023	1 Week
4.	Submission of First Mid Term Exam Marks to the Autonomous Section on or before	23.06.2023		
5.	2 nd Spell of Instructions	19.06.2023	12.08.2023	8 Weeks
6.	II Mid Term Examinations	14.08.2023	19.08.2023	1 Week
7.	Preparation & Practical Examinations	21.08.2023	26.08.2023	1 Week
8.	Submission of Second Mid Term Exam Marks to the Autonomous Section on or before	26.08.2023		
9.	II Semester End Examinations	28.08.2023	09.09.2023	2 Weeks

Commencement of Class Work for II B.Tech I Semester - 11.09.2023

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Class:AI&ML-A Semester: II W.E.F-03-04-2023

LH:-D-105

	I 9:40- 10:30	II 10:30 - 11:20	III 11:20- 12:10	12:10- 12:45	IV 12.45- 1.35	V 1.35- 2.25	VI 2.25- 3.15	VII 3.15-4.00
MON	EC/BEE LAB			L U N C H	EC	EDC	BEE	PYTHON(T)
TUE	EDC	ODE	EC		PYTHON LAB			ODE(T)/EC(T)
WED	CAEG PRACTICE				BEE	ODE	EDC	EDC(T)/ BEE(T)
THU	BEE	ODE	BEE		ITWS LAB			EC(T)/ODE(T)
FRI	EC/BEE LAB				ODE	EC	EDC	LIBRARY
SAT	BEE	ODE	EC		CAEG PRACTICE			BEE(T)/EDC(T)

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the Faculty
MA201BS	ODE-Ordinary Differential Equations & Vector Calculus	V.SRINIVAS	CH206BS	EC LAB Engineering Chemistry Laboratory	Dr.D.PREMALATHA / K.MOUNIKA
CH203BS	EC-Engineering Chemistry	Dr.D.PREMALATHA	EE202ES	BEE LAB-Basic Electrical Engineering Laboratory	K.RAJASHEKAR/S. NISCHALA
ME201ES	CAEG-Computer Aided Engineering Graphics	M.YADHAGIRI	CS201ES	PYTHON Programming Laboratory	M.TEJASWI/P.BALU
EE201ES	BEE-Basic Electrical Engineering	K.RAJASHEKAR	CS203ES	ITWS-IT Workshop	N.KEERTHI CHANDANA/B.SWATHI
EC201ES	EDC-Electronic Devices & Circuits	P.ARUNA KUMARI			

[Signature]
Class In-Charge

[Signature]
Time Table Coordinator



[Signature]
Head of The Department
Sri Indu Institute of Engg. & Tech
Main Road, Sheriguda(V)
Ibrahimpatnam(M), R. P. Dist.,
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LESSON PLAN

S.N O	Unit	TOPIC	Numbe r of Sessions Planned	Teaching method/Aids	REFERENCE
1.	1	Introduction to diode	1	Black Board	R1,T1,PPT
2.		Static resistance and dynamic resistances	1	Black Board	R1,T1
3.		Diode Equivalent circuits	1	Black Board	R1,T1
4.		Diffusion Transition and Capacitances	1	Black Board	R1,T1
5.		Volt Ampere Characteristic of a diode	1	Black Board	R1,T1,PPT
6.		Diode as a switch	1	Black Board	R1,T1,PPT
7.		Diode switching times	1	Black Board	R1,T1
8.		Revision	1	Black Board	R1,T1,T2
9.	2	Half wave Rectifier	1	Black Board	R2,T1,T2
10		Full Wave Rectifier	1	Black Board	R1,T1,T2
11		Bridge Rectifier	1	Black Board	R2,T1
12		Inductor Filters, Capacitor filters	1	Black Board	R2,T1,T2
13		Clipper-clipping at two independent levels	1	Black Board	T2
14		Clamping circuit theorem	1	Black Board	T2
15		Clamping operation	1	Black Board	T2
16		Types of clampers	1	Black Board	T2

17		Problems on half wave and Full wave Rectifier	1	Black Board	T2,T1
18	3	Principle of Operation of BJT	1	Black Board, PPT	T2,PPT
19		Common emitter Configuration	1	Black Board	T2,T1,PPT
20		Efficiency calculation in CE	1	Black Board	T2,W1
21		Common base configuration	1	Black Board	T2,PPT
22		Efficiency calculation in CB	1	Black Board	T2,PPT
23		Common collector configuration	1	Black Board	T2,T1,W1,PPT
24		Efficiency calculation in CC	1	Black Board	T2,PPT
25		Transistor as switch		Black Board	T1
26		Transistor switching times		Black Board	T1
27		4	Junction Field Effect Transistor (FET) Construction	1	Black Board
28	Principle of Operation of FET		1	Black Board	T1,T2,W2
29	Pinch-Off Voltage,		1	Black Board	T1,T2
30	Volt-Ampere Characteristic		1	Black Board	T1,T2,W2
31	Comparison of BJT and FET		1	Black Board	T1,T2,W2
32	FET as Voltage Variable Resistor		1	Black Board	T1,T2,W2
33	MOSFET introduction		1	Black Board	T1
34	Depletion mode MOSTET as a capacitor		1	Black Board	T1
35	Enhancement mode		1	Black Board	T1,T2
36	MOSTET as a capacitor		1	Black Board	T1
37		Special Purpose Devices introduction	1	Black Board	T1,T2,W3
38		Zener Diode - Characteristics	1	Black Board	T1

39	5	Zener diode as Voltage Regulator	1	Black Board	T1,T2
40		Principle of Operation - SCR	1	Black Board	T1
41		Tunnel diode	1	Black Board	T1
42		UJT	1	Black Board	T1,T2
43		Varactor Diode	1	Black Board	T1
44		Photo diode, Schottky diode	1	Black Board	T1,T2
45		Solar cell,LED	1	Black Board	T1,W3

TEXT BOOKS:

1. Jacob Millman - Electronic Devices and Circuits, McGraw Hill Education
2. Robert L. Boylestead, Louis Nashelsky- Electronic Devices and Circuits theory, 11th Edition,2009, Pearson.

REFERENCE BOOKS:

1. Horowitz -Electronic Devices and Circuits, David A. Bell – 5thEdition, Oxford.
2. Chinmoy Saha, Arindam Halder, Debaati Ganguly - Basic Electronics-Principles and Applications, Cambridge, 2018.



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Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana – 501510

WEB REFERENCES:

W1. <https://www.rfwireless-world.com/Terminology/CB-vs-CE-vs-CC-transistor-configurations.html>

W2. <http://www.faadooengineers.com/online-study/post/ece/analog-electronics/557/fet-as-a-voltage-variable-resistor-vvr>

W3. https://www.tutorialspoint.com/basic_electronics/basic_electronics_special_purpose_diodes.htm

W4. http://ggn.dronacharya.info/ECEDept/Downloads/QuestionBank/VIIsem/oc_C-Unit-3-LED_Structures.pdf



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Telangana – 501510**

LECTURE NOTES

UNIT – 1 Diodes

https://drive.google.com/file/d/1GX10RkXW5nT11EYgosG9gxpRBYdwEIT/view?usp=drive_link

UNIT-2 Diode Applications

https://drive.google.com/file/d/1QkCNWI9nDZJEke3Y_uwngswXCgZSwTSj/view?usp=drive_link

UNIT-3 Bipolar Junction Transistor (BJT)

https://drive.google.com/file/d/1QOD0nKU5BjyQv78Ih3PzHqs6hqli7Li/view?usp=drive_link

UNIT-4 Junction Field Effect Transistor (FET)

https://drive.google.com/file/d/1ykPUrK6oekjH5SbCSAWgTGOi6HbdD0io/view?usp=drive_link

UNIT-5 Special Purpose Devices

https://drive.google.com/file/d/1P5mFC9O8nAep4NPiANcx4iMCCWDzHnAe/view?usp=drive_link



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POWER POINT PRESENTATION LINKS

UNIT-1

<https://drive.google.com/file/d/1gXb7UaRibe0VGHm6PN3KbhosS1V-nZxU/view?usp=sharing>

UNIT-2

<https://drive.google.com/file/d/1KdQE27vDIWazVJMU8MUK84f139Ssy1EY/view?usp=sharing>



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PREVIOUS QUESTION PAPERS

Link:

https://drive.google.com/file/d/1KH9dftl_RLJWQ1idPCHak3D76Agn_i7/view?usp=drive_link



SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
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Set-I

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Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana –
501510

I B. TECH II SEM I – MID Examinations, Jun-2023

BR22

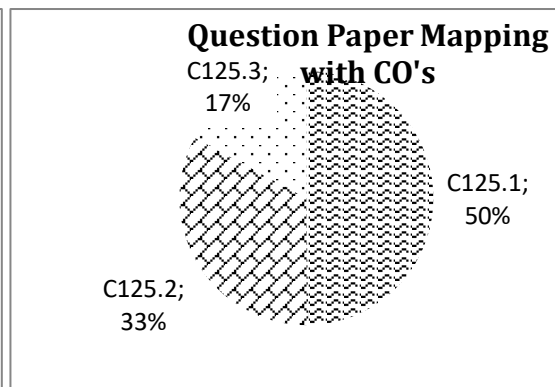
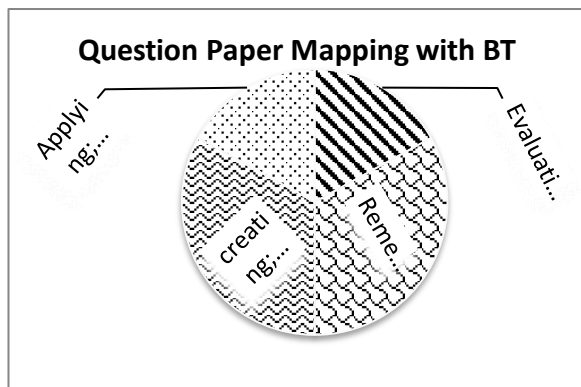
Branch: ECE, CSE (A,B,C), IOT, AI&DS, DS,CS, AI&ML Date: 15-06-2023(FN)
Subject: ELECTRONIC DEVICES AND CIRCUITS Marks: 20 Time: 2 Hours

PART-B

Answer any FOUR Questions. All question Carry Equal Marks

4*5 =20 Marks

- 1 Explain the working of P-N Junction under forward bias & Reverse bias? (C125.1) (Evaluating)
- 2 Define static & dynamic resistances? Derive the expression for dynamic resistance? (C125.1) (Remembering)
- 3 Design the Equivalent circuit of Diode with brief explanation. (C125.1) (Applying)
- 4 Draw a circuit diagram of a Bridge full wave rectifier. Explain its working and draw the input and output waveforms? (C125.2) (Creating)
- 5 Define clipper? Explain any two unbiased clippers with waveforms? (C125.2) (Remembering)
- 6 Construct & Explain the operation of NPN Transistor? (C125.3) (Creating)





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Sheriguda(V), Ibrahimpatnam(M), R.R Dist., Telangana – 501 510

I B.Tech II SEM I-Mid Examinations, June-2023

Branch: **ECE, CSE(A,B,C), IOT, AI&DS, DS, CS,AI&ML**

Subject Name: **Electronic Devices & Circuits**

Student Name: H.T.No.:

Part-A
Objective/Quiz Paper:

The objective/quiz paper is set with multiple choice, fill-in the blanks and match the following type of questions for a total of 10 marks.

Multiple choices:

1. How many Terminals does a P-N Junction Contains----- ()
a) 3 b) 4 c) 2 d) 1
2. What is the cut-in voltage of silicon PN-Junction diode----- ()
a) 0.3 b) 0.7 c) 1.1 d) 0.2
3. What is the efficiency of Half wave rectifier----- ()
a) 81.2% b) 40.6% c) 73.5% d) 78%
4. The number of depletion regions in a transistor----- ()
a) 3 b)2 c)4 d)1

Fill-in the blanks

1. The process of adding impurities to pure semiconductors is called_____.
2. The unwanted ac components present in the output of rectifier is called_____.
3. Positive clipper circuit removes _____ portion of a wave forms .
4. In NPN transistor,_____ are the minority carriers.

Match the following:

9.

- | | | |
|-------------------------------|--------|-------------------------|
| i. Static Resistance | () | a. Forward bias |
| ii. Dynamic Resistance | () | b. Reverse bias |
| iii. Transition Capacitance | () | c. V/I |
| iv. Diffusion Capacitance | () | d. $\Delta V/ \Delta I$ |



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Sheriguda(V), Ibrahimpatnam(M), R.R Dist., Telangana – 501 510

I B.Tech II SEM I-Mid Examinations, June-2023
Subject Name: **Electronic Devices & Circuits**

Set-I

BR22

ANSWER KEY

Descriptive paper key link:

<https://drive.google.com/file/d/1XQDxsXsSM0k9eHgx-EDBrZe05bDT7pr1/view?usp=sharing>

Objective Key Paper

Multiple choices:

1. c
2. b
3. b
4. b

Fill in the blanks:

5. Doping
6. Ripples
7. Positive
8. Electrons

Match the following:

9.
 - i. c
 - ii. d
 - iii. b
 - iv. a



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Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist.,
Telangana – 501510

I B. TECH II SEM II – MID Examinations, August-2023

Set-II

BR22

Branch: ECE, CSE(A,B,C), IOT, AI&DS, DS, CS,AI&ML Date: 18-08-2023(FN)

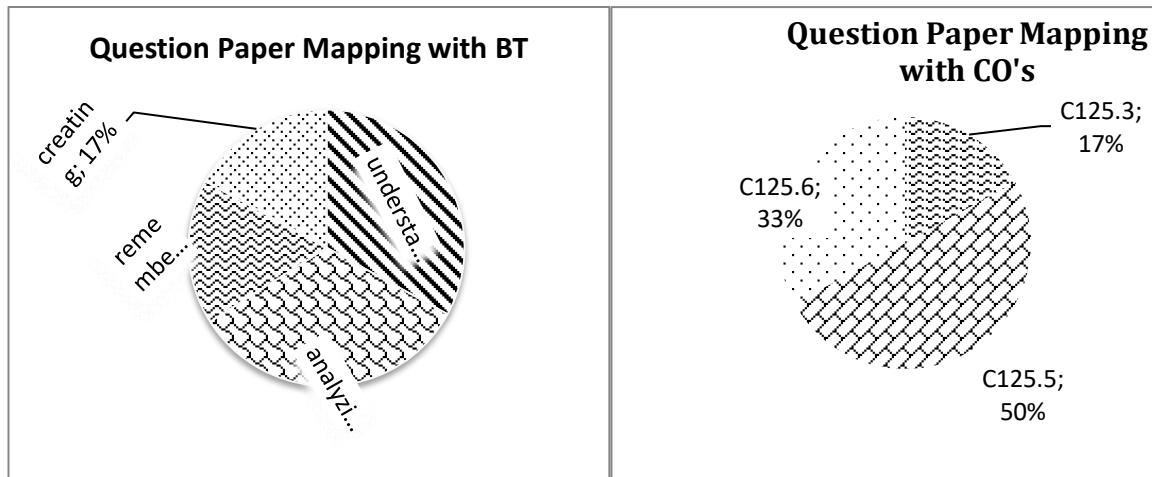
Subject: ELECTRONIC DEVICES AND CIRCUITS Marks: 20 Time: 2 Hours

PART-B

Answer any **FOUR** Questions. All question Carry Equal Marks

4*5 =20 Marks

- 1 Explain how the transistor acts as a switch ? (C125.3) (Understanding)
- 2 Distinguish Between BJT & JFET? (C125.5) (Analyzing)
- 3 Discuss the V-I characteristics of JFET? (C125.5) (Creating)
- 4 Compare JFET & MOSFET? (C125.5) (Analyzing)
- 5 Define UJT ? Explain the operation of UJT? (C125.6) (Remembering)
- 6 Demonstrate the construction &Working of Photo Diode? (C125.6) (Understanding)





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Telangana – 501510

Set-II

I B.Tech II SEM II-Mid Examinations, August-2023

Branch: ECE, CSE(A,B,C), IOT, AI&DS, DS,CS, AI&ML

BR22

Subject Name: **Electronic Devices & Circuits**

Student Name: H.T.No.:

Part-A
Objective/Quiz Paper:

The objective/quiz paper is set with multiple choice, fill-in the blanks and match the following type of questions for a total of 10 marks.

Multiple choices:

1. What is the input terminal of CB Configuration? ()
a) Base b) Collector c) Emitter d) None of the above
- 2 How many P-Regions are present in N-Channel MOSFET? ()
a) 2 b)3 c)4 d)1
3. A JFET has three terminals, namely ()
a)cathode, anode, grid b) emitter, base, collector c)source, gate, drain d)None of the Above
4. Zener diode is used as ()
a) An Amplifier b)A Voltage Regulator c)A Coupler d)A Rectifier

Fill-in the blanks

1. The relation between α & β is _____.
2. The input impedance of MOSFET is _____ than the JFET.
3. The Zener diode is always operated in _____.
4. Write the Terminals of UJT _____.

Match the following:

9.

- | | | |
|--------------------|-----|----------------------------|
| i. Zener Diode | () | a) Variable Capacitor |
| ii. Varactor Diode | () | b) Optical Source |
| iii. UJT | () | c) Voltage Regulator |
| iv. LED | () | d) Uni Junction Transistor |



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Set-II

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Telangana – 501510

I B.Tech II SEM II-Mid Examinations, August-2023
Subject Name: **Electronic Devices & Circuits**

ANSWER KEY

Descriptive paper key link:

https://drive.google.com/file/d/11Lc629186jc41FqvyahUxei6WBUgnLb-/view?usp=drive_link

Objective Key Paper

Multiple choices:

1. c
2. d
3. c
4. b

Fill in the blanks:

5. $\alpha = \beta / 1 + \beta$; $\beta = \alpha / 1 - \alpha$
6. More
7. Reverse Bias
8. Base1; Base2; Emitter

Match the following:

9.
 - i. c
 - ii. a
 - iii. d
 - iv. b

Mid-1 & Mid-2 student answer scripts :

<https://drive.google.com/file/d/1VGNtkfLeJPG6h-6eTffX7XdHp0TbmxxQ/view?usp=sharing>

<https://drive.google.com/file/d/1SoNpRtP3wR0G6XprUWgmyUuj31W8ngWj/view?usp=sharing>



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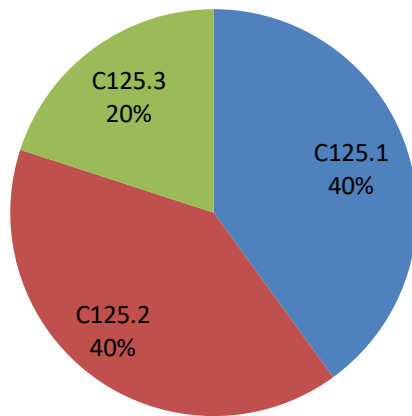
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ASSIGNMENT QUESTIONS (MID-I)

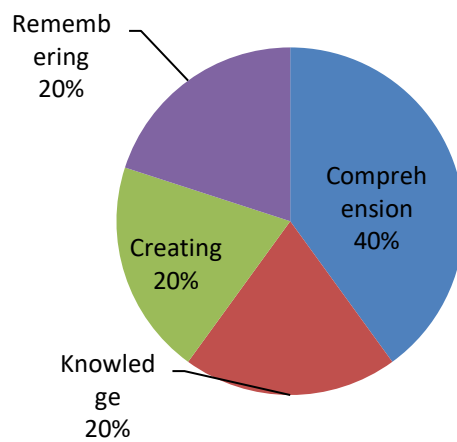
ELECTRONIC DEVICES AND CIRCUITS (SEM-II)

- 1 Explain the working of P-N Junction under forward bias & Reverse bias? (C125.1) (Comprehension)
- 2 Define static & dynamic resistances? Derive the expression for dynamic resistance? (C125.1) (Knowledge)
- 3 What is meant by diffusion & Transition Capacitances? Derive the expression for diffusion capacitance? (C125.1) (Remembering)
- 4 Discuss equivalent circuit of Diode? (C125.1) (Creating)
- 5 Draw a circuit diagram of a Bridge full wave rectifier. Explain its working and draw the input and output waveforms? (C125.2) (Knowledge)
- 6 Derive the Efficiency of half-Wave rectifier? (C125.2) (Remembering)
- 7 Discuss any two unbiased clippers with waveforms? (C125.2) (Creating)
- 8 Explain the operation of Capacitor-Filter with neat diagrams? (C125.2) (Comprehension)
- 9 Explain the construction and operation of NPN Transistor? (C125.3) (Comprehension)
- 10 Explain the input and output characteristics of Transistor in CE configuration. (C125.3) (Comprehension)

Assignment Questions mapping with CO's



Assignment Questions mapping with BT



MID-1 Assignment link :

https://drive.google.com/file/d/19oSjd1WHTsA3lc_zFOS3hRiuT4OtnIvq/view?usp=sharing



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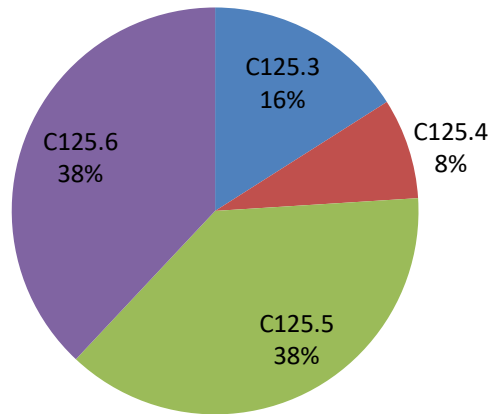
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ASSIGNMENT QUESTIONS (MID-II)

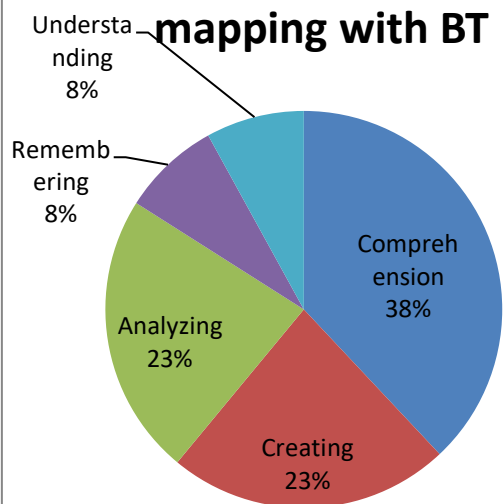
ELECTRONIC DEVICES AND CIRCUITS (SEM-II)

- | | | | |
|----|---|----------|------------------|
| 1 | Compare CB, CE, CC configurations? | (C125.4) | (Analyzing) |
| 2 | Explain how the transistor acts as a switch ? | (C125.3) | (Comprehension) |
| 3 | Discuss Switching times of a Transistor? | (C125.3) | (Creating) |
| 4 | Distinguish Between BJT & JFET? | (C125.5) | (Analyzing) |
| 5 | Explain the Construction & Working of N-Channel JFET? | (C125.5) | (Comprehension) |
| 6 | Discuss the V-I characteristics of JFET? | (C125.5) | (Creating) |
| 7 | Compare JFET & MOSFET? | (C125.5) | (Analyzing) |
| 8 | Explain how the MOSFET acts as a Capacitor ? | (C125.5) | (Comprehension) |
| 9 | Explain the Working & V-I Characteristics of Zener Diode? | (C125.6) | (Comprehension) |
| 10 | Explain the Construction & Working of Varactor Diode? | (C125.6) | (Comprehension) |
| 11 | Discuss the working conditions of Tunnel Diode? | (C125.6) | (Creating) |
| 12 | Define UJT ? Explain the operation of UJT? | (C125.6) | (Remembering) |
| 13 | Demonstrate the construction & Working of Photo Diode? | (C125.6) | (Understanding) |

Assignment Questions mapping with CO's



Assignment Questions mapping with BT



MID -2 Assignment

<https://drive.google.com/file/d/1pF2UtsFJa45Bj3lfKnxyPcxPcyfTWGt1/view?usp=sharing>



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SCHEME OF EVALUATION FOR MID 1

S.NO.	DESCRIPTION	MARKS	BLOOMS TAXONOMY	CO
1	Working Principle of PN Junction	3	(Evaluating)	(C125.1)
	PN Junction Forward bias, Reverse bias connection diagrams	2		
2	Definition for Static ,dynamic resistances	2	(Remembering)	(C125.1)
	Derivation for Static ,dynamic resistances	3		
3	Explanation for Equivalent circuit	2	(Applying)	(C125.1)
	Diagrams for Equivalent circuit	3		
4	Bridge full wave rectifier circuit diagram, waveforms	2.5	(Creating)	(C125.2)
	Bridge full wave rectifier working principle	2.5		
5	Definition, Working of Clippers	2.5	(Remembering)	(C125.2)
	circuit diagram, waveforms of clippers	2.5		
6	NPN Transistor Construction	2	(Creating)	(C125.3)
	NPN Transistor Working	3		

SCHEME OF EVALUATION FOR MID2

S.NO.	DESCRIPTION	MARKS	BLOOMS TAXONOMY	CO
1	For circuit diagram OF transistor	3	(Understanding)	(C125.3)
	Derivation Part	2		
2	Explanation for BJT	2.5	(Analyzing)	(C125.5)
	Explanation for JFET	2.5		
3	JFET V-I characteristics waveform, Circuit diagram of JFET	3	(Creating)	(C125.5)
	Explanation of JFET	2		
4	Explanation for MOSFET	2.5	(Analyzing)	(C125.5)
	Explanation for JFET	2.5		
5	Circuit diagram, symbol of UJT	2.5	(Remembering)	(C125.6)
	Operation of UJT	2.5		
6	Photo diode symbol, Construction	2	(Understanding)	(C125.6)
	Working Principle	3		



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Result Analysis:

CSE(AI&ML)

Course Title	ELECTRONIC DEVICES & CIRCUITS
Course Code	EC201ES
Programme	B.Tech
Year & Semester	Ist year 2 nd semester
Regulation	R22
Course Faculty	Mrs. D. ARUNA KUMARI, Assistant Professor , ECE

Weak Students:

S No	Roll no	No of backlogs	Internal-I Status (35Marks)	Internal-II Status (40Marks)
1	22X31A6605	2	22	21
2	22X31A6606	2	22	28
3	22X31A6610	3	17	21
4	22X31A6619	2	18	24
5	22X31A6620	2	22	26
6	22X31A6637	2	24	25
7	22X31A6640	2	19	A
8	22X31A6641	2	17	22
9	22X31A6644	2	15	19

Advanced learners:

S No	Roll No	Type of support provided
1	22X31A6601	Advanced concepts materials is provided for advanced learners, Subject seminars are presented by advanced learners in the class, advanced learners are encouraged to support slow learners.
2	22X31A6602	
3	22X31A6607	
4	22X31A6608	
5	22X31A6609	
6	22X31A6616	
7	22X31A6622	
8	22X31A6626	
9	22X31A6627	
10	22X31A6631	
11	22X31A6636	
12	22X31A6638	
13	22X31A6639	
14	22X31A6647	
15	22X31A6650	



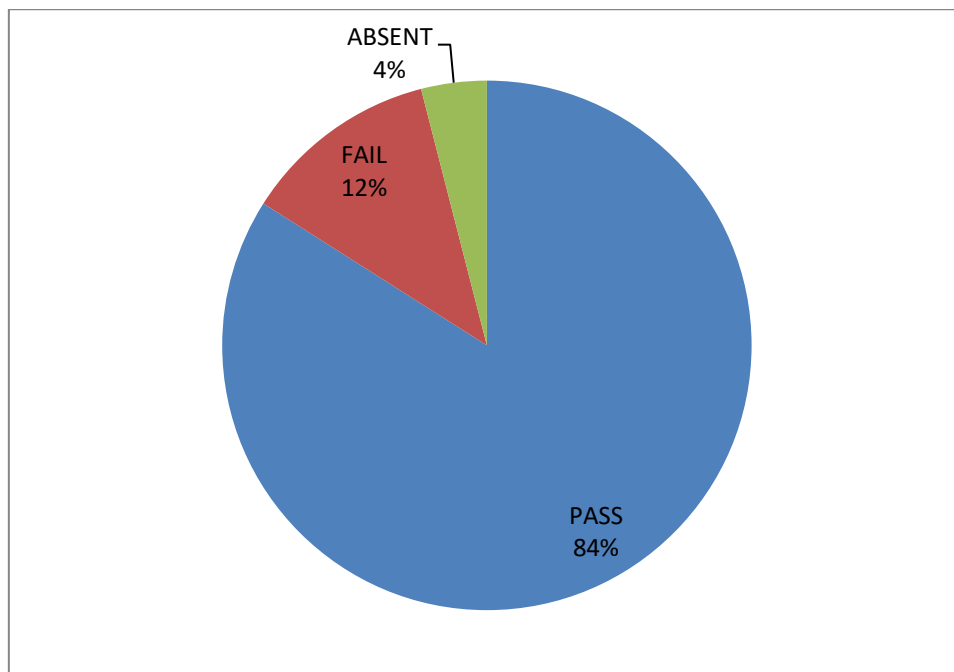
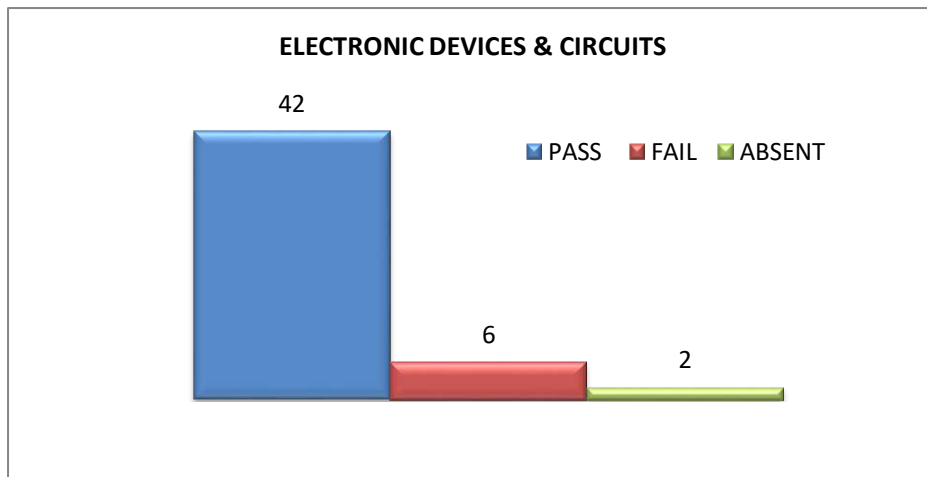
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Telangana – 501510

RESULT ANALYSIS AT THE END OF SEMISTER

Branch: CSE(AI&ML)

Subject: ELECTRONIC DEVICES & CIRCUITS





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Ibrahimpattam, Sheriguda(V), Ibrahimpattam(M), Ranga Reddy Dist., Telangana – 501510

DEPARTMENT OF HUMANITIES AND SCIENCE REMEDIAL CLASSES TIME TABLE

DAY/ PERIOD	MON 4.00-5.00	TUE 4.00-5.00	WED 4.00-5.00	THUR 4.00-5.00	FRI 4.00-5.00	SAT 4.00-5.00
CSE-A	ODE&VC	ENG	EDC	AP	ODE&VC	AP
CSE-B	AP	EDC	ODE&VC	ENG	EDC	ENG
CSE-C	ENG	AP	EDC	ODE&VC	AP	ODE&VC

DAY/ PERIOD	MON 4.00-5.00	TUE 4.00-5.00	WED 4.00-5.00	THUR 4.00-5.00	FRI 4.00-5.00	SAT 4.00-5.00
DS	EDC	AP	ODE&VC	ENG	EDC	ODE&VC
CYBER	ENG	EDC	AP	ODE&VC	AP	ENG

DAY/ PERIOD	MON 4.00-5.00	TUE 4.00-5.00	WED 4.00-5.00	THUR 4.00-5.00	FRI 4.00-5.00	SAT 4.00-5.00
AIML-A	ODE&VC	EC	EDC	BEE	EC	ODE&VC
AIML-B	BEE	EDC	ODE&VC	EC	BEE	EDC

DAY/ PERIOD	MON 4.00-5.00	TUE 4.00-5.00	WED 4.00-5.00	THUR 4.00-5.00	FRI 4.00-5.00	SAT 4.00-5.00
AI&DS	BEE	EC	ODE&VC	EDC	BEE	EC
IOT	EC	ODE&VC	EDC	BEE	ODE&VC	EDC

DAY/ PERIOD	MON 4.00-5.00	TUE 4.00-5.00	WED 4.00-5.00	THUR 4.00-5.00	FRI 4.00-5.00	SAT 4.00-5.00
ECE	ODE&VC	BEE	EC	EDC	BEE	EC
CIVIL	ODE&VC	BEE	EC	AM	BEE	EC


Head of the Department
Department of H&S
SRI INDU INSTITUTE OF ENGG & TECH
Sheriguda(V) Ibrahimpattam (M) R.R. Dist-501 510


PRINCIPAL
Sri Indu Institute of Engineering & Techno.
Sheriguda(VIII), Ibrahimpattam
R.R. Dist. Telangana-501 510.

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY



Department of Humanities & Sciences

Course Outcome Attainment (Internal Examination-1)

Name of the faculty: D.ARUNA KUMARI

Academic Year: 2022-2023

Branch & Section: AI&ML-A

Examination: I Internal

Course Name: EDC

Year I

Semr II

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Q5a	Q5b	Q6a	Q6b	Obj1	A1
Max. Marks ==>		5		5		5		5		5		5		10	5
1	22X31A6601	4.5		5		5		4.5						9	5
2	22X31A6602	5		5		5		5						10	5
3	22X31A6603	4		3						2		2		10	5
4	22X31A6604	4		2		5				2				9	5
5	22X31A6605	2		4						2				9	5
6	22X31A6606	3		1		2		2						9	5
7	22X31A6607	4.5		4		4.5				4				9	5
8	22X31A6608			5				5		5		5		9	5
9	22X31A6609	5		5				5				4		9	5
10	22X31A6610	0		1				1		1				9	5
11	22X31A6611														
12	22X31A6612	3		2						2		1		7	5
13	22X31A6613	4		3				3				2		8	5
14	22X31A6614	5		5				5		5				8	5
15	22X31A6615	4.5				3						3.5		9	5
16	22X31A6616	3.5		2		4.5						3		9	5
17	22X31A6617	5		2				3				3		9	5
18	22X31A6618	5		5				5				5		9	5
19	22X31A6619	2		2				0.5						9	5
20	22X31A6620	2		2		1.5				1.5				10	5
21	22X31A6621	1.5		1.5										9	5
22	22X31A6622			5		5		5				5		9	5
23	22X31A6623	3.5		2.5				1				1		9	5
24	22X31A6624	2		3.5				2				2.5		9	5
25	22X31A6625	2.5						1.5				1		10	5
26	22X31A6626	5		5				5		5				10	5
27	22X31A6627	5		5		5		5						10	5
28	22X31A6628	2.5		2						5		2.5		9	5
29	22X31A6629	2		2						1				10	5
30	22X31A6630	4		5		4		4						10	5
31	22X31A6631	5		5				5				5		10	5
32	22X31A6632	1.5								2		1.5		10	5
33	22X31A6633	2				3				1				10	5
34	22X31A6634	1		5				5				5		10	5
35	22X31A6635	2		2				2.5				1.5		10	5
36	22X31A6636	3.5						3.5		2.5		2.5		7	5
37	22X31A6637	4		2		1		3						9	5
38	22X31A6638	5		4.5						5		4.5		9	5
39	22X31A6639	5				4.5		4.5		5				7	5
40	22X31A6640	3		2								1		8	5
41	22X31A6641	1.5				1.5						1		8	5
42	22X31A6642	4		5				3.5				3.5		8	5
43	22X31A6643	4				5		5						8	5

44	22X31A6644	1.5							1.5				7	5	
45	22X31A6645	3		5				4				2	7	5	
46	22X31A6646	4		4.5					3		2.5		8	5	
47	22X31A6647	5		5					4		5		8	5	
48	22X31A6648	5		4		3		2					8	5	
49	22X31A6649	4		5		4		4					8	5	
50	22X31A6650	4		4		5		4					10	5	
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of students performed above the target		32	0	25	0	15	0	22	0	9	0	12	0	49	49
Number of students attempted		47	0	40	0	19	0	30	0	20	0	26	0	49	49
Percentage of students scored		68%		63%		79%		73%		45%		46%		100%	100%

CO Mapping with Exam Questions:

CO - 1	Y		Y										Y	Y	
CO - 2					Y		Y					Y		Y	Y
CO - 3										Y				Y	Y
CO - 4															
CO - 5															
CO - 6															

% Students Scored	68%		63%		79%		73%		45%		46%		100%	100%
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CO Attainment based on Exam Questions:

CO - 1	68%		63%										100%	100%	
CO - 2					79%		73%					46%		100%	100%
CO - 3									45%					100%	100%
CO - 4															
CO - 5															
CO - 6															

CO	Subj	obj	Asgn	Overall	Level
CO-1	65%	81%	100%	82%	3.00
CO-2	66%	75%	100%	80%	3.00
CO-3	45%	73%	100%	73%	3.00
CO-4					
CO-5					
CO-6					

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal 1 Exam) **3.00**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY



Department of Humanities & Sciences

Course Outcome Attainment (Internal Examination-2)

Name of the faculty: [D.ARUNA KUMARI](#)

Academic Year:

[2022-2023](#)

Branch & Section: [AI&ML-A](#)

Examination:

[II Internal](#)

Course Name: [EDC](#)

Year [I](#)

[Semester:](#)

[II](#)

S.No	HT No.	Q1a	Q1b	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Q5a	Q5b	Q6a	Q6b	Obj	A2	viva/ ppt
Max. Marks ==>		5		5		5		5		5		5		10	5	5
1	22X31A6601			5		4		5				4		10	4	5
2	22X31A6602	5		5				5				5		10	5	5
3	22X31A6603	3		4				5				5		10	5	5
4	22X31A6604			3		3		5				5		10	4	5
5	22X31A6605			1				2						10	3	5
6	22X31A6606	2		2		1		4						10	4	5
7	22X31A6607	5		5				4				4		10	5	5
8	22X31A6608	4		5		4						4		10	5	5
9	22X31A6609	3		3		5		5						10	5	5
10	22X31A6610	1		1				2						10	3	5
11	22X31A6611															
12	22X31A6612	4		5				4				4		10	5	5
13	22X31A6613	4		3		3		3						10	4	5
14	22X31A6614	4		4				5				2		10	5	5
15	22X31A6615			3		2		5				3		10	3	5
16	22X31A6616	5				5		5				4		10	5	5
17	22X31A6617	4		5		3		4						10	5	5
18	22X31A6618	5		5		4		5						8	5	5
19	22X31A6619	1		2		1		2						10	3	5
20	22X31A6620	1		2				2				2		10	4	5
21	22X31A6621			3				2				2		9	3	5
22	22X31A6622			4		4		5				5		10	5	5
23	22X31A6623	1		4		3		3						9	4	5
24	22X31A6624	1		4				3				1		10	5	5
25	22X31A6625			5		2		3				3		10	3	5
26	22X31A6626			5		5		5				5		10	5	5
27	22X31A6627	5				5		5				5		10	5	5
28	22X31A6628			4		4		4				3		9	5	5
29	22X31A6629	2		2				3						10	5	5
30	22X31A6630	2		5				5				4		10	5	5
31	22X31A6631			5		3		5				5		10	3	5
32	22X31A6632	3		3		2		3						9	5	5
33	22X31A6633	2		3				4				2		8	3	5
34	22X31A6634	4		2		1		3						9	5	5
35	22X31A6635	2		3				2						9	3	5
36	22X31A6636	4		3		3		2						10	4	5
37	22X31A6637			3		1		3						8	5	5
38	22X31A6638	5		4		3		5						9	5	5
39	22X31A6639	5		5				5				4		9	3	5
40	22X31A6640															
41	22X31A6641			2		1		2						8	4	5
42	22X31A6642	4		4				5				4		10	4	5
43	22X31A6643	2		2				4						10	5	5
44	22X31A6644			2		2		2						5	3	5
45	22X31A6645			1		3		2				2		10	4	5
46	22X31A6646	4				3		4				3		10	3	5
47	22X31A6647	5		5				5				4		10	5	5
48	22X31A6648	2		3				4				1		10	5	5
49	22X31A6649	2		4				4				4		10	3	5

50	22X31A6650	2		4				5				4		10	5	5
Target set by the faculty / HoD		3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00	3.00
Number of students performed above the target		20	0	34	0	18	0	37	0	0	0	22	0	47	48	48
Number of students attempted		34	0	45	0	27	0	47	0	0	0	29	0	48	48	48
Percentage of students scored more than target		59%		76%		67%		79%				76%		98%	100%	100%

CO Mapping with Exam Questions:

CO - 1																	Y	
CO - 2																		Y
CO - 3	Y													Y	Y	Y		
CO - 4				Y										Y	Y	Y		
CO - 5						Y			Y					Y	Y	Y		
CO - 6			Y									Y		Y	Y	Y		

% Students Scored >Target %		59%		76%		67%		79%				76%		98%	100%	100%
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CO Attainment based on Exam Questions:

CO - 1																	100%
CO - 2																	100%
CO - 3	59%													98%	100%	100%	
CO - 4				59%										98%	100%	100%	
CO - 5						59%								98%	100%	100%	
CO - 6			76%									76%		98%	100%	100%	

CO	Subj	obj	asgn	ppt	Overall	Level
CO-1				100%	100%	3.00
CO-2				100%	100%	3.00
CO-3	59%	98%	100%	100%	89%	3.00
CO-4	59%	98%	100%	100%	89%	3.00
CO-5	59%	98%	100%	100%	89%	3.00
CO-6	76%	98%	100%	100%	93%	3.00

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal Examination)- **3.00**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY



Department of Humanities & Sciences

Course Outcome Attainment (University Examinations)

Name of the faculty : [D.ARUNA KUMARI](#)

Academic Year: [2022-2023](#)

Branch & Section: [AI&ML-A](#)

Year / Semester: [I / II](#)

Course Name: [EDC](#)

S.No	Roll Number	Marks Secured
1	22X31A6601	41
2	22X31A6602	44
3	22X31A6603	32
4	22X31A6604	30
5	22X31A6605	18
6	22X31A6606	23
7	22X31A6607	44
8	22X31A6608	36
9	22X31A6609	36
10	22X31A6610	25
11	22X31A6611	
12	22X31A6612	29
13	22X31A6613	32
14	22X31A6614	36
15	22X31A6615	33
16	22X31A6616	41
17	22X31A6617	36
18	22X31A6618	36
19	22X31A6619	22
20	22X31A6620	24
21	22X31A6621	33
22	22X31A6622	43
23	22X31A6623	21
24	22X31A6624	31
25	22X31A6625	30
26	22X31A6626	44
27	22X31A6627	47
28	22X31A6628	31
29	22X31A6629	12
30	22X31A6630	19
31	22X31A6631	45
32	22X31A6632	32
33	22X31A6633	24
34	22X31A6634	26
35	22X31A6635	23

S.No	Roll Number	Marks Secured
36	22X31A6636	35
37	22X31A6637	23
38	22X31A6638	37
39	22X31A6639	44
40	22X31A6640	
41	22X31A6641	6
42	22X31A6642	21
43	22X31A6643	12
44	22X31A6644	14
45	22X31A6645	31
46	22X31A6646	31
47	22X31A6647	42
48	22X31A6648	28
49	22X31A6649	28
50	22X31A6650	36
51		
52		
53		
54		
55		
56		
57		
58		
59		
60		
61		
62		
63		
64		
65		
66		
67		
68		
69		
70		

Max Marks	60
Class Average mark	31
Number of students performed above the target	27
Number of successful students	48
Percentage of students scored more than target	56%
Attainment level	3

Attainment Level	% students
1	40%
2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Humanities & Sciences

Course Outcome Attainment



Faculty: [D.ARUNA KUMARI](#)

Academic Year: [2022-2023](#)

Branch & Section: [AI&ML-A](#)

Examination: [Internal](#)

Course Name: [EDC](#)

Year: [I](#)

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00	3.00	3.00	3.00	3.00
CO2	3.00	3.00	3.00	3.00	3.00
CO3	3.00	3.00	3.00	3.00	3.00
CO4		3.00	3.00	3.00	3.00
CO5		3.00	3.00	3.00	3.00
CO6		3.00	3.00	3.00	3.00
Internal & University Attainment:			3.00	3.00	
Weightage			25%	75%	
CO Attainment for the course (Internal, University)			0.75	2.25	
CO Attainment for the course (Direct Method)			3.00		

Overall course attainment level

3.00



SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Humanities & Sciences

Program Outcome Attainment (from Course)

Name of Faculty: [D.ARUNA KUMARI](#)

Academic Year: [2022-2023](#)

Branch & Section: [AI&ML-A](#)

Year: [I](#)

Course Name: [EDC](#)

Semester: [II](#)

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	3	-	-	-	-	-	2	3	3	3
CO2	-	1	3	-	-	-	1	-	-	-	2	2	3	3
CO3	1	3	-	-	2	1	-	-	-	-	2	-	3	3
CO4	2	-	2	2	-	-	-	-	-	-	2	3	3	3
CO5	2	3	3	-	3	-	-	1	-	-	2	2	3	3
CO6	3	3	-	-	3	-	-	-	1	1	2	3	3	3
Course	2.2	2.4	2.67	2	2.75	1	1	1	1	1	2	2.6	3	3

CO	Course Outcome Attainment													
	3.00													
CO1	3.00													
CO2	3.00													
CO3	3.00													
CO4	3.00													
CO5	3.00													
CO6	3.00													
Overall course attainment level	3.00													

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainment	2.20	2.40	2.67	2.00	2.75	1.00	1.00	1.00	1.00	1.00	2.00	2.60	3.00	3.00

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)



SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY
(UGC AUTONOMOUS INSTITUTION)

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(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad) Khalsa
Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana – 501510

ATTENDANCE REGISTER

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