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EAMCET CODE: INDI Approved by AICTE, New Delhi, & Affiliated to JNTUH, Hyderabad.

**JNTUH CODE: X3** 

# **COURSE FILE**

ON

# **ELECTRONIC DEVICES & CIRCUITS**

**Course Code – EC201ES** 

I-B. Tech Semester-II

A.Y. 2022-2023

Prepared by

Mrs. P.SUMANA

**Asst. Professor** 

Head of the Department Department of H&S SRI INDU INSTITUTE OF ENGG & TECH beriouda(^/\_ lbrahimostnam (M) R.R. Dist-501 516

PRINCIPAL

Sri Indu Institute of Engineering & Tech Sheriguda(Vill), Ibrahimpatnam R.R. Dist. Telangana-501 510.



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#### **INSTITUTE VISION & MISSION**

#### Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

#### Mission:

- > IM1: To offer outcome-based education and enhancement of technical and practical skills.
- IM2: To Continuous assess of teaching-learning process through institute-industry collaboration.
- IM3: To be a center of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students' fraternity.
- IM4: To Create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders.

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#### PROGRAM OUTCOMES

**PO1:** ENGINEERING KNOWLEDGE: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

**PO2: PROBLEM ANALYSIS**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

**PO3**: **DESIGN/DEVELOPMENT OF SOLUTIONS**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

**PO4**: **CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

**PO5**: **MODERN TOOL USAGE**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

**PO6**: **THE ENGINEER AND SOCIETY**: Apply reasoning informed by the contextual knowledge to associate, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

**PO7**: **ENVIRONMENT AND SUSTAINABILITY**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

**PO8**: **ETHICS**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

**PO9: INDIVIDUAL AND TEAM WORK**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

**PO10**: **COMMUNICATION**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, give and receive clear instructions.

**PO11: PROJECT MANAGEMENT AND FINANCE**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

**PO12**: **LIFE-LONG LEARNING**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

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#### SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY B.Tech. in COMPUTER SCIENCE AND ENGINEERING (Data Science) COURSE STRUCTURE, I YEAR SYLLABUS (BR22 Regulations) Applicable from Academic Year: 2022-23 Batch

#### I Year I Semester

S. No.	Course Code	Course Title	L	Т	Р	Credits
1.	MA101BS	Matrices and Calculus	3	1	0	4
2.	CH103BS	Engineering Chemistry	3	1	0	4
3.	CS103ES	Programming for Problem Solving	3	0	0	3
4.	EE101ES	Basic Electrical Engineering	2	0	0	2
5.	ME101ES	Computer Aided Engineering Graphics	1	0	4	3
6.	CS106ES	Elements of Computer Science & Engineering	0	0	2	1
7.	CH106BS	Engineering Chemistry Laboratory	0	0	2	1
8.	CS107ES	Programming for Problem Solving Laboratory	0	0	2	1
9.	EE102ES	Basic Electrical Engineering Laboratory	0	0	2	1
		Induction Program				
		Total	12	2	12	20

#### I Year II Semester

S. No.	Course Code	Course	L	Т	Р	Credits
1.	MA201BS	Ordinary Differential Equations and Vector Calculus	3	1	0	4
2.	AP202BS	Applied Physics	3	1	0	4
3.	ME202ES	Engineering Workshop	0	1	3	2.5
4.	EN204HS	English for Skill Enhancement	2	0	0	2
<mark>5.</mark>	EC201ES	<b>Electronic Devices and Circuits</b>	<mark>2</mark>	<mark>0</mark>	<mark>0</mark>	<mark>2</mark>
6.	AP205BS	Applied Physics Laboratory	0	0	3	1.5
7.	CS201ES	Python Programming Laboratory	0	1	2	2
8.	EN207HS	English Language and Communication Skills Laboratory	0	0	2	1
9.	CS203ES	IT Workshop	0	0	2	1
10.	*MC201ES	Environmental Science	3	0	0	0
		Total	13	4	12	20

#### ELECTRONIC DEVICES AND CIRCUITS B.Tech. I Year II Sem.

#### **Course Objectives:**

1. To introduce components such as diodes, BJTs and FETs.

2. To know the applications of devices.

3. To know the switching characteristics of devices.

Course Outcomes: Upon completion of the Course, the students will be able to:

1. Acquire the knowledge of various electronic devices and their use on real life.

2. Know the applications of various devices.

3. Acquire the knowledge about the role of special purpose devices and their applications.

#### UNIT - I

**Diodes:** Diode - Static and Dynamic resistances, Equivalent circuit, Diffusion and Transition Capacitances, V-I Characteristics, Diode as a switch- switching times.

#### UNIT - II

**Diode Applications:** Rectifier - Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Rectifiers with Capacitive and Inductive Filters, Clippers-Clipping at two independent levels, Clamper-Clamping Circuit Theorem, Clamping Operation, Types of Clampers.

#### UNIT - III

**Bipolar Junction Transistor (BJT):** Principle of Operation, Common Emitter, Common Base and Common Collector Configurations, Transistor as a switch, switching times,

#### UNIT - IV

**Junction Field Effect Transistor (FET):** Construction, Principle of Operation, Pinch-Off Voltage, Volt-Ampere Characteristic, Comparison of BJT and FET, FET as Voltage Variable Resistor, MOSFET, MOSTET as a capacitor.

#### UNIT - V

**Special Purpose Devices:** Zener Diode - Characteristics, Zener diode as Voltage Regulator, Principle of Operation - SCR, Tunnel diode, UJT, Varactor Diode, Photo diode, Solar cell, LED, Schottky diode.

#### **TEXT BOOKS:**

1. Jacob Millman - Electronic Devices and Circuits, McGraw Hill Education

2. Robert L. Boylestead, Louis Nashelsky- Electronic Devices and Circuits theory, 11th Edition,2009, Pearson.

#### **REFERENCE BOOKS:**

1. Horowitz -Electronic Devices and Circuits, David A. Bell – 5thEdition, Oxford.

2. Chinmoy Saha, Arindam Halder, Debaati Ganguly - Basic Electronics-Principles and Applications, Cambridge, 2018.



Course: Electronic Devices and Circuits
<u>Course Outcomes</u>

Class: I- B TECH- CSE(DATA SCIENCE)

After completing this course the student will be able to:

C125.1: Acquire the knowledge of diode with the help of V-I characteristics. (Understand)

C125.2: Analyze the applications of diode. (Analyze)

C125.3: Understand the principle of operation of BJT. (Understand)

C125.4: Know the characteristics of BJT under various biasing conditions. (Applying)

C125.5: Interpret the construction, operation and characteristics of FET. (Understand)

C125.6: Analyze the performance of special purpose devices and their applications. (Analyze)

#### Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO / CO	PO 1	PO2	PO3	PO4	PO5	P O 6	PO 7	PO 8	PO 9	PO 10	PO1 1	PO12	PSO1	PSO2
C125.1	3	2	-	-	3	-	-	-	-	-	2	3	3	3
C125.2	-	1	3	-	-	-	1	-	-	-	2	2	3	3
C125.3	1	3	-	-	2	1	-	-	-	-	2	-	3	3
C125.4	2	-	2	2	-	-	-	-	-	-	2	3	3	3
C125.5	2	3	3	-	3	-	-	1	-	-	2	2	3	3
C125.6	3	3	-	-	3	-	-	-	1	1	2	3	3	3
C125	2.20	2.40	2.67	2.00	2.75	1	1	1	1	1	2.00	2.60	3.00	3.00



#### **CO-PO mapping Justification**

C125.1: Acquire the knowledge of diode with the help of V-I characteristics. (Understand)

	Justification
PO1	Applying basic knowledge on Electronic Devices And Circuits students can solve basic circuit problems.
PO2	Engineering problems often involve the proper utilization of diodes in electronic circuits. Identifying issues related to diode behavior is crucial for effective problem-solving.
PO5	Acquiring knowledge of diode V-I characteristics through the use of modern simulation tools aligns with PO Modern Tool Usage. The integration of simulation software enables engineers to create, select, and apply appropriate techniques for predicting and modeling diode behavior.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Students can continuously learning to explore more knowledge in semiconductor devices.
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

C125.2: Analyze the applications of diode. (Analyze)

	Justification
PO2	Students can analyze the rectifier, clippers, clamper Circuits using loop equations.
PO3	Students can design the different transistor configuration circuits.
PO7	Engineers focusing on sustainable development can leverage diodes and their applications to design energy-efficient systems, develop renewable energy technologies, and create environmentally friendly products.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12	Students can continuously learning to explore more knowledge in semiconductor devices.
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

# C125.3: Understand the principle of operation of BJT. (Understand)

	Justification
PO1	Understanding the principle of operation of a BJT involves the application of mathematics, science, engineering fundamentals, and specialization in electronics.
PO2	Understanding the principle of operation of a BJT is crucial for problem analysis in electronic engineering. By identifying, formulating, and analyzing complex engineering problems related to BJT behavior, engineers can reach substantiated conclusions.
PO5	Applying simulation tools to visualize and analyze BJT characteristics, including V-I curves.
PO6	Engineers applying BJTs or any technology must assess the broader societal, health, safety, legal, and cultural impacts of their work.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

C125.4: Know the characteristics of BJT under various biasing conditions. (Applying)

	Justification
PO1	Engineers must apply mathematical models, semiconductor physics, and circuit theory to solve complex engineering problems related to BJT biasing and amplifier design.
PO3	The characteristics of BJTs under various biasing conditions play a crucial role in the design and development of engineering solutions. Engineers need to consider these characteristics to design system components or processes that meet specified needs, taking into account public health and safety, as well as cultural, societal, and environmental considerations.
PO4	Engineers, through research-based knowledge, can conduct experiments, analyze data, and synthesize information to draw valid conclusions about BJT behavior.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.

	PO12	Students can continuously learning to explore more knowledge in semiconductor devices.
	PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
Ī	PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

C125.5: Interpret the construction, operation and characteristics of FET. (Understand)

	Justification
PO1	The knowledge of FET principles serves as a foundation for solving complex engineering problems related to electronic circuits and systems.
PO2	Recognizing challenges in electronic circuit design and signal processing that involve FET behavior.
PO3	Students, equipped with this knowledge, can design solutions for complex engineering problems, create system components using FETs, and consider health, safety, environmental, cultural, and societal factors in their designs.
PO5	Students can apply small signal model techniques in the design of FET amplifiers.
PO8	By understanding the construction, operation, and characteristics of FETs, engineers can responsibly and ethically apply this technology.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Students can continuously learning to explore more knowledge in semiconductor devices.
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

C125.6: Analyze the performance of special purpose devices and their applications. (Analyze)

	Justification
PO1	Students get the knowledge on special purpose devices like Zener, Tunnel, varactor diode,
	UJT, SCR to simplify the complex circuits for analysis.
PO2	Stude Students can design the special purpose devices like Zener, Tunnel, varactor diode,
	UJT, SCR .
PO5	Students can apply transistor hybrid model techniques in the design of BJT amplifiers.
PO9	Individuals equipped with expertise in the performance of these devices can effectively tackle
	complex problems or challenges that require the utilization of such technology. They can provide

	innovative solutions by leveraging their understanding of device capabilities.
PO10	Understanding device performance allows engineers to provide clear and precise instructions for integrating these devices into larger systems or for their specific applications.
PO11	Students can get demonstrate knowledge and understanding of the electronic devices and circuits and apply these to one's own project, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Understanding the performance of special purpose devices places learning within the broader context of technological change.
PSO1	Students are able to explore the design of electronic devices in the areas of VLSI design and embedded systems.
PSO2	Students can solve the design problems of electronic devices using Keil and Xilinx.

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

UGC Autonomous Institution, Accredited by NAAC with A+ Grade

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Lr. No. SIIET/BR22/Academic Calendar/2022/02

Date: 15.12.2022

# **REVISED ACADEMIC CALENDAR** I B.TECH FOR THE ACADEMIC YEAR 2022-23 (BR22-REGULATIONS)

Dr. I. Satyanarayana, Principal.

To,

All the HOD's Sir,

Sub: SIIET (Autonomous)-Academic & Evaluation-Revised Academic Calendar for I B.Tech - I & II Semesters for the academic year 2022-2023-Reg.

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The approved Academic Calendar for I B.Tech - I & II Semesters for the academic year 2022-23 is given below. I-SEMESTER

	D 14	Per	Duration	
S. NO	Description	From	To	Duration
1.	Commencement of I Semester class work (including Induction programme)		03.11.2022	
2.	1 <sup>st</sup> Spell of Instructions	03.11.2022	28.12.2022	8 Weeks
3.	I Mid Examinations	`29.12.2022	04.01.2023	1 Week
4.	Submission of First Mid Term Exam Marks to the Autonomous Section on or before	10.01.2023		
5.	2 <sup>nd</sup> Spell of Instructions	05.01.2023	02.03.2023	8 Weeks
6.	Second Mid Term Examinations	03.03.2023	09.03.2023	1 Week
7.	Preparation & Practical Examinations	10.03.2023 16.03.2023		1 Week
8.	Submission of Second Mid Term Exam Marks to the Autonomous Section on or before	16.03.2023		
9.	I Semester End Examinations	17.03.2023	01.04.2023	2 Weeks

#### **II-SEMESTER**

~ ~~~		Per	Duration	
S. NO	Description	From	To	Duration
1.	Commencement of II Semester class work		03.04.2023	
2.	1 <sup>st</sup> Spell of Instructions (including Summer Vacation)	03.04.2023	10.06.2023	10 Weeks
200	Summer Vacation	15.05.2023	27.05.2023	2 Weeks
3.	I Mid Examinations	`12.06.2023	17.06.2023	1 Week
4.	Submission of First Mid Term Exam Marks to the Autonomous Section on or before	23.06.2023		
5.	2 <sup>nd</sup> Spell of Instructions	19.06.2023	12.08.2023	8 Weeks
6.	II Mid Term Examinations	14.08.2023	19.08.2023	1 Week
7.	Preparation & Practical Examinations	21.08.2023	26.08.2023	1 Week
8.	Submission of Second Mid Term Exam Marks to the Autonomous Section on or before	26.08.2023		
9.	II Semester End Examinations	28.08.2023	09.09.2023	2 Weeks

**OF EXAMINATIONS** Indu Institute of Engineering and Technology An Autonomous Institution Under Inflete Depts. & AO: Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510.

Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510.

String Indu Institute of Engineering and Technology (An Autonomous Institution under JNTUH)

**PRINCIPAL** 

Sri Indu Institute of the needed by the Technology (An Autonomous Institution Under JNTUH) Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510.





# SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC)

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KhalsaIbrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana – 501 510 https://siiet.ac.in/

Class: DATA SCIENCE	Semester: II	W.E.F-03-04-2023	

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	I 9:40- 10:30	II 10:30 - 11:20	III 11:20- 12:10	12:10- 12.45	IV 12.45- 1.35	V 1.35- 2.25	VI 2.25- 3.15	VII 3.15-4.00
MON		PYTHON LAP	3		AP	ODE	EDC	LIBRARY
TUE	10	ITWS/EWS LA	В		AP	EDC	ENG	ODE(T) /AP(T)
WED	ODE	AP	ES	N C	ITWS/EWS LAB		PYTHON LAB(T)/ EWS(T)	
THU	ODE	ENG	EDC	н	ODE	EDC	AP	AP(T)/ODE(T)
FRI	AP	ENG	EDC		AP/ELCS LAB		EWS(T)/ PYTHONLAB(T	
SAT	ENG	ODE	ES		AP/ELCS LAB			ES

Course Code	Course Name	Name of the Faculty	Course Code	Course Name	Name of the Faculty
MA201BS	ODE-Ordinary Differential Equations & Vector Calculus	CH.SARITHA	AP205BS	APLAB-Applied Phyics Laboratory	B.SANTHI/M.MAN ISHA/M.JANAIAH /P.SRINIVASACH ARY
AP202BS	AP-Applied Physics	Dr.B.NAGALAKSHMI	CS201ES	Python Programming Laboratory	P.BALU/M.TEJAS WI
EN204HS	ENG- English for Skill Enhancement	S.SWAPNA	EN207HS	ELCS LAB-English Language and Communication Skills Laboratory	E.PRARTHANA/S. SWAPNA
EC201ES	EDC-Electronics Devices and Circuits	P.SUMANA	CS203ES	ITWS-IT Workshop	B.RAJITHA/N.KEE RTHI CHANDANA
ME202ES	EWS-Engineering Workshop	W.MARUTHI/B.SRIN U NAIK	MC201ES	ES-Environmental Science	G.VIJAY

**Class In-Charge** 

Time Table Coordinator

510

LH: D-208

Head of The Department

Sri Indu Institute of Engg. & Tech Main Road, Sheriguda(V) Ibrahimpatnam(M), R.R. Dist. Telangana-501 510



S.N	Unit	TOPIC	Numbe	Teaching	REFERENCE
0			r of Sessions Planned	method/Aids	
1.		Introduction to diode	1	Black Board	R1,T1,PPT
2.		Static resistance and dynamic resistances	1	Black Board	R1,T1
3.		Diode Equivalent circuits	1	Black Board	R1,T1
4.	1	Diffusion Transition and Capacitances	1	Black Board	R1,T1
5.		Volt Ampere Characteristic of a diode	1	Black Board	R1,T1,PPT
6.		Diode as a switch	1	Black Board	R1,T1,PPT
7.		Diode switching times	1	Black Board	R1,T1
8.		Revision	1	Black Board	R1,T1,T2
9.		Half wave Rectifier	1	Black Board	R2,T1,T2
10		Full Wave Rectifier	1	Black Board	R1,T1,T2
11	2	Bridge Rectifier	1	Black Board	R2,T1
12		Inductor Filters, Capacitor filters	1	Black Board	R2,T1,T2
13		Clipper-clipping at two independent levels	1	Black Board	T2
14		Clamping circuit theorem	1	Black Board	T2
15		Clamping operation	1	Black Board	T2
16		Types of clampers	1	Black Board	T2

#### LESSON PLAN

17		Problems on half wave and Full wave Rectifier	1	Black Board	T2,T1
18		Principle of Operation of BJT	1	Black Board, PPT	T2,PPT
19		Common emitter Configuration	1	Black Board	Т2,Т1,РРТ
20		Efficiency calculation in CE	1	Black Board	T2,W1
21		Common base	1	Black Board	T2,PPT
	3	configuration			
22	3	Efficiency calculation in CB	1	Black Board	T2,PPT
23		Common collector configuration	1	Black Board	T2,T1,W1,PPT
24		Efficiency calculation in CC	1	Black Board	T2,PPT
25		Transistor as switch		Black Board	T1
26		Transistor switching times		Black Board	T1
27		Junction Field Effect Transistor (FET) Construction	1	Black Board	T1,T2,W2
28		Principle of Operation of FET	1	Black Board	T1,T2,W2
29		Pinch-Off Voltage,	1	Black Board	T1,T2
30		Volt-Ampere Characteristic	1	Black Board	T1,T2,W2
31	4	Comparison of BJT and FET	1	Black Board	T1,T2,W2
32		FET as Voltage Variable Resistor	1	Black Board	T1,T2,W2
33		MOSFET introduction	1	Black Board	T1
34		Depletion mode MOSTET as a capacitor	1	Black Board	T1
35		Enhancement mode	1	Black Board	T1,T2
36		MOSTET as a capacitor	1	Black Board	T1
37		Special Purpose Devices introduction	1	Black Board	T1,T2,W3
38		Zener Diode - Characteristics	1	Black Board	T1

39		Zener diode as Voltage Regulator	1	Black Board	T1,T2
	5				
40		Principle of Operation - SCR	1	Black Board	T1
41		Tunnel diode	1	Black Board	T1
42		UJT	1	Black Board	T1,T2
43		Varactor Diode	1	Black Board	T1
44		Photo diode, Schottky diode	1	Black Board	T1,T2
45		Solar cell,LED	1	Black Board	T1,W3

#### **TEXT BOOKS:**

1. Jacob Millman - Electronic Devices and Circuits, McGraw Hill Education

2. Robert L. Boylestead, Louis Nashelsky- Electronic Devices and Circuits theory, 11th Edition,2009, Pearson.

#### **REFERENCE BOOKS:**

1. Horowitz -Electronic Devices and Circuits, David A. Bell – 5thEdition, Oxford.

2. Chinmoy Saha, Arindam Halder, Debaati Ganguly - Basic Electronics-Principles and Applications, Cambridge, 2018.



#### **WEB REFERENCES:**

W1. https://www.rfwireless-world.com/Terminology/CB-vs-CE-vs-CC-transistor-configurations.html

W2. <u>http://www.faadooengineers.com/online-study/post/ece/analog-electronics/557/fet-as-a-voltage-variable-resistor-vvr</u>

W3.<u>https://www.tutorialspoint.com/basic\_electronics/basic\_electronics\_special\_purpose\_diodes.h</u> <u>tm</u>

W4. <u>http://ggn.dronacharya.info/ECEDept/Downloads/QuestionBank/VIIsem/oc\_C-Unit-3-LED\_Structures.pdf</u>



### LECTURE NOTES

UNIT – 1 Diodes

https://drive.google.com/file/d/1GX10RkXW5nT11EYgosG9gxpaRBYdwEIT/view?usp=drive\_link

#### **UNIT-2 Diode Applications**

https://drive.google.com/file/d/1QkCNWI9nDZJEke3Y\_uwngswXCgZSwTSj/view?usp=drive\_link

#### **UNIT-3 Bipolar Junction Transistor (BJT)**

https://drive.google.com/file/d/1QOD0nKU5BjyQv78IIh3PzHqs6hqli7Li/view?usp=drive\_link

#### **UNIT-4 Junction Field Effect Transistor (FET)**

https://drive.google.com/file/d/1ykPUrK6oekjH5SbCSAWgTGOi6HbdD0io/view?usp=drive\_link

#### **UNIT-5 Special Purpose Devices**

https://drive.google.com/file/d/1P5mFC9O8nAep4NPiANcx4iMCCWDzHnAe/view?usp=drive\_link

#### POWER POINT PRESENTATION LINKS

UNIT-1

https://drive.google.com/file/d/1gXb7UaRibe0VGHm6PN3KbhosS1V-nZxU/view?usp=sharing

UNIT-2

https://drive.google.com/file/d/1KdQE27vDlWazVJMU8MUK84f139Ssy1EY/view?usp= sharing



#### **PREVIOUS QUESTION PAPERS**

Link:

https://drive.google.com/file/d/1KH90dftl\_RLJWQ1idPCHak3D76Agn\_i7/view?usp=drive\_link



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#### Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist., Telangana -

501510

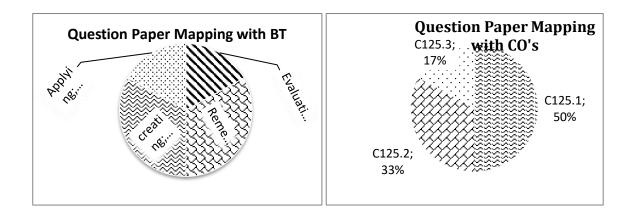
I B. TECH II SEM I – MID Examinations, Jun-2023

BR22

Branch: ECE, CSE (A,B,C), IOT, AI&DS, DS,CS, AI&ML Date: 15-06-2023(FN) Subject: ELECTRONIC DEVICES AND CIRCUITS Marks: 20 Time: 2 Hours

#### PART-B

Answ	ver any FOUR Questions. All question Carry Equal Marks	4*5 =	=20 Marks
1	Explain the working of P-N Junction under forward bias &		
	Reverse bias?	(C125.1)	(Evaluating)
2	Define static & dynamic resistances? Derive the expression for	(C125.1)	(Remembering)
	dynamic resistance?		
3	Design the Equivalent circuit of Diode with brief explanation.	(C125.1)	(Applying)
4	Draw a circuit diagram of a Bridge full wave rectifier. Explain	(C125.2)	(Creating)
	its working and draw the input and output waveforms?		
5	Define clipper? Explain any two unbiased clippers with waveforms?	(C125.2)	(Remembering)
6		(C105.2)	
6	Construct & Explain the operation of NPN Transistor?	(C125.3)	(Creating)



Set-I



#### SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY (UGC Autonomous Institution)

Accredited by NAAC with A+ Grade

Recognized under 2(f) of UGC Act 1956. (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad) Sheriguda(V), Ibrahimpatnam(M), R.R Dist., Telangana – 501 510 I B.Tech II SEM I-Mid Examinations, June-2023



Set-I

Branch: ECE, CSE(A,B,C), IOT, AI&DS, DS, CS, AI&ML

Subject Name: Electronic Devices & Circuits

#### <u>Part-A</u> <u>Objective/Quiz Paper:</u>

The objective/quiz paper is set with multiple choice, fill-in the blanks and match the following type of questions for a total of 10 marks.

#### Multiple choices:

1. How many	Terminals doe	s a P-N Junctio	on Contains	(	)
a) 3	b) 4	c) 2	d) 1		
2. What is the	cut-in voltage	of silicon PN-J	Junction diode	(	)
a) 0.3	b) 0.7	c) 1.1	d) 0.2		
3. What is the efficiency of Half wave rectifier					)
a) 81.2%	b) 40.6%	c) 73.5%	d) 78%		
4. The numbe	r of depletion r	regions in a tran	nsistor	(	)
a) 3	b)2	c)4	d)1		
<ul><li>3. What is the</li><li>a) 81.2%</li><li>4. The number</li></ul>	e efficiency of H b) 40.6% er of depletion r	Half wave recting c) 73.5% regions in a tran	d) 78%	(	)

#### Fill-in the blanks

- 1. The process of adding impurities to pure semiconductors is called\_\_\_\_\_\_.
- 2. The unwanted ac components present in the output of rectifier is called\_\_\_\_\_\_
- 3. Positive clipper circuit removes \_\_\_\_\_\_ portion of a wave forms .

4. In NPN transistor, \_\_\_\_\_\_ are the minority carriers.

#### Match the following:

#### 9.

i.	Static Resistance	(	) a. Forward bias
ii.	Dynamic Resistance	(	) b. Reverse bias
iii.	Transition Capacitance	(	) c. V/I
iv.	Diffusion Capacitance	(	) d. $\Delta V / \Delta I$



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**BR22** 

# ANSWER KEY

**Descriptive paper key link:** 

https://drive.google.com/file/d/1FRhRHBGAFttKhxPfgLSwPKbqMamnYvnO/view?usp=sha

<u>ring</u>

#### **Objective Key Paper**

#### Multiple choices:

- 1. c
- 2. b
- 3. b
- 4. b

#### Fill in the blanks:

- 5. Doping
- 6. Ripples
- 7. Positive
- 8. Electrons

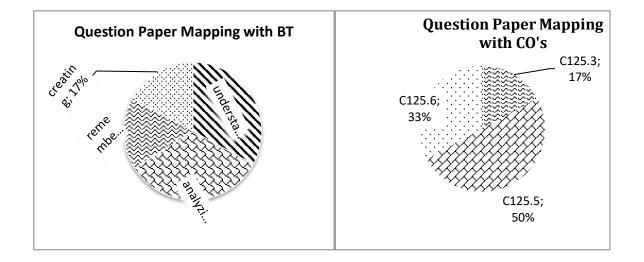
#### Match the following:

- 9.
- i. c
- ii. d
- iii. b
- iv. a

BR22

Branch: ECE, CSE(A,B,C), IOT, AI&DS, DS, CS,AI&ML Date: 18-08-2023(FN) Subject: ELECTRONIC DEVICES AND CIRCUITS Marks: 20 Time: 2 Hours

Ansv	<b>PART-B</b> wer any <b>FOUR</b> Questions. All question Carry Equal Marks	4*5 =20 M	arks
1	Explain how the transistor acts as a switch ?	(C125.3)	(Understanding)
2	Distinguish Between BJT & JFET?	(C125.5)	(Analyzing)
3	Discuss the V-I characteristics of JFET?	(C125.5)	(Creating)
4	Compare JFET & MOSFET?	(C125.5)	(Analyzing)
5	Define UJT ? Explain the operation of UJT?	(C125.6)	(Remembering)
6	Demonstrate the construction & Working of Photo Diode?	(C125.6)	(Understanding)



SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY				
(UGC Autonomous Institution)	Set-II			
Accredited by NAAC A+ Grade, Recognized under 2(f) of UGC Act 1956. (Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyder	rabad)			
Khalsa Ibrahimpatnam, Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy	y Dist.,			
Telangana – 501510				
I B. Tech II SEM II-Mid Examinations, August-2023				
Branch: ECE, CSE(A,B,C), IOT, AI&DS, DS,CS, AI&ML				
Subject Name: Electronic Devices & Circuits				
Student Name:				

### <u>Part-A</u> Objective/Quiz Paper:

The objective/quiz paper is set with multiple choice, fill-in the blanks and match the following type of questions for a total of 10 marks.

## Multiple choices:

1. Wh	at is the input terminal of CB	Configuration?		( )
a)	Base b) Collector	c) Emitter	d) None o	of the above
2 How	w many P-Regions are present	in N-Channel N	AOSFET?	( )
a)	2 b)3		c)4	d)1
3. A J	FET has three terminals, nam	ely		( )
a)(	cathode, anode, grid b) em	nitter, base, colle	ctor c)source, gat	te, drain d)None of the
Above	2			
4. Zen	er diode is used as			( )
a)	An Amplifier b)A Voltage	Regulator	c)A Coupler	d)A Rectifier
	the blanks			
1. The	e relation between $\alpha \& \beta$ is			
2. The	e input impedance of MOSFE	T is	than the J	FET.
	e Zener diode is always operation			
	ite the Terminals of UJT			·
Matcl	<u>h the following:</u>			
9.				
i.	Zener Diode	(	) a) Variable Cap	acitor
ii	Varactor Diode	(	) b) Optical Source	ce
iii	UJT	(	) c) Voltage Regu	ılator
iv	LED	(	) d)Uni Junction	Transistor



I B.Tech II SEM II-Mid Examinations, August-2023 Subject Name: Electronic Devices & Circuits

# ANSWER KEY

#### Descriptive paper key link:

https://drive.google.com/file/d/1k7uaDmgUM7XEqBwFgSo0lc2afqaJ5VA-/view?usp=sharing

#### **Objective Key Paper**

#### Multiple choices:

- 1. c
- 2. d
- 3. c
- 4. b

#### Fill in the blanks:

- 5. α=β/1+β ;β=α/1-α
- 6. More
- 7. Reverse Bias
- 8. Base1; Base2;Emitter

#### Match the following:

9. i. c ii. a iii. d iv. b

#### Mid-1 & Mid-2student answer scripts :

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https://drive.google.com/file/d/19w6Af84YvJt7xtnCfXA9YjV-InBvJuuX/view?usp=sharing

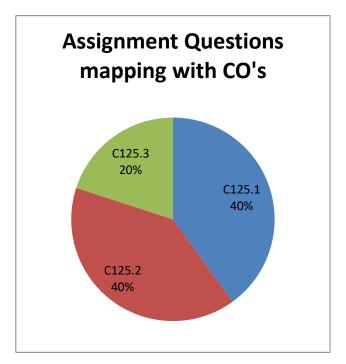
Set-II

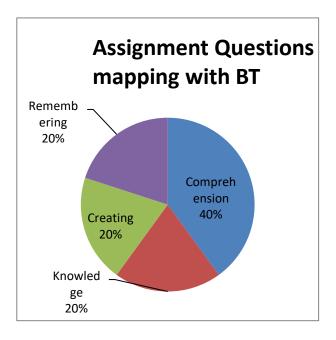


#### **ASSIGNMENT QUESTIONS (MID-I)**

#### ELECTRONIC DEVICES AND CIRCUITS (SEM-II)

Explain the working of P-N Junction under forward bias & Reverse bias?	(C125.1)	(Comprehension)
Define static & dynamic resistances? Derive the expression for dynamic resistance?	(C125.1)	(Knowledge)
What is meant by diffusion & Transition Capacitances? Derive the expression for diffusion capacitance?	(C125.1)	(Remembering)
Discuss equivalent circuit of Diode?	(C125.1)	(Creating)
Draw a circuit diagram of a Bridge full wave rectifier.	(C125.2)	
Explain its working and draw the input and output waveforms?		(Knowledge)
Derive the Efficiency of half-Wave rectifier?	(C125.2)	(Remembering)
Discuss any two unbiased clippers with waveforms?	(C125.2)	(Creating)
Explain the operation of Capacitor-Filter with neat	(C125.2)	(Comprehension)
diagrams?		
Explain the construction and operation of NPN Transistor?	(C125.3)	(Comprehension)
Explain the input and output characteristics of Transistor in CE configuration.	(C125.3)	(Comprehension)
	Reverse bias? Define static & dynamic resistances? Derive the expression for dynamic resistance? What is meant by diffusion & Transition Capacitances? Derive the expression for diffusion capacitance? Discuss equivalent circuit of Diode? Draw a circuit diagram of a Bridge full wave rectifier. Explain its working and draw the input and output waveforms? Derive the Efficiency of half-Wave rectifier? Discuss any two unbiased clippers with waveforms? Explain the operation of Capacitor-Filter with neat diagrams? Explain the construction and operation of NPN Transistor? Explain the input and output characteristics of Transistor in	Define static & dynamic resistances? Derive the expression(C125.1)for dynamic resistance?(C125.1)What is meant by diffusion & Transition Capacitances?(C125.1)Derive the expression for diffusion capacitance?(C125.1)Discuss equivalent circuit of Diode?(C125.2)Draw a circuit diagram of a Bridge full wave rectifier. Explain its working and draw the input and output waveforms?(C125.2)Derive the Efficiency of half-Wave rectifier?(C125.2)Discuss any two unbiased clippers with waveforms?(C125.2)Explain the operation of Capacitor-Filter with neat diagrams?(C125.3)Explain the construction and operation of NPN Transistor?(C125.3)Explain the input and output characteristics of Transistor in(C125.3)





MID-1 Assignment link :

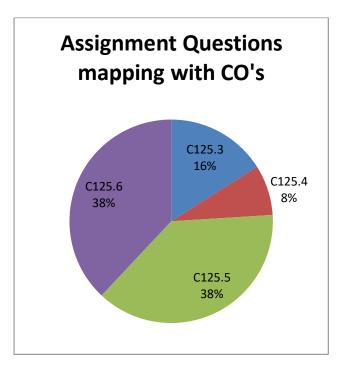
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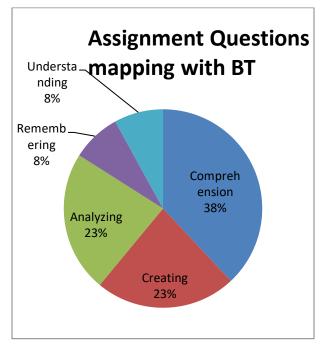


#### ASSIGNMENT QUESTIONS (MID-II)

ELECTRONIC DEVICES AND CIRCUITS (SEM-II)

1	Compare CB, CE, CC configurations?	(C125.4)	(Analyzing)
2	Explain how the transistor acts as a switch ?	(C125.3)	(Comprehension)
3	Discuss Switching times of a Transistor?	(C125.3)	(Creating)
4	Distinguish Between BJT & JFET?	(C125.5)	(Analyzing)
5	Explain the Construction & Working of N-Channel JFET?	(C125.5)	(Comprehension)
6	Discuss the V-I characteristics of JFET?	(C125.5)	(Creating)
7	Compare JFET & MOSFET?	(C125.5)	(Analyzing)
8	Explain how the MOSFET acts as a Capacitor ?	(C125.5)	(Comprehension)
9	Explain the Working & V-I Characteristics of Zener Diode?	(C125.6)	(Comprehension)
10	Explain the Construction & Working of Varactor Diode?	(C125.6)	(Comprehension)
11	Discuss the working conditions of Tunnel Diode?	(C125.6)	(Creating)
12	Define UJT ? Explain the operation of UJT?	(C125.6)	(Remembering)
13	Demonstrate the construction & Working of Photo Diode?	(C125.6)	(Understanding)





#### MID -2 Assignment

https://drive.google.com/file/d/1p8JjxFvWXWsz5-ke03nI0vTWgak6cKmM/view?usp=sharing

#### SCHEME OF EVALUATION FOR MID 1

S.NO.	DESCRIPTION	MARKS	BLOOMS TAXONOMY	СО	
	Working Principle of PN Junction	3			
1	PN Junction Forward bias, Reverse bias connection diagrams	2	(Evaluating)	(C125.1)	
2	Definition for Static ,dynamic resistances2Derivation for Static ,dynamic resistances3		(Remembering)	(C125, 1)	
<u>_</u>	Derivation for Static ,dynamic resistances	3	(Kemenibering)	(C123.1)	
3	Explanation for Equivalent circuit	2	(Applying)	(C125, 1)	
3	Diagrams for Equivalent circuit	3	(Apprying)	<ul> <li>(C125.1)</li> <li>(C125.1)</li> <li>(C125.1)</li> <li>(C125.2)</li> <li>(C125.2)</li> </ul>	
	Bridge full wave rectifier circuit diagram,				
4	waveforms	2.5	(Creating)	(C125.2)	
	Bridge full wave rectifier working principle	2.5			
5	Definition, Working of Clippers	2.5	(Remembering)	(C125.2)	
3	circuit diagram, waveforms of clippers	2.5	(Remembering)	(C125.2)	
6	NPN Transistor Construction	2	(Creating)	(C125.3)	
U	NPN Transistor Working	3	(Creating)	(C125.3)	

#### SCHEME OF EVALUATION FOR MID2

S.NO.	DESCRIPTION	MARKS	BLOOMS TAXONOMY	со
	For circuit diagram OF transistor	3		
1	Derivation Part	2	(Understanding)	(C125.3)
2	Explanation for BJT	2.5	(Analyzing)	(C125.5)
<u>_</u>	Explanation for JFET	2.5	(Analyzing)	(C123.3)
	JFET V-I characteristics waveform, Circuit			
3	diagram of JFET	3	(Creating)	(C125.5)
	Explanation of JFET	2		
4	Explanation for MOSFET Explanation for JFET	2.5 2.5	(Analyzing)	(C125.5)
	Circuit diagram, symbol of UJT	2.5		
5	Operation of UJT	2.5	(Remembering)	(C125.6)
6	Photo diode symbol, Construction	2	(Understanding)	(C125.6)
U	Working Principle	3	(Understanding)	(C123.0)



#### **Result Analysis:**

#### CSE(DATA SCIENCCE)

Course Title	ELECTRONIC DEVICES & CIRCUITS
Course Code	EC201ES
Programme	B.Tech
Year & Semester	Ist year 2 <sup>nd</sup> semester
Regulation	R22
Course Faculty	Mrs. P. SUMANA, Assistant Professor, ECE

#### Weak Students:

S No	Roll no	No of backlogs	Internal-I Status (35Marks)	Internal-II Status (40Marks)
1	22X31A6702	3	18	23
2	22X31A6705	2	17	26
3	22X31A6706	5	11	1
4	22X31A6708	2	24	20
5	22X31A6714	4	14	15
6	22X31A6722	2	19	21
7	22X31A6729	4	25	16
8	22X31A6730	2	25	19
9	22X31A6739	2	18	21
10	22X31A6740	1	14	14
11	22X31A6741	4	15	24
12	22X31A6742	2	24	24

# **Advanced learners:**

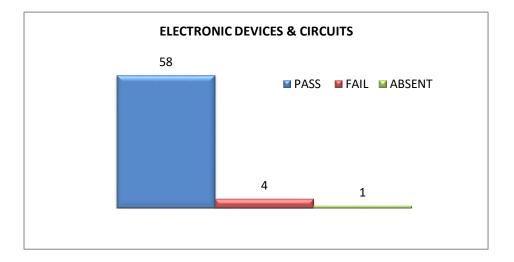
S No	Roll No	Type of support provided
1	22X31A6701	
2	22X31A6703	Advanced concepts materials is provided for advanced
3	22X31A6704	learners, Subject seminars are presented by advanced learners
4	22X31A6707	<ul> <li>in the class, advanced learners are encouraged to support slow learners.</li> </ul>
5	22X31A6711	
6	22X31A6715	
7	22X31A6718	
8	22X31A6724	
9	22X31A6725	
10	22X31A6726	
11	22X31A6733	
12	22X31A6734	
13	22X31A6736	
14	22X31A6745	
15	22X31A6746	
16	22X31A6747	
17	22X31A6750	
18	22X31A6751	
19	22X31A6759	
20	22X31A6760	
21	22X31A6762	

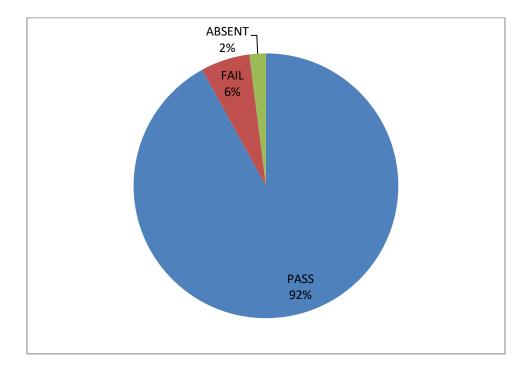


#### **RESULT ANALYSIS AT THE END OF SEMISTER**

#### **Branch: CSE(DATA SCIENCE)**

#### Subject: ELECTRONIC DEVICES & CIRCUITS







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#### DEPARTMENT OF HUMANITIES AND SCIENCE <u>REMEDIAL CLASSES TIME TABLE</u>

DAY/ PERIOD	MON 4.00-5.00	TUE 4.00-5.00	WED 4.00-5.00	THUR 4.00-5.00	FRI 4.00-5.00	SAT 4.00-5.00
CSE-A	ODE&VC	ENG	EDC	AP	ODE&VC	AP
CSE-B	AP	EDC	ODE&VC	ENG	EDC	ENG
CSE-C	ENG	AP	EDC	ODE&VC	AP	ODE&VC

DAY/ PERIOD	MON 4.00-5.00	TUE 4.00-5.00	WED 4.00-5.00	THUR 4.00-5.00	FRI 4.00-5.00	SAT 4.00-5.00
DS	EDC	AP	ODE&VC	ENG	EDC	ODE&VC
CYBER	ENG	EDC	AP	ODE&VC	AP	ENG
				·		
DAY/	MON	TUE	WED	THUR	FRI	SAT
PERIOD	4.00-5.00	4.00-5.00	4.00-5.00	4.00-5.00	4.00-5.00	4.00-5.00
AIML-A	ODE&VC	EC	EDC	BEE	EC	ODE&VC

DAY/ PERIOD	MON 4.00-5.00	TUE 4.00-5.00	WED 4.00-5.00	THUR 4.00-5.00	FRI 4.00-5.00	SAT 4.00-5.00
AI&DS	BEE	EC	ODE&VC	EDC	BEE	EC
ΙΟΤ	EC	ODE&VC	EDC	BEE	ODE&VC	EDC

DAY/ PERIOD	MON 4.00-5.00	TUE 4.00-5.00	WED 4.00-5.00	THUR 4.00-5.00	FRI 4.00-5.00	SAT 4.00-5.00
ECE	ODE&VC	BEE	EC	EDC	BEE	EC
CIVIL	ODE&VC	BEE	EC	AM	BEE	EC

Head of the Department Department of H&S SRI INDU INSTITUTE OF ENGG & TECH beriouda(M lbrahimostnam (M) R.R. Dist-501 516

Sri Indu Institute of Engineering & Tech. Sheriguda(Vill), Ibrahimpatnam R.R. Dist. Telangana-501 510.

#### SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

SULVER STATE

Department of Humanities & Sciences

and and	Course Outcome Attainment (Internal Examination-1)														
Nan	ne of the facult	P.SUI						lemic						-2023	-
	nch & Section:			-			Exar	ninati	ion.				I Inte	rnal	
	rse Name:	EDC	(00)				Year		1011.						
S.No		r	011	01-	0.01	02-			04	05-	051	0(-	Semell a Q6b Obj1 A1		
		_	Q1b	-	Q2b		QSD		Q4b		Q5D		Qod	•	A1
-	. Marks ==>	5		5		5		5		5		5		10	5
1	22X31A6701	4.5		5				3				4.5		8	5
2	22X31A6702	1		2				1				1		8	5
3	22X31A6703	5		5		_		3				5		7	5
4	22X31A6704	5		4		5		5		5				10	5
5	22X31A6705	1		4		2				2				3	5
6	22X31A6706	5		5		5		5						5	5
7	22X31A6707	3		4		5		2		0				10 10	5
8	22X31A6708 22X31A6709	2		5				Z		0				2	5
		3		3											5
10	22X31A6710	5		5				15				4.5		8 9	5
$\frac{11}{12}$	22X31A6711	5		Э				4.5 1		1		4.5		9	5
12	22X31A6712 22X31A6713	2		0				1		1		1		9 7	5
13	22X31A0713 22X31A6714	0.5		0.5				1		1				7	5
14	22X31A0714 22X31A6715	4		5				4		4				10	5
16	22X31A6716	4		2				2				3		10	5
17	22X31A6717	3		2				2		1		2		10	5
18	22X31A6718	5		5		5		5		-		5		10	5
19	22X31A6719	5		2		4		5		2		5		10	5
20	22X31A6720	5		5		5		5						9	5
21	22X31A6721	3		3		5		-				3		9	5
22	22X31A6722	2		0		-		2				1		9	5
23	22X31A6723	2		4				1						9	5
24	22X31A6724	5		5		5						5		10	5
25	22X31A6725	4		5		5						4		10	5
26	22X31A6726	5		5		4		4						10	5
27	22X31A6727	3		5		3		3						10	5
28	22X31A6728	4		4		2				2				9	5
29	22X31A6729	2		3		3				2				10	5
30	22X31A6730	3		3		2		2						10	5
31	22X31A6731	4		4				3		3				10	5
32	22X31A6732														
33	22X31A6733	5		5		5		5						10	5
34		5		5		5		5						10	5
35	22X31A6736			5		5		5		5				10	5
36	22X31A6737	5		4.5		1		2.5						9	5
37	22X31A6738	5		0		1						3		8	5
38	22X31A6739	2		0								2		9	5
39	22X31A6740	0												9	5
40	22X31A6741	1												9	5
41	22X31A6742	4		4		_		1						10	5
42	22X31A6743	5		5		5		5						10	5

			-				-		-		-			
43 22X31A6744	_		4				3		3		3		10	5
44 22X31A6745	5						5		5		5		10	5
45 22X31A6746	2		5		4						3		10	5
46 22X31A6747	5		5		5		5						9	5
47 22X31A6748	4.5		5		4.5						4		10	5
48 22X31A6749	2		4				2						10	5
49 22X31A6750	4		5		5						4		9	5
50 22X31A6751			5		4		2				4		9	5
51 22X31A6752	1		0						0		0		7	5
52 22X31A6753	2						0				0		8	5
53 22X31A6754	4.5		5				5		4.5				8	5
54 22X31A6755	3		3				3		3				8	5
55 22X31A6756	0						0						9	5
56 22X31A6757	1												9	5
57 22X31A6758	0												10	5
58 22X31A6759			5		5				5		5		10	5
59 22X31A6760	5		5		5						5		10	5
60 22X31A6761	3		1				1				1		8	5
61 22X31A6762	4		5		5						4		10	5
62 22X31A6763	3		4		3.5		1.5						9	5
63 22X31A6764	4		5		4						5		10	5
Target set by the	2	0.00		0.00		0.00			2.00		• • • •		6.00	2.00
faculty / HoD	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00
Number of														
students performed	37	0	41	0	25	0	20	0	9	0	19	0	59	62
above the target														1
Number of	57	0	51	0	30	0	37	0	18	0	27	0	62	62
students attempted Percentage of														
students scored	6 - 0 /		000/		0.000		- 40/		500/		=00/		0.50/	1000/
	65%		80%		83%		54%		50%		70%		95%	100%
more than target														
CO Mapping with	Exam	Que	stions:											
CO - 1	Y		Y										Y	Y
CO - 2	-				Y		Y				Y		Y	Y
CO - 3					1		1		v		1			
CO - 3 CO - 4									Y				Y	Y
CO - 4 CO - 5														
-														
CO - 6														
				1			!							
>Target %	65%		80%	Ļ	83%		54%		50%		70%		95%	100%
CO Attainment ba		Exai		tions:										
CO - 1	65%		80%										95%	100%
CO - 2					83%		54%				70%		95%	100%
CO - 3									50%				95%	100%
CO - 4									23/3					100/0
CO - 5														
CO - 6														
000	1	I							I		1	l		

CO	Subj	obj	Asgn	Overall	Level
CO-1	73%	88%	100%	87%	3.00
CO-2	69%	76%	100%	82%	3.00
CO-3	50%	73%	100%	74%	3.00
CO-4					
CO-5					
CO-6					

ttainn	nent Lev
1	40%
2	50%
3	60%

Attainment (Internal 1 Exam 3.00

- ALA	Sur and a sur a	C		-								•				
la la					e Attain	imen					atio	<u>n-2)</u>				
BRAMM	C. the facult	P.SUI	MANA				Acad	lemic	Year	r:				<u>2022-</u>	<u>2023</u>	
Brar	nch & Section:	CSE(I	DS)				Exan	ninati	on:					ll Inte	rnal	
Cou	rse Name:	EDC					Year	Ι						Semester:		П
																viva/
S.No	HT No.	O1a	Q1b	Q2a	Q2b	O3a	O3b	Q4a	O4b	O5a	O5b	O6a	O6b	Obj	A2	ppt
Max	. Marks ==>	5	<b>x</b>	5	<b>x</b> -~	5	<b>x</b> - ~	5	× -~	5	<b>x</b> =~	5	× **	10	5	5
1	22X31A6701	4		5		5		3		5		3		8	5	5
2	22X31A6702	3		4				3				5		9	4	5
3	22X31A6703	5		5		4		5						10	5	5
4	22X31A6704	5		5				5				5		10	5	5
5	22X31A6705	3		5		3		2				5		8	5	5
6	22X31A6706	1		1		5		2				1		9	4	5
7	22X31A6707	5		5		2		4						10	5	5
8	22X31A6708	3		1		1		2						9	4	5
9	22X31A6709	3		2				1						10	5	5
10	22X31A6710	4		4				1						9	4	5
11	22X31A6711	5		5				5				5		10	5	5
12	22X31A6712	4		2		1		5				2		9	5	5
13	22X31A6713			4				3				3		10	5	5
14	22X31A6714	1		1				1				0		9	3	5
15	22X31A6715	5		5		2		5						10	5	5
16	22X31A6716	3		3		1		3						10	5	5
17	22X31A6717	2		1				1						9	5	5
18	22X31A6718	5		5				5				5		10	5	5
19	22X31A6719	3		5				3				-		9	5	5
20	22X31A6720	-		5		4		5				4		10	5	5
21	22X31A6721	2		3		1		3						10	5	5
22	22X31A6722			2		1		2				2		10	4	5
23	22X31A6723	3		2				2						8	5	5
24	22X31A6724	-		5		5		5				5		10	5	5
25	22X31A6725	3		4		2		4				-		9	5	5
26	22X31A6726	4		4				5				5		10	5	5
27	22X31A6727	2		3				1						10	5	5
28	22X31A6728	2		2				3				3		9	3	5
29	22X31A6729			3				2				2		5	4	5
30	22X31A6730			3		1		1				2		9	3	5
31	22X31A6731	5		5		3		4						10	5	5
32																
33	22X31A6733	l		5		5		5		5				9	5	5
34	22X31A6734	5		5				4				4		10	5	5
35	22X31A6736			5				5		5		5		10	5	5
36	22X31A6737	3		4				3				3		8	5	5
37	22X31A6738	3		4		2		3						10	4	5
38	22X31A6739			5				3						10	3	5
39	22X31A6740	1		1										9	3	5
40	22X31A6741			4				3				3		9	5	5
41	22X31A6742	2		4				4				3		9	3	5
42	22X31A6743			5		2		5				4		10	5	5
43	22X31A6744			5		3		5				4		10	5	5
44	22X31A6745					5		5		5		5		10	5	5
									•	•	•	•				·

#### SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Humanities & Sciences

AND DI ENCINEERING

45	22X31A6746	4		4		2		4						10	5	5
46	22X31A6747	5		5		5						5		10	5	5
47	22X31A6748	3		4				4				3		10	5	5
48	22X31A6749	5						3				2		10	1	5
49	22X31A6750			5		4		5				4		10	5	5
50	22X31A6751	4		5				5						9	5	5
51	22X31A6752			2								1		10	4	5
52	22X31A6753			2				1						9	5	5
53	22X31A6754			5		4		5				4		10	5	5
54	22X31A6755	3		4		1		2						10	5	5
55	22X31A6756			4				4				4		10	4	5
56	22X31A6757			1								1		8	5	5
57	22X31A6758			3				3				2		9	4	5
58	22X31A6759	5		5				5				5		10	5	5
59	22X31A6760	4		5				5				5		10	5	5
60	22X31A6761	3		3				4		1				10	5	5
61	22X31A6762	4		5		2		5						10	3	5
62	22X31A6763	4		4		3								8	5	5
63	22X31A6764	3		4		3		4						9	5	5
-	et set by the	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	6.00	3.00	3.00
facu	lty / HoD	5.00	0.00	3.00	0.00	3.00	0.00	3.00	0.00	5.00	0.00	3.00	0.00	0.00	3.00	3.00
stud	nber of ents performed we the target	34	0	47	0	13	0	42	0	3	0	24	0	61	13	62
stud	ber of ents attempted entage of	42	0	60	0	27	0	56	0	4	0	33	0	62	13	62
stud	entige of ents scored e than target	81%		78%		48%		75%		75%		73%		98%	100%	100%
CO	Mapping with	Exam	Quest	ions:												
	CO - 1															Y
	CO - 2															Y
	CO - 3	Y												Y	Y	Y
	CO - 4	1				Y								Y	Y	Y
	CO - 4 CO - 5					I		Y		Y				Y	I Y	Y
	CO - 6			Y				1		1		Y		Y	Y	Y
	00 0			1								1		1	1	1
% S	tudents Scored	1										I				
	>Target %	81%		78%		48%		75%		75%		73%		98%	100%	100%
	Attainment bas		Exam		ons:	.070		1010		1010		1010		2070	10070	10070
	CO - 1															100%
	CO - 2															100%
		0101												0.00 /	10001	
	CO - 3	81%				1001						ļ		98%	100%	100%
	CO - 4					48%						ļ		98%	100%	100%
	CO - 5							75%		75%				98%	100%	100%
	CO - 6			78%								73%		98%	100%	100%
		a				c		r ·	ł							1
	CO	Subj	obj	asgn	ppt	Ove		Leve							inment	
	CO-1				100%		0%	3.00						1		)%
	CO-2				100%	10	0%	3.00						2	5	0%
	CO-3	81%	98%	100%	100%	95	%	3.00						3	6	0%
	CO-4	48%	98%	100%	100%	87	'%	3.00								
	CO-5	75%	98%	100%	100%	93		3.00								
		76%	98%	-				3.00								
	CO-6	/070	7070	100%	100%	93	70	5.00								

Attainment (Internal Examinatic 3.00

# SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY



Department of Humanities & Sciences Course Outcome Attainment (University Examinations)

Academic Year:

Year / Semester:

- HORAHRANDE THE			•••••
	of the faculty :		
	& Section:	CSE(DS)	
Course		EDC	_
S.No	Roll Number	Marks Secured	
1	22X31A6701	32	
2	22X31A6702	30	
3	22X31A6703	32	
4	22X31A6704	44	
5	22X31A6705	36	
6	22X31A6706	16	
7	22X31A6707	32	
8	22X31A6708	26	
9	22X31A6709	24	
10	22X31A6710	22	
11	22X31A6711	39	
12	22X31A6712	25	
13	22X31A6713	24	
14	22X31A6714	27	
15	22X31A6715	47	
16	22X31A6716	26	
17	22X31A6717	28	
18	22X31A6718	43	
19	22X31A6719	25	
20	22X31A6720	41	
21	22X31A6721	32	
22	22X31A6722	34	
23	22X31A6723	26	
24	22X31A6724	40	
25	22X31A6725	32	
26	22X31A6726	32	
27	22X31A6727	29	
28	22X31A6728	28	
29	22X31A6729	35	
30	22X31A6730	39	
31	22X31A6731	48	
32	22X31A6732		
33	22X31A6733	42	
34	22X31A6734	40	
35	22X31A6736	44	
Max Ma	arks	60	
Class A	verage mark		32
Number	of students perf	formed above the target	36
	of successful st	-	62
Percenta	ige of students s	cored more than target	58%
Attai	3		

S.No	Roll Number	Marks Secured
36	22X31A6737	47
37	22X31A6738	40
38	22X31A6739	46
39	22X31A6740	22
40	22X31A6741	22
41	22X31A6742	33
42	22X31A6743	32
43	22X31A6744	34
44	22X31A6745	53
45	22X31A6746	38
46	22X31A6747	49
47	22X31A6748	32
48	22X31A6749	6
49	22X31A6750	38
50	22X31A6751	30
51	22X31A6752	21
52	22X31A6753	22
53	22X31A6754	51
54	22X31A6755	26
55	22X31A6756	36
56	22X31A6757	14
57	22X31A6758	3
58	22X31A6759	49
59	22X31A6760	52
60	22X31A6761	26
61	22X31A6762	35
62	22X31A6763	25
63	22X31A6764	31
64		
65		
66		
67		
68		
69		
70		

2022-2023

<u>| / ||</u>

Attainment Level	% students
1	40%
2	50%
3	60%

STATE STATE	De	partment of Hum	anities & So	ciences	
Constanting of the second seco		Course Out	tcome Att	<u>ainment</u>	
N le faculty	P.SUMAN	<u>A</u>		Academic Year:	<u>2022-2023</u>
Branch & Section:	<u>CSE(DS)</u>			Examination:	<u>Internal</u>
Course Name:	<u>EDC</u>			Year:	<u>l</u>
				Semester:	<u>II</u>
	1st Internal	2nd Internal	Internal		
Course Outcomes	Exam	Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00	3.00	3.00	3.00	3.00
CO2	3.00	3.00	3.00	3.00	3.00
CO3	3.00	3.00	3.00	3.00	
	2100	2.00	2.00	2100	3.00
<b>CO4</b>		3.00	3.00	3.00	3.00
CO5		3.00	3.00	3.00	
		5.00	5.00	5.00	3.00
CO6		3.00	3.00	3.00	3.00
Inter	nal & Unive	ersity Attainment:	3.00	3.00	
		Weightage	25%	75%	
CO Attainment for th	e course (In	ternal, University	0.75	2.25	
CO Attainment for	the course	(Direct Method)		3.00	

# SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Overall course attainment level 3.00

# SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Humanities & Sciences

#### Program Outcome Attainment (from Course)

SIRA AMARON THUN				$\mathbf{P}$	rogram	Outco	ome Atta	inment	t (from C	<u>(ourse)</u>						
Name of Faculty:			P.SUMANA						emic Yeai	r:	<u>2022-2023</u>					
Branch & Section:			CSE(DS)						Year:			1				
Course N	<u>EDC</u>	Semester:														
CO-PO m	nappir	ng														
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2		
CO1	3	2	-	-	3	-	-	-	-	-	2	3	3	3		
CO2	-	1	3	-	-	-	1	-	-	-	2	2	3	3		
CO3	1	3	-	-	2	1	-	-	-	-	2	-	3	3		
CO4	2	-	2	2	-	-	-	-	-	-	2	3	3	3		
CO5	2	3	3	-	3	-	-	1	-	-	2	2	3	3		
CO6	3	3	-	-	3	-	-	-	1	1	2	3	3	3		
Course	2.2	2.4	2.67	2	2.75	1	1	1	1	1	2	2.6	3	3		
со		Course Outcome Attainment														
	3.00													1		
CO1																
							3.	00								
CO2							Ę.									
							3.	00								
СОЗ																
							3.	00								
CO4																
							3.	00								
CO5																
CO6	3.00															
Overall	cours	e atta	ainmer	nt leve	el				3.	.00				-		
1									_							

#### **PO-ATTAINMENT**

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO														
Attainm ent	2.20	2.40	2.67	2.00	2.75	1.00	1.00	1.00	1.00	1.00	2.00	2.60	3.00	3.00

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)



#### SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY (UGC AUTONOMOUS INSTITUTION)

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#### ATTENDANCE REGISTER

https://drive.google.com/file/d/1NJctgTeitj4T\_0RP529bBde7r7iblAlz/view?usp=sharing