Sri Indu Institute of Engineering & Technology

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COURSE FILE

ON

ANALOG AND DIGITAL ELECTRONICS LAB

Course Code- CS306ES

II B.Tech I-SEMESTER

A.Y.:2022-2023

Prepared by

Mrs.S.Alekhya
Assistant Professor

B. Rahul Kanth
Computer Science & Engg. Dept.
SRI INDU INSTITUTE OF ENGG & TECH.
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Sheriguda(Vill), Ibrahimpatnam
R.R. Dist. Telangana-501 510.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Academic Year	2022-2023
Course Title	ANALOG AND DIGITAL ELECTRONICS LAB
Course Code	CS306ES
Room Number	A-114
Name of the lab incharge	Mr.K.Rajender
Name of the faculty incharge	Mrs.S.Alekhya

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

INSTITUTE VISION AND MISSION

Vision:

To become a premier institute of academic excellence by providing the world class education that transforms individuals into high intellectuals, by evolving them as empathetic and responsible citizens through continuous improvement.

Mission:

IM1: To offer outcome-based education and enhancement of technical and practical skills.

IM2: To continuous assess of teaching-learning process through institute-industrycollaboration..

IM3: To be a centre of excellence for innovative and emerging fields in technology development with state-of-art facilities to faculty and students fraternity.

IM4: To create an enterprising environment to ensure culture, ethics and social responsibility among the stakeholders

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

DEPARTMENT VISION AND MISSION

Vision:

To become a prominent knowledge hub for learners, strive for educational excellence with innovative and industrial techniques so as to meet the global needs.

Mission:

DM1 : To provide ambience that enhances innovations, problem solving skills, leadership qualities, decision making, team-spirit and ethical responsibilities.

DM2 : To impart quality education with professional and personal ethics, so as to meet the challenging technological needs of the industry and society.

DM3 : To provide academic infrastructure and develop linkage with the world class organizations to strengthen industry-academia relationships for learners.

DM4 : To provide and strengthen new concepts of research in the thrust area of Computer Science and Engineering to reach the needs of Government and Society.

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

PROGRAM EDUCATIONAL OBJECTIVES

PEO1: To develop trained graduates with strong academic and technical skills of modern computer science and engineering.

PEO2: To promote trained graduates with leadership qualities and the ability to solve real time problems using current techniques and tools in interdisciplinary environment.

PEO3: To motivate the graduates towards lifelong learning through continuing education and professional development.

PROGRAM SPECIFIC OUTCOMES

PSO1 : **Professional Skills:** To implement computer programs of varying complexity in the areas related to Web Design, Cloud Computing, Network Security and Artificial Intelligence.

PSO2: **Problem-Solving Skills**: To develop quality products using open ended programming environment.

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PROGRAMME OUTCOMES (POs)

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design/development of solutions:**Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesisof the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO6: **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities andnorms of the engineering practice.

PO9: **Individual and team work:** Function effectively as an individual, and as a member orleader in diverse teams, and in multidisciplinary settings.

PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give andreceive clear instructions.

PO11: **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning:** Recognize the need for, and have the preparation and ability to engagein independent and life-long learning in the broadest context of technological change.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. tech. in COMPUTER SCIENCE AND ENGINEERING

II YEAR COURSE STRUCTURE AND SYLLABUS (R18)

Applicable From 2018-19Admitted Batch

II YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	CS301ES	Analog and Digital Electronics	3	0	0	3
2	CS302PC	Data Structures	3	1	0	4
3	MA303BS	Computer Oriented Statistical Methods	3	1	0	4
4	CS304PC	Computer Organization and Architecture	3	0	0	3
5	CS305PC	Object Oriented Programming using C++	2	0	0	2
6	CS306ES	Analog and Digital Electronics Lab	0	0	2	1
7	CS307PC	Data Structures Lab	0	0	3	1.5
8	CS308PC	IT Workshop Lab	0	0	3	1.5
9	CS309PC	C++ Programming Lab	0	0	2	1
10	*MC309	Gender Sensitization Lab	0	0	2	0
		Total Credits	**14**	**2**	**12**	**21**

II YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1	CS401PC	Discrete Mathematics	3	0	0	3
2	SM402MS	Business Economics & Financial Analysis	3	0	0	3
3	CS403PC	Operating Systems	3	0	0	3
4	CS404PC	Database Management Systems	3	1	0	4
5	CS405PC	Java Programming	3	1	0	4
6	CS406PC	Operating Systems Lab	0	0	3	1.5
7	CS407PC	Database Management Systems Lab	0	0	3	1.5
8	CS408PC	Java Programming Lab	0	0	2	1
9	*MC409	Constitution of India	3	0	0	0
		Total Credits	**18**	**2**	**8**	**21**

***MC-Satisfactory/Unsatisfactory**

ANALOG AND DIGITAL ELECTRONICS LAB

B.Tech. II Year I Sem. **LT/PC 00/21**

Course Objectives

1. To introduce components such as diodes, BJTs and FETs.
2. To know the applications of components.
3. To give understanding of various types of amplifier circuits
4. To learn basic techniques for the design of digital circuits and fundamental conceptsused in the design of digital systems.
5. To understand the concepts of combinational logic circuits and sequential circuits.

Course Outcomes: Upon completion of the Course, the students will be able to:

1. Know the characteristics of various components.
2. Understand the utilization of components.
3. Design and analyze small signal amplifier circuits.
4. Postulates of Boolean algebra and to minimize combinational functions
5. Design and analyze combinational and sequential circuits
6. Known about the logic families and realization of logic gates.

LIST OF EXPERIMENTS

1. Full Wave Rectifier with & without filters
2. Common Emitter Amplifier Characteristics
3. Common Base Amplifier Characteristics
4. Common Source amplifier Characteristics
5. Measurement of h-parameters of transistor in CB, CE, CC configurations
6. Input and Output characteristics of FET in CS configuration
7. Realization of Boolean Expressions using Gates
8. Design and realization logic gates using universal gates
9. generation of clock using NAND / NOR gates
10. Design a 4 – bit Adder / Subtractor
11. Design and realization a Synchronous and Asynchronous counter using flip-flops
12. Realization of logic gates using DTL, TTL, ECL, etc.

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Website: https://siiet.ac.in/

Course: Analog & Digital Electronics Lab (C216) **Class: II CSE-A Course Outcomes**

After completing this course the student will be able to:

CO Number	Course Outcomes	Bloom's Taxonomy
C216.1	Design and test rectifiers with filters.	Comprehensive, Understand
C216.2	Design, construct and test amplifier circuits and interpret the results.	Creative , comprehensive
C216.3	Utilize the postulates of the Boolean Algebra to minimize the Combinational circuits.	Creative
C216.4	Design and Analyze Combinational and Sequential circuits and verify the functionality.	Comprehensive
C216.5	Realize the logic gates using different Logic families and verify the functionality.	Comprehensive, Understand
C216.6	Design a Adder/ subtractor and synchronous & asynchronous counter using flip-flop	Applying , Analyzing

Mapping of course outcomes with program outcomes:

High-3 Medium-2 Low-1

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	P12	PSO1	PSO2
C216.1	3	3	-	3	-	-	-	-	-	-	-	-	3	3
C216.2	2	3	2	2	-	-	-	-	-	-	2	-	2	2
C216.3	2	3	2	2	-	-	-	-	-	-		3	3	3
C216.4	1	3	2	2	-	-	-	-	-	-	2	-	3	3
C216.5	3	2	1	2	-	-	-	-	-	-	-	3	2	2
C216.6	2	3	2		-	-	-	-	-	-	-	-	1	1
C216	**2.17**	**2.83**	**1.83**	**2.00**	-	-	-	-	-	-	**2**	**3**	**2.33**	**2.33**

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LIST OF EXPERIMENTS AND THEIR CO, PO/PSO MAPPING

S.No	Name of The Experiment	CO	PO/PSO
1	Full Wave Rectifier with & without filters	1	PO1,PO2,PO4, PSO1,PSO2
2	Common Emitter Amplifier Characteristics	2	PO1,PO2,PO3,PO4,PO11, PSO1,PSO2
3	Common Base Amplifier Characteristics	2	PO1,PO2,PO3,PO4,PO11, PSO1,PSO2
4	Common Source amplifier Characteristics	2	PO1,PO2,PO3,PO4,PO11, PSO1,PSO2
5	Measurement of h-parameters of transistor in CB, CE, CC configurations	2	PO1,PO2,PO3,PO4,PO11, PSO1,PSO2
6	Input and Output characteristics of FET in CS configuration	2	PO1,PO2,PO3,PO4,PO11, PSO1,PSO2
7	Realization of Boolean Expressions using Gates	3	PO1,PO2,PO3,PO4,PO12, PSO1,PSO2
8	Design and realization logic gates using universal gates	3	PO1,PO2,PO3,PO4,PO12, PSO1,PSO2
9	generation of clock using NAND / NOR gates	4	PO1,PO2,PO3,PO4,PO11, PSO1,PSO2
10	Design a 4 – bit Adder / Subtractor	6	PO1,PO2,PO3,PSO1,PSO2
11	Design and realization a Synchronous and Asynchronous counter using flip-flops	6	PO1,PO2,PO3,PSO1,PSO2
12	Realization of logic gates using DTL, TTL, ECL, etc.	5	PO1,PO2,PO3,PO4,PO12, PSO1,PSO2

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TIME TABLE FOR A.Y 2022-23

Class: II-B. Tech CSE -A **Semester: I** **LH. NO: A-301** **W.E.F:28-11-2022**

Period/ Day	1	2	3	4	1:00-1:30	5	6	7
	9:40-10:30	10:30-11:20	11:20-12:10	12:10-1:00		1:30-2:20	2:20-3:10	3:10-4:00
Monday	COSM	ITWS LAB(BATCH-I)/ A&DE LAB(BATCH-II)			LUNCH	A&DE	DS	C++
Tuesday	COSM	C++	COA	DS		A&DE	CO-C/SS/DAA	
Wednesday	C++	COSM	INT	COA		DS LAB(BATCH-I)/ C++ LAB(BATCH-II)		
Thursday	DS	GS LAB		COSM/DS(T)		C++	A&DE	SPORTS
Friday	COA	DS LAB(BATCH-II)/ C++ LAB(BATCH-I)				A&DE	LIB	DS/COSM(T)
Saturday	C++	DS	COUN	COA		ITWS LAB(BATCH-II)/ A&DE LAB(BATCH-I)		

(T) – Tutorial (concern faculty)

Subject Code	Subject Name	Name of the Faculty	Subject Code	Subject Name	Name of the Faculty
CS301ES	Analog and Digital Electronics	Mrs. S.Alekhya	CS309PC	C++ Programming Lab	Mrs P H Swarna Rekha/ Mrs.P.Souwjanya/ Mrs.G.Swapna
CS302PC	Data Structures	Mrs. D.Rajeshwari	MC309	Gender Sensitization Lab	Mrs S Swapna
MA303BS	Computer Oriented Statistical Methods	Mrs. B.Ramadevi		CO-C/SS/DAA	Mrs. D.Rajeshwari
CS304PC	Computer Organization and Architecture	Dr. Sasikumar D	Sports	Sports	Mr K Veera Kishore
CS305PC	Object Oriented Programming Using C++	Mrs P H Swarna Rekha	Internet	Internet	Mrs. Ch Sai Vijaya
CS306ES	Analog and Digital Electronics Lab	Mrs. S.Alekhya	LIB	Library	Mrs P H Swarna Rekha
CS307PC	Data Structures Lab	Mrs. D.Rajeshwari/ Mrs D.Uma/ Mrs.A.Sudha	COUN	Counselling	Mrs.R.Sravanthi
CS308PC	IT Workshop Lab	Mrs T Ramya Priya/ Mrs.Ch.Sai Vijaya/ Mrs. Jakkala Priyanka			

Class In-Charge : Mrs. D.Rajeshwari **Mentor 1** : Mrs. D.Rajeshwari **Mentor 2:** Mrs P H Swarna Rekha

Class In-Charge HOD PRINCIPAL

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Lab External Question Paper

Subject Name: Analog and Digital Electronics Lab **Year & Semester: II-I** **A.Y:2022-2023**

1. Full Wave Rectifier with & without filters.
2. Common Emitter Amplifier Characteristics
3. Common Base Amplifier Characteristics
4. Common Source amplifier Characteristics
5. Measurement of h-parameters of transistor in CB, CE, CC configurations
6. Input and Output characteristics of FET in CS configuration
7. Realization of Boolean Expressions using Gates
8. Design and realization logic gates using universal gates
9. generation of clock using NAND / NOR gates
10. Design a 4 – bit Adder / Subtractor
11. Design and realization a Synchronous and Asynchronous counter using flip-flops
12. Realization of logic gates using DTL, TTL, ECL, etc.

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A&DE Lab External Time-Table
With Examiner

A.Y.: 2022-23 **SEM-I**

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY
LAB EXTERNAL EXAMINATIONS TIME-TABLE, APR-2023 (I SEM)
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING(IOT,CS,AIML,AI&DS)
TIMINGS FN: 10:00 AM TO 1:0 PM AN: 1:00PM TO 4:00PM Date:04/04/2023

S.NO	YEAR/ SEC	NAME OF THE LAB	DATE	SESSION	LOCATION	NAME OF THE INTERNAL EXAMINER	NAME OF THE EXTERNAL EXAMINER
1	II-I-CSE-A	A&DE LAB	15/4/2023	FN	LAB NO-A-114	Mrs.K.Padma	Mr. S. Kranthi Reddy (9573013861)
2		DATA STRUCTURES LAB	04-12-23	AN	LAB NO-1,2	Mrs.D.Rajeshwari	Mr.G. Harish Reddy (9963992727)
3		IT WORKSHOP LAB	04-11-23	FN	LAB NO-10A	Mrs.S.Sandhya	Mrs. R. Akshara(9177841919)
4		PROGRAMMING	13/4/2023	AN	LAB NO-4,6	Mrs.M.Swapna	Dr. B.Srinu(8185924275)
5	II-I-CSE-B	A&DE LAB	04-11-23	FN	LAB NO-A-114	Mrs.K.Padma	Mr.G. Harish Reddy (9963992727)
6		DATA STRUCTURES LAB	13/4/2023	FN	LAB NO-1,2	Mrs.D.Uma	Mr. S. Kranthi Reddy (9573013861)
7		IT WORKSHOP LAB	04-12-23	AN	LAB NO-4,6	Mrs.S.Sandhya	Mr. CH. Chaitanya kumar(8500330546)
8		PROGRAMMING	15/4/2023	FN	LAB NO-4,6	Mrs.M.Karuna	Mrs.K.L. Anusha(9704446862)
9	II-I-CSE-C	A&DE LAB	04-12-23	AN	LAB NO-A-114	Mrs.K.Padma	Mr. S. Kranthi Reddy (9573013861)
10		DATA STRUCTURES LAB	13/4/2023	AN	LAB NO-1,2	Mr.P.Sri Ramulu	Mrs. Durga Devi(9948353838)
11		IT WORKSHOP LAB	15/4/2023	FN	LAB NO-10A	Mrs.S.Sandhya	Mrs.K.L. Anusha(9704446862)
12		PROGRAMMING	04-11-23	FN	LAB NO-4,6	Mrs.M.Swapna	Mr. U.Nehru(9912226377)

HOD
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LAB OCCUPANCY CHART

Analog &Digital Electronics LAB

ROOMNO: A-114 **BLOCK: A** **FLOOR: I**

	I 9:40-10:30	II 10:30-11:20	III 11:20-12:10	IV 12:10-1:00	LUNCH	V 1:30-2:20	VI 2:20-3:10	VII 3:10-4:00
MON		**II BTECH I SEM CSE-A**						
TUE						**II BTECH I SEM CSE-B**		
WED		**II BTECH I SEM CSE-C**						
THU						**II BTECH I SEM CSE-C**		
FRI		**II BTECH I SEM CSE-B**						
SAT						**II BTECH I SEM CSE-A**		

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Do's and Don'ts

Do's

1. Come with completed observation and record.
2. Remove your shoes or wear foot socks before you enter the lab.
3. Always keep quiet. Be considerate to other lab users.
4. Report any problems with the computer to the person in charge.
5. Shut down the computer properly.
6. Wear ID card before entering into the lab.
7. Read and understand how to carry out an activity thoroughly before coming to the lab.
8. Write In time, Out time and system details in the login register

Don'ts

1. Do not touch any part of the computer with wet hands.
2. Do not change system settings.
3. Do not hit the keys on the computer too hard.
4. Don't damage, remove, or disconnect any labels, parts, cables or equipment.
5. Do not install or download any software or modify or delete any system files on any lab computers
6. Do not disturb your neighboring students. They may be busy in completing tasks.
7. Do not remove anything from the computer laboratory without permission.
8. Do not use pen drives.

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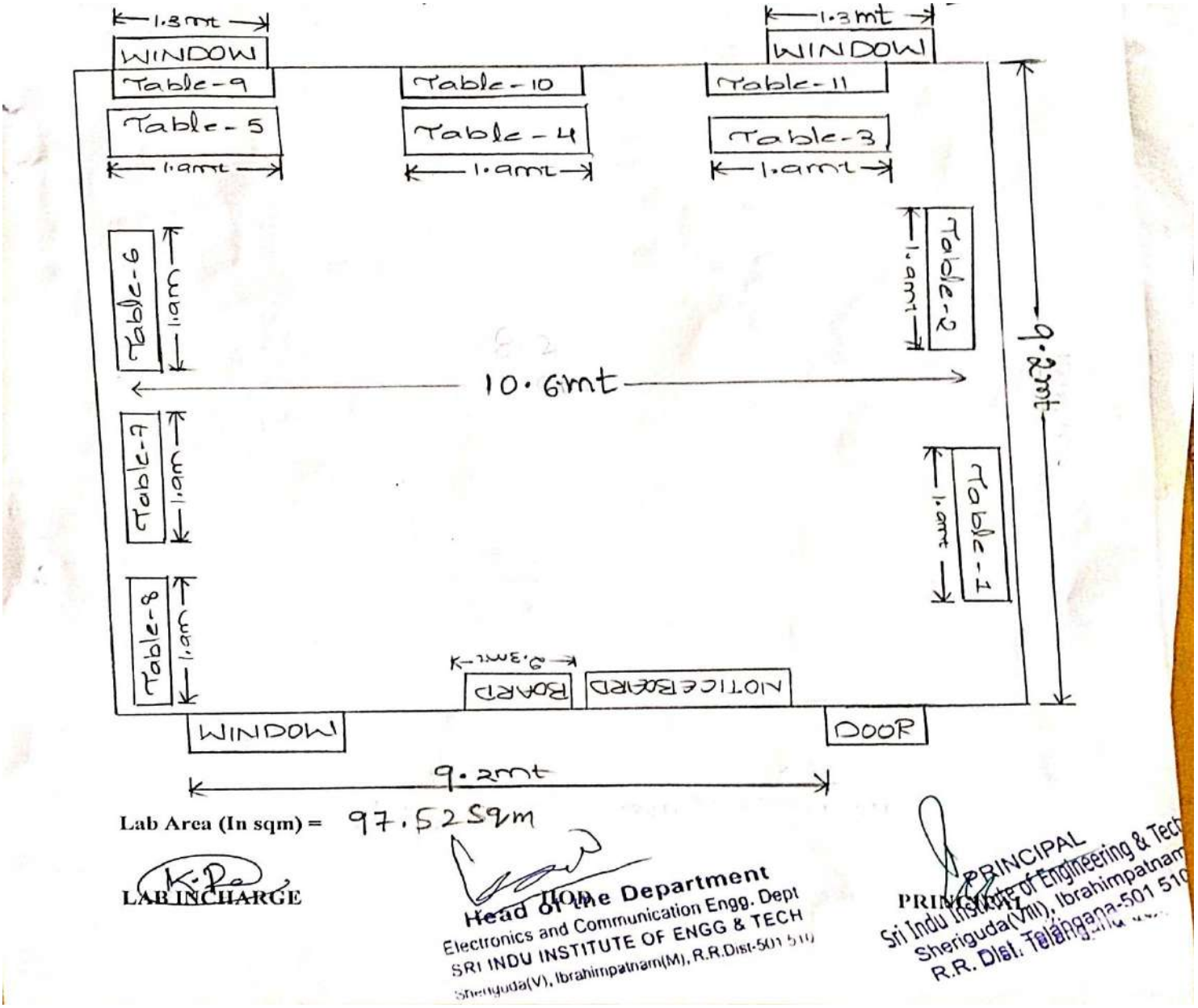
Analog & Digital Electronics LAB

PHYSICAL LAB- FLOOR PLAN

ROOM NO: A-114 **BLOCK: A** **FLOOR:1**



Lab Area (In sqm) = 97.529sqm

LAB INCHARGE

HOD
Head of the Department
Electronics and Communication Engg. Dept
SRI INDU INSTITUTE OF ENGG & TECH
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Lab manual link:

https://drive.google.com/file/d/1AmtDTALFyfYSQFSI47k2oHTiuSziSu6Y/view?usp=sharing

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Computer Science and Engineering

Course Outcome Attainment (Internal Examination-1)

Name of the faculty : S.ALEKHYA 2022-23
Branch & Section: CSE - A I Internal
Course Name: A&DE Lab Year/Semester: II/I

S.No	HT No.	A+A+CD+MG	T+P+C+R	DDE
Max. Marks ==>		5	5	15
1	21X31A0501	4	5	14
2	21X31A0502	4	5	15
3	21X31A0503	5	4	14
4	21X31A0504	5	5	13
5	21X31A0505	5	5	14
6	21X31A0506	5	5	15
7	21X31A0507	5	4	14
8	21X31A0508	5	5	13
9	21X31A0509	5	5	15
10	21X31A0510	5	5	12
11	21X31A0511	5	5	14
12	21X31A0512	5	4	14
13	21X31A0513	4	5	14
14	21X31A0514	5	5	13
15	21X31A0515	5	5	14
16	21X31A0516	5	5	12
17	21X31A0517	5	5	15
18	21X31A0518	5	5	14
19	21X31A0519	5	4	14
20	21X31A0520	5	5	14
21	21X31A0521	4	5	14
22	21X31A0522	5	5	14
23	21X31A0523	5	4	14
24	21X31A0524	5	5	15
25	21X31A0525	5	5	13
26	21X31A0526	4	5	15
27	21X31A0527	4	5	14
28	21X31A0528	5	4	12
29	21X31A0529	5	5	14
30	21X31A0530	5	5	13
31	21X31A0531	5	4	14
32	21X31A0532	5	4	15
33	21X31A0533	5	4	15
34	21X31A0534	5	5	13
35	21X31A0535	5	5	14
36	21X31A0536	4	4	13
37	21X31A0537	5	5	14
38	21X31A0538	5	5	12
39	21X31A0539	5	5	14
40	21X31A0540	5	5	14
41	21X31A0541	5	4	14
42	21X31A0542	5	5	14
43	21X31A0543	5	4	13
44	21X31A0544	4	4	6
45	21X31A0545	5	5	15
46	21X31A0546	5	5	14
47	21X31A0547	3	5	6
48	21X31A0548	5	5	15

49	21X31A0549	5	4	14
50	21X31A0550	5	5	13
51	21X31A0552	5	5	14
52	21X31A0554	5	5	15
53	21X31A0555	4	5	15
54	21X31A0556	5	5	14
55	21X31A0557	4	5	14
56	21X31A0559	5	5	15
57	21X31A0560	5	5	14
58	21X31A0561	5	5	13
59	21X31A0562	3	4	15
60	21X31A0563	4	5	11
61	21X31A0564	5	5	15
62	21X31A0565	5	5	15
63	22X35A0501	5	4	14
64	22X35A0502	5	5	14
65	22X35A0503	5	5	14
66	22X35A0504	5	4	13
67	22X35A0505	5	5	15
68	22X35A0506	5	5	14
69	22X35A0507	5	4	14
70	22X35A0508	5	5	14
Target set by the faculty / HoD		3.00	3.00	9.00
Number of students performed above the target		60	60	58
Number of students attempted		60	60	60
Percentage of students scored more than target		100%	100%	97%

CO Mapping with Exam Questions:

CO - 1	y	y	Y
CO - 2	y	y	Y
CO - 3	y	y	Y
CO - 4	y	y	Y
CO - 5	y	y	Y
CO - 6	y	y	Y

CO Attainment based on Exam Questions:

CO - 1	100%	100%	97%
CO - 2	100%	100%	97%
CO - 3	100%	100%	97%
CO - 4	100%	100%	97%
CO - 5	100%	100%	97%
CO - 6	100%	100%	97%

CO	Intrnal practica	DDE	Overall	Level
CO-1	100%	97%	98%	3
CO-2	100%	97%	98%	3
CO-3	100%	97%	98%	3
CO-4	100%	97%	98%	3
CO-5	100%	97%	98%	3
CO-6	100%	97%	98%	3

Attainment I
1
2
3

Attainment (Internal 1 Examination) = **3**

Level
40%
50%
60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Computer Science and Engineering

Course Outcome Attainment (Internal Examination-2)

Name of the faculty : S.ALEKHYA 2022-23
Branch & Section: CSE- A II Internal
Course Name: A&DE LAB Semester: I

S.No	HT No.	A+A+CD+MG	T+P+C+R	DDE
Max. Marks ==>		5	5	15
1	21X31A0501	4	5	14
2	21X31A0502	4	5	14
3	21X31A0503	5	4	14
4	21X31A0504	5	5	13
5	21X31A0505	5	5	14
6	21X31A0506	5	5	15
7	21X31A0507	5	5	14
8	21X31A0508	5	5	13
9	21X31A0509	5	5	15
10	21X31A0510	5	4	12
11	21X31A0511	5	5	13
12	21X31A0512	5	4	14
13	21X31A0513	4	5	14
14	21X31A0514	5	5	13
15	21X31A0515	4	5	14
16	21X31A0516	5	5	12
17	21X31A0517	5	5	15
18	21X31A0518	5	5	14
19	21X31A0519	5	4	14
20	21X31A0520	5	5	13
21	21X31A0521	4	5	14
22	21X31A0522	5	5	14
23	21X31A0523	5	4	14
24	21X31A0524	5	5	14
25	21X31A0525	5	5	13
26	21X31A0526	4	5	15
27	21X31A0527	4	5	14
28	21X31A0528	5	5	12
29	21X31A0529	5	5	14
30	21X31A0530	5	5	13
31	21X31A0531	5	4	14
32	21X31A0532	5	4	15
33	21X31A0533	5	5	15
34	21X31A0534	5	5	13
35	21X31A0535	5	5	14
36	21X31A0536	4	4	13
37	21X31A0537	5	5	13
38	21X31A0538	5	5	12
39	21X31A0539	5	5	14
40	21X31A0540	5	5	14
41	21X31A0541	5	4	14

42	21X31A0542	5	4	14
43	21X31A0543	5	4	13
44	21X31A0544	4	4	6
45	21X31A0545	5	5	15
46	21X31A0546	5	5	14
47	21X31A0547	3	5	6
48	21X31A0548	5	5	14
49	21X31A0549	5	4	13
50	21X31A0550	5	5	13
51	21X31A0552	5	5	14
52	21X31A0554	5	5	15
53	21X31A0555	4	5	15
54	21X31A0556	5	5	14
55	21X31A0557	4	5	15
56	21X31A0559	5	5	15
57	21X31A0560	5	5	14
58	21X31A0561	5	5	13
59	21X31A0562	3	4	15
60	21X31A0563	4	5	11
61	21X31A0564	5	5	15
62	21X31A0565	5	5	15
63	22X35A0501	5	5	14
64	22X35A0502	5	5	14
65	22X35A0503	5	5	14
66	22X35A0504	5	4	12
67	22X35A0505	5	5	15
68	22X35A0506	5	5	14
69	22X35A0507	5	5	14
70	22X35A0508	5	5	14
Target set by the faculty / HoD		3.00	3.00	9.00
Number of students performed above the target		51	51	49
Number of students attempted		51	51	51
Percentage of students scored more than target		100%	100%	96%

CO Mapping with Exam Questions:

CO - 1	**y**	**y**	Y
CO - 2	**y**	**y**	Y
CO - 3	**y**	**y**	Y
CO - 4	**y**	**y**	Y
CO - 5	**y**	**y**	Y
CO - 6	**y**	**y**	Y

CO Attainment based on Exam Questions:

CO - 1	100%	100%	96%
CO - 2	100%	100%	96%
CO - 3	100%	100%	96%
CO - 4	100%	100%	96%
CO - 5	100%	100%	96%
CO - 6	100%	100%	96%

CO	Intrnal practical	DDE	OverallI	Level
CO-1	100%	96%	98%	3
CO-2	100%	96%	98%	3
CO-3	100%	96%	98%	3
CO-4	100%	96%	98%	3
CO-5	100%	96%	98%	3
CO-6	100%	96%	98%	3

Attainment Level	
1	40%
2	50%
3	60%

Attainment (Internal 2 Examination) = **3**

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Computer Science and Engineering

Course Outcome Attainment (University Examinations)

Name of the faculty : S.ALEKHYA Academic Year: 2022-23

Branch & Section: CSE - A Year / Semester: II/I

Course Name: A&DE Lab

S.No	Roll Number	Marks Secured
1	21X31A0501	72
2	21X31A0502	72
3	21X31A0503	73
4	21X31A0504	70
5	21X31A0505	72
6	21X31A0506	74
7	21X31A0507	70
8	21X31A0508	65
9	21X31A0509	72
10	21X31A0510	69
11	21X31A0511	72
12	21X31A0512	68
13	21X31A0513	73
14	21X31A0514	73
15	21X31A0515	73
16	21X31A0516	74
17	21X31A0517	72
18	21X31A0518	69
19	21X31A0519	73
20	21X31A0520	72
21	21X31A0521	74
22	21X31A0522	72
23	21X31A0523	73
24	21X31A0524	70
25	21X31A0525	73
26	21X31A0526	72
27	21X31A0527	74
28	21X31A0528	70
29	21X31A0529	71
30	21X31A0530	73
31	21X31A0531	68
32	21X31A0532	70
33	21X31A0533	74
34	21X31A0534	74
35	21X31A0535	69
Max Marks		75

S.No	Roll Number	Marks Secured
36	21X31A0536	68
37	21X31A0537	70
38	21X31A0538	69
39	21X31A0539	70
40	21X31A0540	70
41	21X31A0541	68
42	21X31A0542	69
43	21X31A0543	65
44	21X31A0544	70
45	21X31A0545	74
46	21X31A0546	66
47	21X31A0547	-1
48	21X31A0548	70
49	21X31A0549	70
50	21X31A0550	70
51	21X31A0552	69
52	21X31A0554	72
53	21X31A0555	70
54	21X31A0556	70
55	21X31A0557	70
56	21X31A0559	68
57	21X31A0560	71
58	21X31A0561	73
59	21X31A0562	70
60	21X31A0563	72
61	21X31A0564	70
62	21X31A0565	72
63	22X35A0501	70
64	22X35A0502	67
65	22X35A0503	72
66	22X35A0504	73
67	22X35A0505	71
68	22X35A0506	71
69	22X35A0507	-1
70	22X35A0508	73

Class Average mark	69
Number of students performed above the target	57
Number of successful students	68
Percentage of students scored more than target	84%
Attainment level	**3**

Attainment Level	% students
1	40%
2	50%
3	60%

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Computer Science and Engineering

Course Outcome Attainment

Name of the faculty : S.ALEKHYA
Branch & Section: CSE - A
Course Name: A&DE LAB

Academic Year: 2022-23
Examination: I Internal
Year: II
Semester: I

Course Outcomes	1st Internal Exam	2nd Internal Exam	Internal Exam	University Exam	Attainment Level
CO1	3.00	3.00	3.00	3.00	3.00
CO2	3.00	3.00	3.00	3.00	3.00
CO3	3.00	3.00	3.00	3.00	3.00
CO4	3.00	3.00	3.00	3.00	3.00
CO5	3.00	3.00	3.00	3.00	3.00
CO6	3.00	3.00	3.00	3.00	3.00
Internal & University Attainment:			3.00	3.00	
Weightage			70%	30%	
CO Attainment for the course (Internal, University)			2.10	0.90	
CO Attainment for the course (Direct Method)			3.00		

Overall course attainment level **3.00**

SRI INDU INSTITUTE OF ENGINEERING & TECHNOLOGY

Department of Computer science and Engineering

Program Outcome Attainment (from Course)

Name of Faculty:	S.ALEKHYA	Academic Year:	2022-23
Branch & Section:	CSE - A	Year:	II
Course Name:	A&DE Lab	Semester:	I

CO-PO mapping

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10	P11	P12	PSO1	PSO2
C216.1	3	3	-	3	-	-	-	-	-	-	-	-	3	3
C216.2	2	3	2	2	-	-	-	-	-	-	2	-	2	2
C216.3	2	3	2	2	-	-	-	-	-	-		3	3	3
C216.4	1	3	2	2	-	-	-	-	-	-	2	-	3	3
C216.5	3	2	1	2	-	-	-	-	-	-	-	3	2	2
C216.6	2	3	2		-	-	-	-	-	-	-	-	1	1
C216	**2.17**	**2.83**	**1.83**	**2**	-	-	-	-	-	-	**2**	**3**	**2.33**	**2.33**

CO	Course Outcome Attainment
CO1	3.00
CO2	3.00
CO3	3.00
CO4	3.00
CO5	3.00
CO6	3.00
Overall course attainment level	**3.00**

PO-ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO Attainment	**2.17**	**2.83**	**1.83**	**2.00**	-	-	-	-	-	-	**2.00**	**3.00**	**2.33**	**2.33**

CO contribution to PO - 33%, 67%, 100% (Level 1/2/3)